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PREFACE

During the last decade the technical community has witnessed a revolution in two superficially unrelated areas: VLSI development and digital signal processing. Close examination shows that they are not unrelated and that there is a high degree of synergy between them. Specifically, advances in VLSI have made it possible to successfully implement significant digital signal processing systems. The demonstrated utility of such digital signal processors has created a demand for even higher VLSI performance levels.

The purpose of this book is to provide architectural guidance to designers of signal processing systems and modules and the VLSI circuits needed to implement them. A related purpose is to illustrate successful application of the architectural concepts to real signal processing systems. Toward this goal, the book examines the algorithms, structures, and technology appropriate for development of special purpose systems. This strong applications orientation manifests itself in the inclusion of numerous examples and case studies. Such material is intended to provide motivation, indicate practical issues that arise in the development of real systems, and establish an intuitive feeling for the current state-of-the-art.

The first three chapters address VLSI from an internal and external architectural perspective. The next four chapters examine signal processing applications and implementation of example systems with VLSI. Finally, Chapter 8 provides an introduction to networking. Generalized networks are not now widely used

for signal processing systems, but as the networking field matures and as more signal processing systems become distributed (both physically and logically), the two fields will merge in much the same way that VLSI and signal processing have merged over the past decade.

This book is an outgrowth of a series of seminars presented in the United States and in Europe in the Spring of 1983. In fact, the seminars were based on work performed (and published) over the preceding decade. Subsequent to the seminars, many subsets of the material have been presented in tutorials, workshops, and technical briefings. Throughout this process many constructive comments have been made by the audiences that have greatly improved the presentation of the material.

Based on feedback from the various audiences, the book should be useful to engineers and managers working in VLSI and digital signal processing, and should be an effective supplement for graduate classes in signal processing. The book is oriented toward system and logic design. No attempt has been made to cover either VLSI processing or specific signal processing algorithm development.

A minor notational note is appropriate: throughout the book, log is used to indicate the base 2 logarithm while ln indicates the natural logarithm.

I would like to acknowledge my sincere gratitude to Lauren Hall who transcribed the original lectures and typed innumerable copies of the manuscript with a consistent cheerful attitude. Tracy Blyth and the support staff in TRW publications have provided significant assistance during the final manuscript preparation process. During the last decade, TRW has provided continued support and encouragement for my various activities in VLSI and signal processing. Such support is truly gratifying. Most of all I thank my wife, Joan, who radiates joy, happiness, and enthusiasm.

CONTENTS

CHAPTER 1.
THE VLSI CONTEXT

In the last 25 years a revolution in electronics has occurred. Component technology has evolved from discrete transistors to Very Large Scale Integrated (VLSI) circuits containing tens of thousands of transistors on a single chip. This chapter describes the changing technology environment in Section 1.1. The succeeding sections briefly describe the VLSI design process and the goals of the Very High Speed Integrated Circuit (VHSIC) program.

1.1 Technology Evolution

In 1964 Gordon Moore noted that the number of components per circuit for the most advanced integrated circuits had doubled every year since 1959 and predicted that the trend would continue [1-1]. More recently, he has modified "Moore's Law" showing an annual doubling from 1959 to 1975 and predicting a biannual doubling subsequent to 1975 [1-2] as charted in Figure 1-1.

It is convenient to categorize technology into four levels of integration as shown in Table 1-1. The complexity spans a four order of magnitude range. In the early to mid 1960s, Small Scale Integration (SSI) devices were being developed with 1 to 30 gates on a chip. At the Medium Scale Integration (MSI) level the number

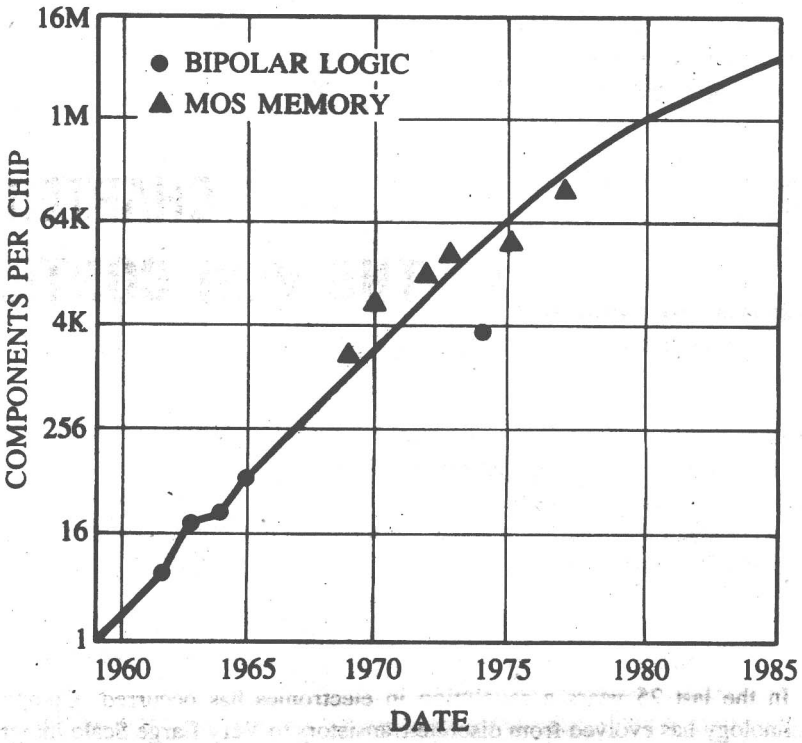

Figure 1-1. Moore's Law (After [1-2])

Integration Level	Introduced	Gates/Chips
Small Scale (SSI)	1964	1 to 30
Medium Scale (MSI)	1968	10 to 300
Large Scale (LSI)	1972	100 to 3K
Very Large Scale (VLSI)	1976	1K to 30K

Table 1-1. Historical Evolution

of gates on a chip increased by an order of magnitude to about 100 gates per chip. The Large Scale Integration (LSI) level began in the early 1970s with another order of magnitude increase in gate count. Early in the "LSI era" designers of electronic systems began to develop custom circuits tailored to the requirements of specific systems to reduce complexity and improve performance. Complex systems, consisting of many circuit boards of SSI and MSI devices could be reduced to a few custom chips thus simplifying the processor and reducing the production cost, power consumption, weight, etc. At the current VLSI level where circuits consist of tens of thousands of gates, the high nonrecurring cost of custom circuit development requires that the development effort is amortized across many projects. In the current environment a chip that is developed for a particular system will be designed with interfaces facilitating its use in other systems. Thus the chip development cost can be shared amongst the many systems that use it.

Table 1-2 shows typical circuit functions developed with the various levels of technology. The issues that have been the major concern to users at each functional level are identified. Early SSI device functions were gates and flip flops, i.e., simple traditional logic building blocks. These are the basic logic and memory functions that are taught in logic design classes. The companies that developed SSI circuits based their designs on the functions implemented with vacuum tube and transistor logic modules in early generations of digital computers. The largest user-issue then was critical mass; specifically, does a particular chip family have all of the functions needed to build a wide variety of systems? Will the logic designer get into a situation where the processor can be built except for one critical component that doesn't exist or is very difficult to implement? Some early families suffered from the lack of critical logic functions.

Integration	Function	User Issues
SSI	Gates, Flip-Flops	Critical Mass
MSI	Counters, 4 Bit Adders	Breadth
LSI	Memory, Microprocessors	Programming
VLSI	Signal Processors, Multipliers	System "Glue"

Table 1-2. Functional Evolution

The lack of critical components was effectively solved in the development of MSI, which was created by adding functions to the successful SSI families. The new functions were multiple adders, 4-bit wide binary, decimal, and duo-decimal counters, multiplexers, etc. These devices extended beyond previous computer modules into a higher level of complexity and were designed to complement the previous SSI circuits. The user's concern was which family had the widest breadth and would be most efficient in developing a variety of different systems. When MSI became available, most logic was standardized to Transistor-Transistor Logic (TTL) interfaces, so that users could mix components from several companies.

Within LSI, the most significant developments were memory and the microprocessor. Semiconductor Random Access Memory (RAM) was the first circuit to achieve LSI (and subsequently VLSI) levels of complexity. Dynamic RAM is a nearly ideal vehicle for technology demonstration since RAM circuits are developed by replicating a few cell types in two dimensional patterns. As a result the circuit design effort required to develop a new generation RAM is much less than the effort to develop a new logic circuit.

The microprocessor was a new system component unlike anything previously used. Users had to program the microprocessors to realize specific applications; a double edged sword. The microprocessor user achieves high flexibility because it is possible to reprogram the microprocessor to accommodate application changes even after a product is in the field. But, the traditional system designer was experienced in logic design and hardware development and generally knew little about programming and software. This forced users to learn a new discipline to take advantage of the LSI devices. As microprocessors advance to VLSI and higher integration levels, the programming aspect is mitigated. Higher level languages make it easier for relatively inexperienced software people to take full advantage of the microprocessors. At the LSI level, Metal Oxide Semiconductor (MOS) circuits were introduced. Generally, TTL interface levels are supported to simplify usage.

The first VLSI circuits were large dynamic RAM chips. Other early VLSI circuits are floating point arithmetic circuits and signal processing circuits. These VLSI chips provide the functional equivalent of several boards of LSI and MSI logic. An important VLSI issue is the desire to use new power supply and logic signal levels. So far, users have been willing to make speed and power sacrifices so that their VLSI chips will be compatible with previous technologies. In the future, new power supply and interface standards will necessitate redevelopment of support functions that are currently taken for granted.

The design source for integrated circuits is the next important issue. As shown in Table 1-3 with SSI and MSI circuits, the basic design source was generally the modules for mainframe computers. There were extensions to take advantage of the high density of MSI which were departures from previous computer modules. The largest issue, as mentioned earlier, was whether the resulting devices would be sufficiently universal for use in a variety of different applications. Certainly, if a semiconductor company developed a set of logic modules or a family of SSI and MSI chips based on the computer modules of a particular

Integration	Design Source	Issues
SSI, MSI	Computer Modules	Universality
LSI	Breakthrough	Testability
VLSI	Cellular Logic	

Table 1-3. Design Evolution

computer company; they knew the chips would have a good market with that computer company. The question was whether those chips would be usable in other systems or whether they would apply to only one computer line. Although many different logic families were developed in the 1960s, only a few remain viable today. The survivors are those that offered good performance and were reasonably universal. This universality was recognized and a number of semiconductor companies "second sourced" the chips of the families and worked with the original developer to create additional functions that were interoperable with the original chips.

Within LSI, many designs were extensions of MSI functions, but the design and concept of the microprocessor was a breakthrough. It was totally different from previous generations of circuits. For the first time performance was sacrificed to provide a high degree of programmability. The new emphasis was to strive for maximum flexibility by sacrificing speed and power to achieve flexibility.

VLSI began a trend back to cellular logic. This idea enjoyed some prominence in the 1950s in Automata theory for defining building blocks for Turing machines, universal computers, and self reproducing modules. Concurrently, there was a push to examine the use of arithmetic processes with a small library of primitive cells. Developing two or three cells that would snap together to build a larger function (in the same sense that pieces of a jigsaw puzzle snap together to create a picture) was envisioned. There was a very substantial sacrifice in speed and complexity for the cellular logic designs relative to custom, highly-optimized designs. The one advantage was that it was only necessary to develop a very small number of cell types. In present VLSI circuit design, minimizing the design effort by constructing a chip using replicated simple cells helps to circumvent the high design cost.

There is concern about testability at the LSI and VLSI levels of integration. VLSI circuits are often so complex that testability must be considered in the initial design phase. Even if a chip is testable, it may require impractically long test sequences. Such chips are hard for users to test and may complicate the diagnosis of problems within a system; for example, when a system fails, which chip or other part of the system has failed? The 1980s has witnessed a renewed interest in work on testability initiated in the 1950s. In the early days, the concern was with testability of large digital computers. Now single chips are as complex as early computers so that many of the same concepts apply.

1.2 The VLSI Design Process

Figure 1-2 shows how the system designer interacts with the VLSI design process. The designer develops preliminary chip specifications. These are analyzed to determine the implementation requirements; often in the form of algorithms and preliminary chip architectures. Where possible, the designer develops candidate architectures of cellular logic building blocks which are analyzed to determine the approximate complexity. An initial complexity assessment based on the complexity (i.e., gate count and memory requirements) and the required speed is used to develop an initial estimate of the proposed chip's complexity. Based on the complexity estimate, the chip feasibility is evaluated. If the estimated complexity is too low, the system application is reconsidered to determine if more of the system could be placed on the chip. If the estimated complexity is too high, it is necessary to determine if there is a lower complexity approach to implement the chip; perhaps sacrificing some performance, accuracy, etc. This process of estimating the complexity, evaluating the feasibility, and then modifying the specifications is repeated until a chip is defined that meets the complexity guidelines for the available technology. A more refined complexity estimate is made at that

point using the specific characteristics of the candidate technologies. For example, in a Complimentary MOS (CMOS) implementation, it might be possible to exploit the availability of bidirectional data transfer structures to reduce the chip complexity. When technology selection is complete, the classical chip development and fabrication process begins.

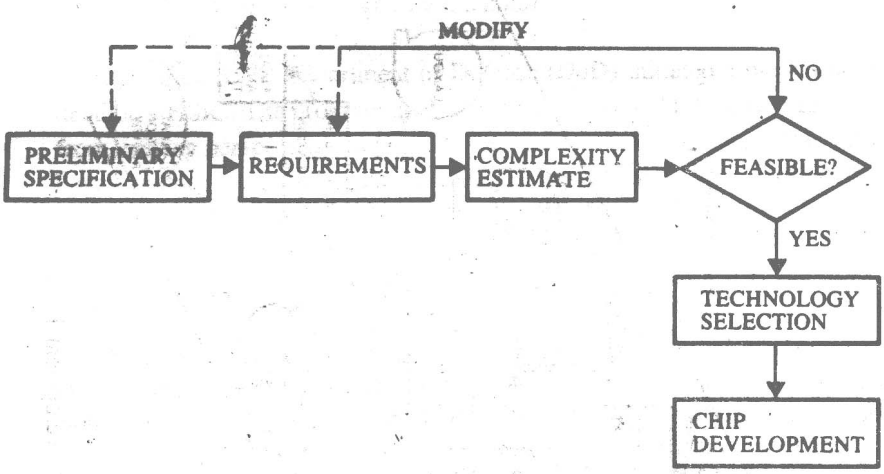

Figure 1-2. VLSI Design Process

Developing a preliminary specification and modifying it based on the available technology limits to produce a final specification are the first steps in the complete VLSI development process shown in Figure 1-3. Major steps in the development cycle include functional and gate level logic design, test design, circuit (i.e., silicon) design, layout, mask making, wafer fabrication, and final test. This book focuses on the functional, logic, and test design steps. The other development stages are effectively described in [1-3].

The benefits of VLSI are well known. Using VLSI, it becomes possible to implement a given system more efficiently. Fewer chips are used, thus the system is more reliable, lower in cost (assuming a reasonable production run), lower in power, smaller, and easier to support in the field. Alternatively, VLSI technology can be used to increase system performance while staying at a fixed complexity (i.e., cost, power, size, weight, etc.). In this scenario, VLSI implemen-

Figure 1-3. VLSI Development Process

tation provides better performance than conventional implementation. The performance improvements may be in the form of higher precision arithmetic, multiple elements operating in parallel to provide fault tolerance, a higher level of operating margin, etc.

1.3 Very High Speed Integrated Circuits

In 1980 the U.S. Department of Defense (DoD) initiated a major activity to develop VHSIC. The program goals are summarized in [1-4] with further details from varying perspectives in [1-5], [1-6], and [1-7]. The first program director, Larry Sumney, explains the initial accomplishments and hypotheses concerning the future of the VHSIC program and the VLSI industry in [1-8].

1.4 References

The book edited by Sze [1-3] provides an introduction to VLSI processing (i.e., crystal growth, epitaxy, photoresist, ion implementation, etc). The subscription series of [1-9] is an ongoing series that provides detailed information on various aspects ranging from VLSI processing to design and applications. The book edited by Dave Barbe [1-10] provides an overview of VLSI fundamentals. A good overview of bipolar and MOS circuit forms is included in [1-11]. Several conference/course proceedings have been published that identify current activities in VLSI design [1-12] — [1-16].

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CHAPTER 2. VLSI DESIGN

This chapter addresses three important topics. The first is the use of performance metrics to compare the performance of different technologies and to estimate the complexity of specific systems. These metrics are useful in assessing the feasibility of potential VLSI circuits, since the complexity required to implement candidate circuits is easily compared with the capability of the technology.

The second topic examined in this chapter is the use of semi-custom design. This can be a very efficient way to develop (i.e., design and fabricate) small to moderate production runs of specialized circuits. Semi-custom logic includes gate arrays and standard cell logic both of which use predesigned cells from a computer design library. By use of such cells, VLSI circuits are produced faster, for less cost, and with reduced risk relative to custom design.

VLSI constraints are identified in the last two sections of this chapter. The areas of packaging and testing currently represent critical limitations on the design and use of VLSI. These areas are examined in Sections 2.3 and 2.4, respectively.