V. Arvind
Sanjiva Prasad (Eds.)

FSTTCS 2007: Foundations of Software Technology and Theoretical Computer Science

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New Delhi, India, December 2007
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Preface

This volume contains the proceedings of the 27th annual conference on the Foundations of Software Technology and Theoretical Computer Science (FSTTCS 2007) held during December 12–14, 2007 at the India International Centre in New Delhi. The conference was organized under the auspices of the Indian Association for Research in Computing Science (IARCS).

This year's conference attracted 135 submissions from 31 countries. Except for a few papers that were outside the scope of the conference, each submission was assigned to at least three Programme Committee members, who, with the assistance of external expert researchers, ensured that each paper had at least three independent reviews. Given the high quality of the submissions, the Programme Committee decided to accept 40 papers. We thank all the expert reviewers for their invaluable help. We are very grateful to the PC members who put in enormous time and work in selecting the papers. Without their untiring efforts the conference would not have been possible.

The entire process of submission, refereeing, and the subsequent electronic PC meeting for selecting the papers for the conference program was greatly facilitated by the EasyChair conference management system; we would like to thank Andrei Voronkov and his team for this wonderful software.

One of the highlights of FSTTCS is the high quality of the invited talks. This year's conference was fortunate to have five very eminent invited speakers: Maurice Herlihy, Benjamin Pierce, Thomas Reps, Salil Vadhan, and Andrew Yao. Andrew Yao delivered the keynote address at the conference titled "A Modern Theory of Trust-but-Verify." In addition, Richard Karp, who could not make it to the conference to give his invited talk, kindly agreed to send an article for inclusion in the proceedings. It gives us great pleasure to thank all the invited speakers for agreeing to talk at the conference and for contributing to this volume.

Two satellite workshops were organized in conjunction with FSTTCS this year. These workshops were hosted by the Indian Institute of Technology Delhi. The conference was preceded by a one-day workshop on Compiler Techniques on December 11, felicitating Priti Shankar on her 60th birthday. Following the conference, on December 15, there was a one-day workshop on BioInformatics and Systems Biology organized by Neelima Gupta.

We thank the Organizing Committee for making all the arrangements for the conference. We thank IARCS and the sponsors for their support. As always, Alfred Hofmann and his team at Springer were very helpful in preparing the proceedings.

December 2007

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The Multicore Revolution
The Challenges for Theory

Maurice Herlihy*

Brown University Computer Science Department

Abstract. Computer architecture is undergoing, if not another revolution, then a vigorous shaking-up. The major chip manufacturers have, for the time being, simply given up trying to make processors run faster. Instead, they have recently started shipping "multicore" architectures, in which multiple processors (cores) communicate directly through shared hardware caches, providing increased concurrency instead of increased clock speed. As a result, system designers and software engineers can no longer rely on increasing clock speed to hide software bloat. Instead, they must somehow learn to make effective use of increasing parallelism. This adaptation will not be easy. Conventional synchronization techniques based on locks and conditions are unlikely to be effective in such a demanding environment. Coarse-grained locks, which protect relatively large amounts of data, do not scale, and fine-grained locks introduce substantial software engineering problems. Transactional memory is a computational model in which threads synchronize by optimistic, lock-free transactions. This synchronization model promises to alleviate many (perhaps not all) of the problems associated with locking, and there is a growing community of researchers working on both software and hardware support for this approach. This paper surveys the area, with a focus on open research problems.

1 Introduction

The computer industry is undergoing, if not another revolution, then a vigorous shaking-up. The major chip manufacturers have, for the time being, given up trying to make processors run faster. Moore's law has not been repealed: each year, more and more transistors fit into the same space, but their clock speed cannot be increased without overheating. Instead, attention is turning toward *multicore* architectures, in which multiple computing cores are included on each processor chip. Although these changes are propelled by changes in technology, they also provide a unique opportunity for theoretical distributed computing to have a substantial impact on practice. This paper suggests some promising research directions.

These trends mean that, in the medium term, advances in technology will provide increased parallelism, but not increased single-thread performance. System designers and software engineers can no longer rely on increasing clock speed

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