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High Performance Embedded Architectures and Compilers

First International Conference, HiPEAC 2005
Barcelona, Spain, November 2005
Proceedings

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Preface

As Chairmen of HiPEAC 2005, we have the pleasure of welcoming you to the proceedings of the first international conference promoted by the HiPEAC Network of Excellence. During the last year, HiPEAC has been building its clusters of researchers in computer architecture and advanced compiler techniques for embedded and high-performance computers. Recently, the Summer School has been the seed for a fruitful collaboration of renowned international faculty and young researchers from 23 countries with fresh new ideas. Now, the conference promises to be among the premier forums for discussion and debate on these research topics.

The prestige of a symposium is mainly determined by the quality of its technical program. This first program lived up to our high expectations, thanks to the large number of strong submissions. The Program Committee received a total of 84 submissions; only 17 were selected for presentation as full-length papers and another one as an invited paper. Each paper was rigorously reviewed by three Program Committee members and at least one external referee. Many reviewers spent a great amount of effort to provide detailed feedback. In many cases, such feedback along with constructive shepherding resulted in dramatic improvement in the quality of accepted papers. The names of the Program Committee members and the referees are listed in the proceedings. The net result of this team effort is that the symposium proceedings include outstanding contributions by authors from nine countries in three continents.

In addition to paper presentations, this first HiPEAC conference featured two keynotes delivered by prominent researchers from industry and academia. We would like to especially acknowledge Markus Levy and Per Stenström for agreeing to deliver invited lectures.

The Levy lecture focused on the development of multicore processor benchmarks that address both heterogeneous and homogenous processor implementations. The Stenström lecture covered new opportunities and challenges for the chip-multiprocessing paradigm. They both provided us with insight into current technology and new directions for research and development in compilers and embedded systems.

Many other people have contributed greatly to the organization of HiPEAC 2005. The Steering Committee members provided timely answers to numerous questions regarding all aspects of the symposium preparation. Josep Llosa, Eduard Ayguad and Pilar Armas, the local Chairmen and Financial Chair, covered many time-consuming tasks of organizing a symposium: hotel negotiation, symposium registration and administration. We thank Sally McKee for the publicity, and Michiel Ronsse for the website and support for the PC meeting. Many thanks also to the Publication Chair Theo Ungerer, his scientific assistants Jan Petzold

and Faruk Bagci for volume preparation, and to Springer for publishing these proceedings as *Lecture Notes in Computer Science.*

We would like to also note the support from the Sixth Framework Programme of the European Union, represented by our Project Officer Mercè Griera i Fisa, for sponsoring the event and the student travel grants.

Finally, we would like to thank the contributors and participants, whose interest is the reason for the success of this symposium.

September 2005

Tom Conte
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Invited Program

Keynote 1: Using EEMBC Benchmarks to Understand Processor Behavior in Embedded Applications

Markus Levy

President EEMBC

Abstract. Since its first introduction five years ago, benchmark software from the Embedded Microprocessor Benchmark Consortium (EEMBC) has gained critical mass as an industry standard for measuring the performance of embedded processors. From the beginning, EEMBC benchmarks have been distinguished by the application-specific representations of real processor tasks that they provide, and by the strict requirements for score certification before publication established by the Consortium. EEMBC is working to ensure its continued success by developing new benchmarks to reflect the evolving embedded market and to developing new ways to place the benchmark code in the hands of more engineers around the world.

This presentation begins with an introduction and overview of EEMBC's accomplishments and implementation strategy to date. From there, I will discuss the organization's future goals. Some of the hottest topics in the embedded industry include multicore systems and power conservation. Within EEMBC, work is now underway to develop multicore processor benchmarks that address both heterogeneous and homogenous processor implementations. A simultaneous effort is also underway, within a separate organization, to develop standards that will support the development of multicore platforms. These standards will initially address multicore debugging, on the chip and system level, and they will also address the issues of messaging and synchronization and how standards for scalable APIs could be leveraged and developed for embedded systems. On the power front, EEMBC is nearing the release of its specification for performing standardized power measurements on embedded platforms. Significantly, these measurements are performed while the platform is running the EEMBC benchmarks, thus helping to simultaneously characterize the performance and energy profile of a processor. But the real success of EEMBC's power measurements is that they work in a consistent manner, and, when released, will have been agreed to by the majority of vendors in the processor market.

This presentation will also describe other EEMBC benchmark projects currently under development, such as real-time automotive, office automation, and benchmarks to support VoIP applications. Using case studies, I will also demonstrate various methods for applying EEMBC to derive execution profiles and improve the designer's understanding of compiler and system-level design options.

Finally, the presentation will discuss how the adoption of these benchmarks within the embedded industry is expanding, with the implementa-

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