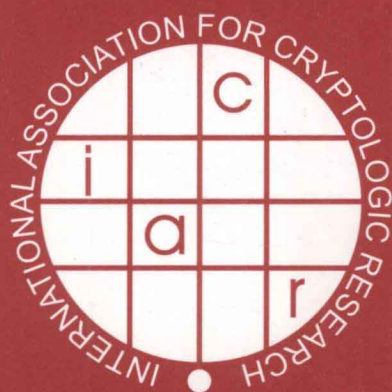


LNCS 4727

Pascal Paillier
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Cryptographic Hardware and Embedded Systems – CHES 2007

9th International Workshop
Vienna, Austria, September 2007
Proceedings



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Cryptographic Hardware and Embedded Systems - CHES 2007

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September 10-13, 2007
Proceedings

 Springer

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Library of Congress Control Number: 2007933579

CR Subject Classification (1998): E.3, C.2, C.3, B.7, G.2.1, D.4.6, K.6.5, F.2.1, J.2

LNCS Sublibrary: SL 4 – Security and Cryptology

ISSN 0302-9743
ISBN-10 3-540-74734-6 Springer Berlin Heidelberg New York
ISBN-13 978-3-540-74734-5 Springer Berlin Heidelberg New York

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Printed in Germany

Typesetting: Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India
Printed on acid-free paper SPIN: 12118106 06/3180 5 4 3 2 1 0

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Preface

CHES 2007, the ninth workshop on Cryptographic Hardware and Embedded Systems, was sponsored by the International Association for Cryptologic Research (IACR) and held in Vienna, Austria, September 10–13, 2007. The workshop received 99 submissions from 24 countries, of which the Program Committee (39 members from 15 countries) selected 31 for presentation. For the first time in the history of CHES, each submission was reviewed by at least four reviewers instead of three (and at least five for submissions by PC members, those now being limited to two per member) and many submitted papers have received plenty of extra reviews (some papers received up to nine reviews), thus totalling the unprecedented record of 483 reviews overall.

The papers collected in this volume represent cutting-edge worldwide research in the rapidly evolving fields of crypto-hardware, fault-based and side-channel cryptanalysis, and embedded cryptography, at the crossing of academic and industrial research. The wide diversity of subjects appearing in these proceedings covers virtually all related areas and shows our efforts to extend the scope of CHES more than usual. Although a relatively young workshop, CHES is now firmly established as a scientific event of reference appreciated by more and more renowned experts of theory and practice: many high-quality works were submitted, all of which, sadly, could not be accepted. Selecting from so many good works is no easy task and our deepest thanks go to the members of the Program Committee for their involvement, excellence, and team spirit. We are grateful to the numerous external reviewers listed below for their expertise and assistance in our deliberations.

In addition to the contributions appearing in these proceedings, the workshop program included two invited lectures given by Kim Nguyen and Pankaj Rohatgi. The program also included the traditional rump session, chaired by Nigel Smart, featuring short informal talks on late-breaking research news. This year's rump session was augmented with a parallel demo and poster session welcoming informal presentations of prototypes, attack demos and research works. The Program and Steering Committees commonly agreed on giving the CHES 2007 Best Paper Award to two papers: "Arithmetic Operators for Pairing-Based Cryptography" by Jean-Luc Beuchat, Nicolas Brisebarre, Jérémie Detrey and Eiji Okamoto (University of Tsukuba, Université Monnet and École Normale Supérieure de Lyon) and "Side Channel Cryptanalysis of a Higher Order Masking" by Jean-Sébastien Coron, Emmanuel Prouff and Matthieu Rivain (University of Luxembourg and Oberthur Card Systems). The purpose of the award is to formally acknowledge authors of outstanding papers and to recognize excellence in their research works. Interestingly, these two works represent well the two sides of our field: efficient implementations and hardware-based cryptanalysis.

Ingrid and myself deeply thank Elisabeth Oswald (University of Bristol, UK, and Graz University of Technology, Austria), the General Chair of CHES 2007, for her excellent work managing the local organization and orchestrating the conference logistics. We are grateful to Thomas Herlea (KUL, Belgium) for diligently maintaining the Web system. The review and discussion process was run using e-mail and the WebReview software by Wim Moreau and Joris Claessens. We also owe our gratitude to Lejla Batina (also from KUL) for her help in preparing the call for papers and the proceedings. We would like to deeply thank the Steering Committee and personally Jean-Jacques Quisquater (UCL, Belgium) for his support, trust and kind advice at many occasions. We would also like to thank the Institute for Applied Information Processing and Communications (IAIK) of Graz University of Technology for assisting with local arrangements. Our gratitude also goes to our generous sponsors, namely, Cryptography Research, Comodo, Novacard, Thomson, Infineon and IBM. We heartily thank all those who have contributed to make this workshop a reality: we are forever in your debt.

Finally, we would like to profoundly thank and salute all those who, from all over the world, submitted their work to this workshop as well as all the speakers who provided the scientific contents of CHES 2007: the success of the CHES series is their success and reflects every year the vitality of our community.

July 2007

Pascal Paillier
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A First-Order DPA Attack Against AES in Counter Mode with Unknown Initial Counter

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Abstract. Previous first-order differential power analysis (DPA) attacks have depended on knowledge of the target algorithm’s input or output. This paper describes a first-order DPA attack against AES in counter mode, in which the initial counter and output values are all unknown.

Keywords: power analysis, SPA, DPA, HO-DPA, AES, counter mode.

1 Introduction

Previous first-order differential power analysis (DPA) attacks have depended on knowledge of the target algorithm’s input or output [1][2]. This paper describes a first-order DPA attack against the Advanced Encryption Standard (AES) [3] in counter mode, in which the initial counter, input values, and output values are all unknown.

The attack proceeds as follows. Suppose the input data to an algorithm is unknown, but can be expressed as single secret constant summed with known, variable data. The known, variable part of the data is used to mount a DPA attack, and the secret constant is treated as part of the key to be recovered. The “key” recovered by the DPA attack is then a function of the actual key and the secret constant. The known input values are then combined with the recovered “key” to compute the actual intermediate values produced by the algorithm. The recovered intermediates are then used to carry the attack forward into later rounds, enabling additional DPA attacks to recover the real key.

The attack also addresses the challenges to DPA presented by block ciphers used in counter mode [4]. DPA attacks target secrets when they are mixed with known *variable* quantities. In counter mode only the low-order bits of the input change with each encryption. Hence there are few variable intermediates to target in the first round of a typical block cipher. We demonstrate a method for propagating the attack into later rounds in which more known, variable data is available.

Although counter mode presents additional challenges to DPA attacks, in certain respects it also makes the attack easier. Unlike most first-order DPA attacks, the sequential nature of the counter enables the attack to succeed with

only knowledge of the power measurements. Knowledge of input, output, and initial counter values are not required to implement the attack.

1.1 Related Work

Simple power analysis (SPA) attacks have been used to extract portions of keys directly from power traces without requiring knowledge of input messages. Fahn and Pearson used inferential power analysis (IPA), an attack that exploits binary SPA leaks [5]. Mayer-Sommer presented attacks exploiting SPA leaks in high-amplitude power variations [6]. Mangard presented an SPA attack against the AES key expansion step [7]. Messerges et al described SPA attacks on Hamming weight and transition count leaks [8].

Side channel collision attacks were introduced by Dobbertin, and have traditionally targeted SPA leaks using chosen ciphertext [9] [10] [11]. Side channel collision attacks can be adapted to the case in which inputs are known to be successive values of a counter.

High-order differential power analysis (HO-DPA) [12] attacks target a hypothesized key-dependent relationship between data parameters in a computation. Previous work has noted that HO-DPA attacks can be applied to situations in which cipher input values are not known [13].

Fouque and Valette presented the “doubling attack” [14] which exploits the relationship between inputs in successive RSA decryptions to recover the exponent. The attack succeeds despite the fact that the input to the modular exponentiation step is masked by a blinding factor. Messerges presented a second-order DPA attack [15] that defeated a data whitening scheme.

Chari et al [16] and Akkar et al [17] also presented DPA attacks on block ciphers with a “whitening” step.

2 Preliminaries

2.1 Notation

Suppose X and Y are used to denote input and output data of a transformation. (Letters other than X or Y will also be used.) If the transformation is implemented as a sequence of rounds, the input and output of the i^{th} round are denoted by X_i and Y_i .

Within a round, data may be partitioned into bytes for processing. $X_{i,j}$ and $Y_{i,j}$ denote the j^{th} bytes of round data X_i and Y_i .

K is used to denote input keys, K_i denotes the i^{th} round key derived from K , and $K_{i,j}$ denotes the j^{th} byte of round key K_i .

Symbols

The symbol $\oplus$ denotes the bitwise XOR of two n -bit vectors.

The symbol $+$ denotes the ordinary addition of two numbers.

The symbol $\circ$ denotes multiplication between two elements of $GF(2^8)$.

The symbol $\parallel$ denotes the concatenation of two vectors.