

Richard J. Boulton  
Paul B. Jackson (Eds.)

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# Theorem Proving in Higher Order Logics

14th International Conference, TPHOLs 2001  
Edinburgh, Scotland, UK, September 2001  
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## Preface

This volume constitutes the proceedings of the *14th International Conference on Theorem Proving in Higher Order Logics* (TPHOLs 2001) held 3–6 September 2001 in Edinburgh, Scotland. TPHOLs covers all aspects of theorem proving in higher order logics, as well as related topics in theorem proving and verification.

TPHOLs 2001 was collocated with the *11th Advanced Research Working Conference on Correct Hardware Design and Verification Methods* (CHARME 2001). This was held 4–7 September 2001 in nearby Livingston, Scotland at the Institute for System Level Integration, and a joint half-day session of talks was arranged for the 5th September in Edinburgh. An excursion to Traquair House and a banquet in the Playfair Library of Old College, University of Edinburgh were also jointly organized. The proceedings of CHARME 2001 have been published as volume 2144 of Springer-Verlag's *Lecture Notes in Computer Science* series, with Tiziana Margaria and Tom Melham as editors.

Each of the 47 papers submitted in the full research category was refereed by at least 3 reviewers who were selected by the Program Committee. Of these submissions, 23 were accepted for presentation at the conference and publication in this volume. In keeping with tradition, TPHOLs 2001 also offered a venue for the presentation of work in progress, where researchers invite discussion by means of a brief preliminary talk and then discuss their work at a poster session. A supplementary proceedings containing associated papers for work in progress was published by the Division of Informatics at the University of Edinburgh.

The organizers are grateful to Bart Jacobs and N. Shankar for agreeing to give invited talks at TPHOLs 2001, and to Steven D. Johnson for agreeing to give an invited talk at the joint session with CHARME 2001. Much of Bart Jacobs's research is on formal methods for object-oriented languages, and he is currently coordinator of a multi-site project funded by the European Union on tool-assisted specification and verification of JavaCard programs. His talk covered his own research and research of this project. A three page abstract on the background to his talk is included in this volume. N. Shankar is one of the principal architects of the popular PVS theorem prover, and has published widely on many theorem-proving related topics. He talked about the kinds of decision procedures that can be deployed in a higher-order-logic setting and the opportunities for interaction between them. We are very pleased to include an accompanying paper in these proceedings. Steven D. Johnson is a prominent figure in the formal methods community. His talk surveyed formalized system design from the perspective of research in interactive reasoning. He contrasted two interactive formalisms: one based on logic and proof, the other based on transformations and equivalence. The latter has been the subject of Johnson's research since the early 1980s. An abstract for this talk is included in these proceedings, and a full accompanying paper can be found in the CHARME 2001 proceedings.



The TPHOLs conference traditionally changes continent each year in order to maximize the chances that researchers all over the world can attend. Starting in 1993, the proceedings of TPHOLs and its predecessor workshops have been published in the following volumes of the Springer-Verlag *Lecture Notes in Computer Science* series:

1993 (Canada)	780	1997 (USA)	1275
1994 (Malta)	859	1998 (Australia)	1479
1995 (USA)	971	1999 (France)	1690
1996 (Finland)	1125	2000 (USA)	1869

The 2001 conference was organized by a team from the Division of Informatics at the University of Edinburgh and the Department of Computing Science at the University of Glasgow.

Financial support came from Intel and Microsoft Research. The University of Glasgow funded publicity and the University of Edinburgh loaned computing equipment. This support is gratefully acknowledged.

June 2001

*Richard J. Boulton, Paul Jackson*

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Bart Jacobs (Nijmegen)  
 Steven D. Johnson (Indiana) (*joint with CHARME 2001*)  
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# JavaCard Program Verification

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**Abstract.** This abstract provides some background information on smart cards, and explains the challenges these cards represent for formal verification of software.

## Smart Card Trends

Increasingly, physical keys are being replaced by cryptographic keys, which are typically a thousand bits in size. Modern smart cards are the ideal carriers for such keys, because they have enough computing power to do the necessary en- or de-cryption on-card, so that the secret key never has to leave the card. Smart cards are meant to be tamper-resistant secure tokens, typically bound to individuals via a PIN, possibly in combination with biometric identification.

Modern smart cards contain a standard interface (API) for a mini-operating system which is capable of executing application programs (called *applets*) written in high-level languages. The standard language in this area is JavaCard [Che00], which is a “superset of a subset” of Java: it is a simplified version of Java (no threads, multi-dimensional arrays, floats or doubles) with some special features, like persistent objects and a transaction-commit mechanism. Two further characteristics of modern smart cards are:

- **Multi-application.** One card can hold multiple applets for different applications. These are typically centered around the basic cryptographic functions, in for example banking, telecommunication (GSM or UMTS SIMs), access to buildings or networks, identification, voting, *etc.*) Limited communication can be allowed between applets, *e.g.* for automatically adding loyalty points after certain commercial transactions.
- **Post-issuance Downloading.** In principle, it is possible to add applets to a card after it has been issued. This option gives enormous flexibility, but is disabled for security reasons in all currently operational cards.

Security evaluation and certification are very important in the smart card area, because cards are distributed in large numbers for security critical applications. Correctness should be established both for the card platform, and for applets.

## Challenges for Formal Methods

The so-called Common Criteria<sup>1</sup> form a standard for the evaluation of IT security. They are much used for smart cards. The Common Criteria involve seven different levels of evaluation, where the two highest levels (6 and 7) require the explicit use of formal methods. Currently available smart cards are evaluated at levels 4 and 5, but there is a clear pressure to move to higher levels. Therefore the smart card industry is open to the use of formal methods. For the formal verification community smart cards form an ideal target since they are within reach of existing verification tools, because of their limited size.

### VerifiCard: Aims

In 2000 a European research consortium called VerifiCard<sup>2</sup> was set up, with support from the European Union's IST programme. Its aim is to apply the existing verification tools (mostly theorem provers, but also model checkers) to establish the correctness of JavaCard-based smart cards. The approach is pragmatic: no new development of semantics of Java(Card) from scratch, but application of available expertise and experience in Europe in tool-assisted formal methods, to see what can be achieved in a concentrated effort in a small, well-defined area. This is a potential killer application for formal methods in software verification, which can cut in two directions: if this succeeds, the success may spread to other areas. But if this fails there may be a serious setback for formal methods in software: it is bad news if these methods cannot deliver for such relatively small systems as smart cards.

### VerifiCard: Work

The VerifiCard consortium consists of five academic partners, some of which are well-known in the TPHOLs community: Nijmegen (coordinator; Jacobs, Poll), INRIA (Barthe, Bertot, Jensen, Paulin-Mohring), Munich (Nipkow, Strecker), Hagen (Poetzsch-Heffter), SICS (Dam). Also, the consortium involves two smart card manufacturers: Gemplus and SchlumbergerSema (formerly Bull CP8). The planned work is roughly divided along two lines: source code / byte code, and platform / applets. The work involves for instance formalization of the JavaCard virtual machine and byte code verifier, non-interference properties, and specification and verification of the API and of individual applets. Towards the end of the project the industrial partners will carry out a tool-evaluation, to see which approaches can contribute most to their evaluation needs.

### Scientific Work of Nijmegen

The talk will elaborate on the work done at Nijmegen, as part of VerifiCard. This involves verification of JavaCard programs, that are part of the API and applets.

<sup>1</sup> See <http://www.commoncriteria.org>.

<sup>2</sup> See <http://www.verificard.org>.



The correctness properties are specified using the interface specification language JML [LBR99], developed by Gary Leavens *et al.* in Iowa, see *e.g.* [PBJ01]. A Java(Card) program with JML annotation is translated to PVS using the LOOP tool [BJ01]. Actual verification in PVS proceeds via a tailor-made Hoare logic for JML [JP01]. See [BJP01] for a small case study, involving the AID class from the JavaCard API. Basically, the verification technology for Java is there, but scaling it up to larger programs is still a real challenge.

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# View from the Fringe of the Fringe

## (Joint with CHARME 2001)

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**Abstract.** Formal analysis remains outside the mainstream of system design practice. Theorem proving is regarded by many to be on the margin of exploratory and applied research activity in this formalized system design. Although it may seem relatively academic, it is vital that this avenue continue to be as vigorously explored as approaches favoring highly automated reasoning. Design derivation, a term for design formalisms based on transformations and equivalence, represents just a small twig on the theorem-proving branch of formal system analysis. A perspective on current trends in is presented from this remote outpost, including a review of the author's work since the early 1980s.

A full accompanying paper can be found in the CHARME 2001 proceedings [1].

## References

- [1] Steven D. Johnson. View from the fringe of the fringe. In Tiziana Margaria and Tom Melham, editors, *Proceedings of 11th Advanced Research Workshop on Correct Hardware Design and Verification Methods (CHARME 2001)*, volume 2144 of *Lecture Notes in Computer Science*. Springer Verlag, 2001.