VLSI Electronics Microstructure Science

Volume 7

Edited by

Norman G. Einspruch

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College of Engineering
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Preface

Civilization has passed the threshold of the second industrial revolution. The first industrial revolution, which was based upon the steam engine, enabled man to multiply his physical capabilities to do work. The second industrial revolution, which is based upon semiconductor electronics, is enabling man to multiply his intellectual capabilities. VLSI (Very Large Scale Integration) electronics, the most advanced state of semiconductor electronics, represents a remarkable application of scientific knowledge to the requirements of technology. This treatise is published in recognition of the need for a comprehensive exposition that describes the state of this science and technology and that assesses trends for the future of VLSI electronics and the scientific base that supports its development.

These volumes are addressed to scientists and engineers who wish to become familiar with this rapidly developing field, basic researchers interested in the physics and chemistry of materials and processes, device designers concerned with the fundamental character of and limitations to device performance, systems architects who will be charged with tying VLSI circuits together, and engineers concerned with utilization of VLSI circuits in specific areas of application.

This treatise includes subjects that range from microscopic aspects of materials behavior and device performance—through the technologies that are incorporated in the fabrication of VLSI circuits—to the comprehension of VLSI in systems applications.

The volumes are organized as a coherent series of stand-alone chapters, each prepared by a recognized authority. The chapters are written so that specific topics of interest can be read and digested without regard to chapters that appear elsewhere in the sequence.

There is a general concern that the base of science that underlies integrated circuit technology has been depleted to a considerable extent and is in need of revitalization; this issue is addressed in the National Research

Council (National Academy of Sciences/National Academy of Engineering) report entitled "Microstructure Science, Engineering and Technology." It is hoped that this treatise will provide background and stimulus for further work on the physics and chemistry of structures that have dimensions that lie in the submicrometer domain and the use of these structures in serving the needs of humankind.

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Chapter 1

Advanced Manufacturing Equipment for VLSI Lithography

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I. INTRODUCTION

A. General Introduction

The microelectronics industry has seen an astonishing growth since the advent of the miniaturized transistor, and there is no a priori reason why this growth should not continue to surprise both participants within the industry and onlookers without. The reason for this enthusiasm is straightforwardly stated in terms of the incredible potential for a wide range of VLSI applications from huge consumer markets to smaller but highly profitable technical, medical, and scientific needs. Obviously, the predicted growth of computer use and computer-oriented skills is a major factor.

Central to this growth is the role to be played by microlithography, and it behooves manufacturers of such equipment to adopt a very aggressive attitude lest they be guilty of limiting the progress made. There are three central challenges facing the ongoing development of microlithographic technology when it is viewed strategically and one critical problem when the emphasis is placed on details of technology. To examine this somewhat oversimplified view of our present position, we shall begin by noting that the bulk of the lithographic work is carried out by photon optical systems, while in the wing two new, but unproven, technologies—electron-beam (e-beam) lithography and x-ray lithography—await their call to the stage. The choice of the emphasis to be placed on the proven technology relative to the two new contenders represents one of the major challenges. We are at an exciting threshold in relation to factory automation and the application of computer technology to industry in general. A prime candidate here is the VLSI industry. This is our second main challenge. How do we automate the industry so as to increase cost-effectiveness? This particular problem covers a wide range of technologies from the use of computer-aided design (CAD) for the devices themselves through the entwined processes of microlithography, pattern development, and structure formation to the final processes of device testing and establishing the necessary data banks to monitor performance. Both in concept and in terms of detailed practicalities, we

have extensive interplays and trade-offs to consider. Finally, there is the question of cost-effectiveness. The systems we shall discuss are, of necessity, complex and costly because of the sophistication of the problem we are tackling and the conditions under which it is undertaken. We have to make such systems reliable, easy to maintain, capable of self-diagnostics, and usable with insignificant downtime.

When the problem is viewed technically, a strong case can be made to support the view that the major technical limitation facing us today is the alignment and overlay of the successive patterns from which integrated devices are compounded. This viewpoint differs from that of recent years during which the emphasis was placed on resolution, i.e., on our ability to achieve the ultimate in miniaturization of the patterns to be established. Now this aspect of the specification has been overtaken by difficulties associated with the correct location of one pattern on top of the other.

The preceding paragraphs set the general background against which practical microlithographic systems have to be developed. Because of space limitations, we have had to be selective in our content and emphasis. We have elected to stress the area involving device fabrication in which the minimum feature size (see Subsection I.B) is in the region of 1 μm. The reason for this choice is that this is the most significant work area for the 1980s in terms of practical realization on the factory floor. This selectivity limits the techniques that can be discussed fully (see Subsection I.B). Any analysis of contending microlithographic approaches has to be undertaken against a reasonable prediction of the industry's short- and long-term needs, both in the developmental laboratory and, particularly, on the factory floor. In the next section we shall outline such a prediction, taking an appropriately aggressive outlook and stressing factory usage.

B. Industry Needs in the 1980s

Qualitatively stated, the challenge is to make the individual devices themselves smaller and smaller and, at the same time, to integrate more and more of them onto one chip. In other words, both the packing density itself and the total number of devices within a chip are contributory factors toward increasing productivity and cost-effectiveness. For our present purposes and without loss of generality, we shall work in terms of packing density, or, equivalently, in terms of the corresponding minimum feature size. Table I gives the market prediction expressed as a function of time in terms of this parameter. A point can be made about Table I that concerns the major uncertainty, i.e., that involving time scale. The uncertainties increase as the projection is extended, with the major uncertainty centered

TABLE I
Predicted Industry Needs through the 1980s in Terms of Required Minimum Feature Size

Time scale	Required minimum feature (μm)	Comment
1982	2.00–2.50 (approx. 3.0)	Today's design rules in practice
1984	1.25–1.50 (approx. 2.0)	IC fabrication at this level planned and implemented with increasing stress
1986	1.00 (1.25 → 1.5)	Instrument, system, and fabrication facilities being planned and funded on the basis of extensive developmental experience
1988–1990	0.5 (approx. 1.0)	Considerable e-beam experience gained both in the private sector and with government support

on the 0.5-μm level. These uncertainties do not represent a difficulty in our considerations here, which are mainly concerned with performance. When one bears in mind the need to be aggressive and the fact that it takes some three years to develop and prove out systems of this complexity, it is of little relevance to argue that the 1.0-μm level may be needed in 1985 or may be delayed until 1987. In any case, there will be a spectrum of individual needs, both within any one organization and from one fabrication house to the next. Here we ask nothing more of the data given in Table I than that the 1.25–1.50-μm level be effectively planned for, that the long-term features relating to the 1.0-μm level be actively under way, and that some uncertainty exist with regard to the 0.5-μm level. For completeness we have added a further datum in Table I related to time scale. The figures given for required minimum feature size and discussed so far represent the aggressive outlook appropriate to developmental planning. In parentheses, we have added a more conservative estimate of what in reality will evolve. This estimate is based on the opinions of experienced workers in this area.

To sustain this drive toward higher packing density, we have to consider technologies based on

(1) photon optics: (a) steppers, (b) scanners, and (c) holographic systems,
(2) electron-beam technology,
(3) x rays, and
(4) ion-beam technology.

In the present context, we shall stress optical steppers, electron-beam technology, and approaches using x rays. The approach based on optical scanners is not stressed because it is too limited in application below the 1.5-μm level. Similarly, ion-beam technology will not be considered in depth

because it is somewhat too futuristic at present. On the same basis, we have omitted considerations of lithography based on holographic procedures, which still need further developmental work.

In the next section, we shall outline the specifications that practical systems have to attain.

II. THE NATURE OF THE LITHOGRAPHIC PROCESS

A. System Specification—Main Parameters

In this section, we shall outline the challenges facing the microlithographer. This is best done in terms of the salient parameters that define the system and that are listed below. Contained within the listing and the associated descriptions is a summary of the ways in which integrated devices are fabricated today.

1. Resolution

Much of the notation applicable to photography is pertinent here, because several of the "photographic" processes are exploited. The designer of VLSI circuits breaks up the problem into a series of patterned layers that have to be superimposed on the underlying silicon. The imposition of each pattern consists of two steps. Expressed in terms of optical lithography, the pattern is first transferred to a light-sensitive layer—a resist layer—that has been deposited on the appropriate semiconductor wafer. This optical transfer is best done by exposures using high-quality microprojection lenses that give a significantly reduced image size and are capable of using high numerical apertures with extended sources. Subsequently, the exposed pattern is "developed," usually by chemical means, to give a silicon wafer "exposed," i.e., unprotected, in some areas while protected in others. The pattern is then transferred to the silicon itself either by "wet," i.e., chemical, or by "dry," i.e., active gas, etchants. The term *resolution* is used here in two or three contexts. *Optical resolution* refers to the quality of the projected light distribution, i.e., the smallest resolvable feature that can be obtained optically. The resolution obtainable in the resist pattern represents the optical resolution convoluted by the resist properties. This latter *resist resolution* is directly measurable and is an oft-used measure of lithographic performance. Finally, there is the resolution of the structure etched into the silicon itself. This resolution reflects not only optical and resist properties but the features of the etching process as well. These three resolutions are quantitatively close to each other and are monotonically variant.

2. Control of Critical Dimension Size

Obviously, it is insufficient just to achieve a given resolution, i.e., a minimum feature size, over part of the exposure area. We have to achieve it over the whole area. Not only that, but we have to *maintain* this performance over extended periods of time. So to specify the size of a given feature, we have to specify the allowed tolerance range about this value. In practice we would require a 1-μm line to be 1.0 ± 0.1 μm for the 3 sigma point of a normal distribution. The monitoring and control of such dimensions are referred to as critical dimension (CD) control, which is one of the most important methods of ensuring ongoing cost-effectiveness.

3. Alignment/Overlay

The previous paragraphs deal with the formation of a single pattern layer, but the device is the superimposition of several layers. Not only does any single patterned layer have to maintain positional accuracy throughout itself, but each layer has to be correctly related to the previous one. This problem of the correct relation between patterns is referred to as the alignment/overlay task and is *the* significant limitation to microlithography at present. It is a near-convention within the industry to divide the total alignment/overlay problem into two separate areas of responsibility. First, we are concerned with the *precision* of the pattern. By this term we mean the accuracy of placement of the "center of gravity" of a given shape relative to some origin. This factor is mainly the concern of mask makers, pattern generators, etc. Second, we have variations of the size of the feature. These variations can be caused by processing, by exposure uncertainties, etc., and they can contribute to the *total overlay* error; i.e., they affect the accuracy to which we can place two *edges* relative to each other. *Alignment* is probably best used to describe the process of establishing the best total overlay. But there are variants in usage, and here we refer to the total problem as the alignment/overlay problem.

4. Process–System Interactions

In practice the semiconductor wafer is subjected to a series of process steps both before and after the superimposition of a given pattern. These steps can subject the wafer to relatively hostile environments in terms of both temperature range and reactive chemicals. Temperature itself and the deposition/removal of surface layers can result in geometrical distortion both in the plane of the wafer and in the normal to the wafer plane. Etchants, contaminants, and surface dust can cause loss of significant detail and thus device failure. Overly rapid temperature changes can compound the difficulties. A particularly complex interaction occurs between the resist technology and

the alignment problem (see Subsection II.C). All of these work areas come within the range of device–processing system interactions and each involves the same basic trade-off between freedom of action for the device engineer on the one side and accuracy/precision needs of the microlithographer on the other.

5. Throughput/Uptime/Output

System throughput is a measure of the system's ability to expose resist-covered wafers. Usually measured in wafers per hour, this parameter is a straightforward measure of the instrument's capability that is unaffected by the learning curve of the user, the degree of discipline imposed on the fabrication areas, etc. To complete the assessment of the system we specify the *uptime* of a system; i.e., we give a realistic prediction of the fraction of the available time that a system can be expected to operate at its full throughput. Again, some ambiguity of terms occurs here, depending on the depth of detail with which a given dialogue is concerned. Here we are concerned with the performance after the system has been set up and the necessary learning curve completed. In the *initial* stages, *setup time* has a significant meaning, particularly under competitive conditions. To incorporate factors relating both to system usage and, particularly, to customer usage, we introduce the concept of yield, or the fraction of the started devices that become saleable products. Finally, estimates of throughput, uptime, and yield are combined to give a measure of output, i.e., the number of useful devices manufactured per shift, per month, etc.

6. Cost/Performance

Finally, we have to assess the system in terms of its total performance, that is, its ability to produce profit. Performance, or cost-effectiveness, is an appropriate measure of the number of useful products divided by the cost of producing the devices. This assessment is both critical and complex, because the contributions to cost are many and varied and the manner in which they are treated depends strongly on the financial procedures appropriate to a given customer or to a particular time.

We can now use the framework established by this list of salient parameters to give quantitative estimates of the capability of each technology.

B. Resolution

There is a strong consensus that resolution is not a significant limitation at present. As a result of the application of excellent CAD capabilities and modern fabrication/quality-control techniques, it is probable that optical

microlithography will produce 0.75-μm minimum features on a commercial basis, will reach 0.6-μm in the developmental laboratory, and, with the application of special resist techniques, will reach approximately 0.6 and 0.5 μm in the factory and laboratory, respectively. These improvements in resolution can be obtained with lenses capable of giving extensive areas of exposure by using high numerical apertures so that no unacceptable limitation is imposed on other areas affecting throughput or customer usage, etc.

In practical environments x-ray techniques can operate at a resolution of 0.25 μm. X-ray protagonists may argue that higher resolution is obtainable. This comment is true in the laboratory, but in production the very acceptable figure just given is appropriate. The analogous figure for electron-beam lithography is 0.10 μm. This figure is some 10 times greater than can be achieved in the laboratory. At the 0.10–0.25-μm level, we are in a regime in which several potential limitations in other areas pose severe problems, including questions involving device operation itself. In summary, we can say that there are significant areas of concern to be faced in our drive toward the ultimate in miniaturization before we are impacted by resolution. Compare this situation with the alignment/overlay area.

C. Alignment/Overlay

Alignment/overlay is *the* problem currently facing microlithographers. From the viewpoint of the device manufacturer, there is considerable pressure to improve our ability to overlay patterns. For example, by improving overlay it has proved possible simply to shrink existing devices and chips without changing fabrication procedures and without continuing outlay in developmental funds and new facilities. The net result has been devices with increased performance produced more cost-effectively with minimal developmental time and cost.

The manufacturer of microlithographic equipment can only regard alignment/overlay as an upfront work area, because it quickly enters into initial dialogues between vendors and would-be customers. Alignment/overlay is the first parameter put to practical test and so can set the tone of subsequent interactions. To the designer of microlithographic systems, it presents some unique challenges.

(i) The designer does not have the total problem under control. For an established house serving a wide range of customers, a wide range of processing techniques is used with a wide, and often significant, impact on the alignment procedure. This interaction is going to increase as the resist systems used become increasingly complex. An example, given in passing, is the use of bi- or trilevel resists with up to 3 μm of resist above previously