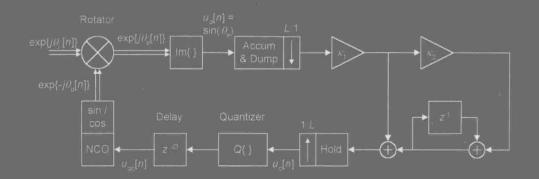


Phaselock Techniques

Third Edition

Floyd M. Gardner



PHASELOCK TECHNIQUES

Third Edition

FLOYD M. GARDNER

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PREFACE

The first edition of this book was published in 1966 and the second in 1979. Phaselock was an unimaginably exotic subject in 1966, with limited applications and few practitioners. Now phaselock is a mature subject: myriads of phaselock loops are ensconced in the world's electronic devices; numerous applications include phaselock loops; large numbers of practitioners deal with phaselock. No other books on phaselock loops existed when the first edition was published, but more than 20 exist today. Why is a third edition justified at this time?

In 1966, a simple, short introduction to the basics of the subject was needed for an audience for whom phaselock was strange and new. Today, phaselock loops are firmly established in the mainstream of electronics engineering. Much new information on phaselock loops has accumulated over the years, and several topics once thought important have proved to be ephemeral. Experience has taught me that certain explanations would be better presented from revised viewpoints.

There is no need for another introductory text; that function is well served by a number of the books listed in Section 1.3 and probably others as well. Instead, this book reexamines the traditional phaselock topics in greater depth than previously. In addition, much new material has been included, some of it never before published. Examples of additions include revised and expanded material on transfer functions, two chapters related to phase noise, two chapters related to digital phaselock loops, a chapter on charge-pump phaselock loops, expanded material on phase detectors, and a chapter on anomalous phaselocking.

As in the earlier editions, only minimal space has been devoted to circuits. The book is concerned with underlying principles, which remain valid despite technology advances, not with implementations, which change drastically as technology changes. Several parts of the second edition have been omitted: the chapters on

XVIII PREFACE

optimization and synchronization, and the mathematical appendix. Formal optimization has not proved to be as important to design as was earlier anticipated; instead, a designer is much more likely to perform a trade-off among the few parameters available in a practical phaselock loop. The mathematical appendix has been omitted on the premise that the level of mathematics presented here should be comfortable for all electrical engineering graduates. Synchronization (recovery of carrier and clock from data signals), a major discipline of its own, was deemed to have grown too large to cover adequately in a book on phaselock loops. See Section 17.1 for a brief guide to synchronization.

Simulation is another absent topic. Information presented in several chapters is based on simulations, certain kinds of new data can be gathered only by simulation, and simulation is crucial for design and verification of integrated circuits. Nonetheless, the book does not tell how to conduct simulations of phaselock loops. That topic deserves a separate book of its own; it is too extensive to include here.

Many thousands of articles and books on phaselock have appeared worldwide over the years, far too many to cite individually. Although many pertinent references have been cited in the individual chapters of the book, it is not possible to discover every valuable publication written on each topic. Nor, after many years of work on the subject, is it possible always to remember who originated every technique that is presented. I apologize in advance to anyone who may have been slighted; the omission is not deliberate.

Several guidelines have been followed in selecting reference citations for each chapter: The reference is to an original work; wherever possible, the reference appeared in a public, archival publication; the reference treats lasting principles rather than transitory details of implementation. A reader will observe a preponderance of citations to IEEE publications and to books published in the United States. This choice reflects the omnipresence of IEEE publications and also the contents of my personal library.

I want to thank my many clients over the years who have afforded me the opportunities to learn so much about such a fascinating subject.

FLOYD M. GARDNER

Palo Alto, California October 2004

NOTATION

Α	Amplitude
B_i	Bandwidth (Hz) of an input bandpass filter
B_L	Noise bandwidth (Hz) of a PLL
b	Number of bits in a digital word
b	Ratio of frequency of a pole to frequency of a zero
f	Frequency (Hz)
f	Transform variable of Fourier transforms
f_c	Comparison frequency (Hz) at a phase detector
f_{ck}	Clock frequency (Hz)
f_m	Frequency (Hz) of modulation
f_s	Sampling frequency (Hz), = $1/t_s$
Δf	Peak frequency deviation (Hz)
$rac{\Delta f}{\delta f}$	Frequency offset (Hz) from a carrier
δf	Frequency increment (Hz) in a quantized-tuning oscillator
D	Delay (sample intervals)
E(f)	$=E(s) _{s=j2\pi f}$
E(s)	Closed-loop error transfer function of a PLL
F(s)	Transfer function of a loop filter
FP[x]	Fractional part of x
G(s)	Open-loop transfer function of a PLL
H(f)	$=H(s) _{s=j2\pi f}$
H(s)	Closed-loop system transfer function of a PLL
Im[x]	Imaginary part of x
IP[x]	Integer part of x
i	Subscript denoting "input"

XX NOTATION

i	An integer
$J_n(x)$	Bessel function of the first kind, order n , and argument x
j	$\sqrt{-1}$
K	Loop gain (rad/sec) of a PLL
<i>K'</i>	Normalized (dimensionless) loop gain, = $K\tau_2$
K_d	Gain (V/rad or A/rad) of a phase detector
K_{DC}	DC gain (rad/sec) of a PLL
K_i	Gain coefficient in analog PLL, $i = 1, 2,$
K_m	Gain (V^{-1}) of a multiplier
K_o	Gain (rad/sec·V) of a VCO
K_p	Gain (V/cycle) of a phase detector = $2\pi K_d$
K_v	Gain (Hz/V) of a VCO, = $K_o/2\pi$
k	An integer
$L\{x\}$	Laplace transform of x
$\mathcal{L}(f)$	Normalized one-sided RF spectrum of a signal
m, M	An integer
m(t)	Modulation waveshape
N_0	One-sided spectrum (V^2/Hz) of white noise
n, N	An integer
n(t)	Noise voltage (V)
$n_c(t), n_s(t)$	Baseband quadrature components of bandpass noise (V)
0	Subscript denoting "output" or "oscillator"
$P_{RF}(f)$	Spectrum analyzer representation of the one-sided spectral
_	density of an RF signal
P_s	Signal power (W)
p	Normalized Laplace variable, $= s\tau_2$
Q	Quality factor of a resonator
Q	Number of quantization levels
Q	Division ratio
Re[x]	Real part of x
r(t)	Received signal
$s = \sigma + j\omega$	Transform complex variable of a Laplace transform
SNR	Signal-to-noise ratio
SNR_L	Signal-to-noise ratio in PLL noise bandwidth $2B_L$
ť	Time (sec)
t_s	Sampling interval (sec), $= 1/f_s$
$u_c[n]$	Sample- <i>n</i> control input (dimensionless) to an NCO
$u_d[n]$	Sample-n output (dimensionless) of a digital
***	phase detector
V_o	Peak output voltage (V) of a VCO
V_s	Peak voltage (V) of an input signal
$v_c(t), V_c(s)$	VCO control voltage (V)
$v_d(t), V_d(s)$	Phase detector output (V)
$W_{n'}(f)$	One-sided spectral density (rad ² /Hz) of the equivalent noise
	out of a phase detector

NOTATION XXI

$W_{\theta no}(f)$	One-sided spectral density of the VCO phase (rad ² /Hz) due to
	the noise input to a PLL
$W_{RF}(f)$	Measured one-sided spectral density (V ² /Hz) of an RF signal
$W_{vo}(f)$	Theoretical one-sided spectral density (V ² /Hz) of an oscillator output
$W_{\phi}(f)$	One-sided baseband spectrum (rad ² /Hz) of phase noise
Z	Transform variable of z-transforms

Greek Symbols

α	Signal suppression factor (dimensionless) in a limiter
β	Modulation index (rad) of angle modulation
γ	Crest factor of a signal
$\varepsilon[n]$	Sample <i>n</i> of phase (cycles)
ζ	Damping factor of a second-order PLL
$\overset{\circ}{ heta}$	Phase angle (rad)
θ_a	Steady-state phase error (rad) due to frequency-ramp input
θ_e	Phase error (rad) between an input signal and a
	$VCO_i = \theta_i - \theta_o$
θ_i	Phase angle (rad) of an input signal
θ_{no}	Fluctuation of VCO phase (rad) caused by noise
θ_o	VCO phase (rad)
$ heta_v$	Steady-state phase error (static phase error; loop stress) due to
	frequency offset
$\Delta heta$	Phase deviation (rad)
$\Delta heta$	Amplitude (rad) of phase step
κ	Loop gain (dimensionless) in a digital PLL
κ_d	Gain (rad ⁻¹) of a digital phase detector
κ_i	Gain coefficient in a digital PLL, $i = 1, 2,$
κ_o	Gain (rad) of a NCO
κ_p	Gain (cycle ⁻¹) of a digital phase detector, = $2\pi \kappa_d$
κ_v	Gain (cycles) of an NCO, = $\kappa_o/2\pi$
Λ	Rate of change (rad/sec ²) of frequency, = $d\omega/dt$
ρ	Signal-to-noise ratio
σ_{x}	Standard deviation of x
τ	Timing error (sec)
τ	Delay (sec)
$ au_i$	Time constant (sec), $i = 1, 2, \dots$
$ au_2$	Time constant (sec) of stabilizing zero in a type 2 PLL
$\phi(t)$	Phase noise (rad)
ψ	Angle (rad) around a unit circle
ψ	Normalized frequency (dimensionless), = ωt_s
$\psi(s)$	Phase (rad) of a transfer function
ψ_{gc}	Normalized unity-gain crossover frequency $\omega_{gc}t_s$ of open-loop transfer function of sampled PLL, $ G(e^{j\psi_{gc}}) = 1$

XXII NOTATION

ω	Angular frequency (rad/sec), = $2\pi f$
ω_c	Comparison frequency (rad/sec) at a phase detector, = $2\pi f_c$
ω_{gc}	Unity-gain crossover frequency (rad/sec) of open-loop transfer function, $ G(j\omega_{gc}) = 1$
ω_m	Modulating frequency (rad/sec)
ω_n	Natural frequency (rad/sec) of a second-order PLL
ω_{π}	Phase crossover frequency (rad/sec), $Arg[G(j\omega_{\pi})] = -\pi$
$\Delta \omega$	Frequency offset or frequency step (rad/sec)
$\Delta \omega_H$	Hold-in limit (rad/sec) of a PLL
$\Delta\omega_L$	Lock-in limit (rad/sec) of a PLL
$\Delta\omega_P$	Pull-in limit (rad/sec) of a PLL

CONTENTS

PR	EFACE	.		XVII
VO	TATIO	N		xix
1	INTR	TION	1	
	1.1	Salient	Properties of PLLs / 2	
		1.1.1	Bandwidth / 2	
		1.1.2	Linearity / 3	
	1.2	Organiz	zation of the Book / 3	
	1.3	Annota	ted Bibliography / 3	
		1.3.1	Books / 3	
		1.3.2	Reprint Volumes / 4	
		1.3.3	Journal Special Issues / 5	
2	TRAI	NSFER	FUNCTIONS OF ANALOG PLLs	6
	2.1	Basic 7	Fransfer Functions / 6	
		2.1.1	Transfer Functions of Individual Elements / 7	
		2.1.2	Combined Transfer Functions / 8	
		2.1.3	Characteristic Equation / 9	
		2.1.4	Nomenclature, Coefficients, and Units / 9	
	2.2	Second	-Order PLLs / 10	
		2.2.1	Loop Filters / 10	
		2.2.2	Order and Type / 12	

viii CONTENTS

2.2.3 Loop Parameters / 12

3

	2.2.4	Frequency Response / 15			
2.3	Other Loop Types and Orders / 20				
	2.3.1	General Definition of Loop Gain K / 20			
	2.3.2	Examples of Type 1 PLLs / 22			
	2.3.3	Examples of Type 2 PLLs / 24			
	2.3.4	Higher-Type PLLs / 28			
	Referen	ice / 28			
GRA	PHICAL	AIDS	29		
3.1	Root-Le	ocus Plots / 30			
	3.1.1	Description of Root-Locus Plots / 30			
	3.1.2	Stability Criterion / 33			
	3.1.3	Root Loci of Type 1 PLLs / 33			
	3.1.4	Root Loci of Type 2 PLLs / 33			
	3.1.5	Root Loci of Type 3 PLLs / 34			
	3.1.6	Root Loci of Higher-Order PLLs / 35			
	3.1.7	Effect of Loop Delay on Root Locus / 38			
3.2 Bode Plots / 38		lots / 38			
	3.2.1	Presentation Options / 38			
	3.2.2	Stability / 39			
	3.2.3	Bode Plots of Type 1 PLLs / 40			
	3.2.4	Bode Plots of Type 2 PLLs / 43			
	3.2.5	Bode Plots of Type 3 PLLs / 48			
3.3	Nyquis	t Diagrams / 49			
3.4	Nichols	Charts / 49			
	3.4.1	Stability Criterion / 49			
	3.4.2	M-Contours / 50			
	3.4.3	Examples of Nichols Charts / 50			
3.5	Closed-	Loop Frequency-Response Curves / 52			
	Append	lix 3A: Salient Features of Root Loci / 52			
	3A.1	Branches of Root Loci / 53			
	3A.2	Locus on the Real Axis / 53			
	3A.3	Locus Intersections with Axes / 54			
	Append	lix 3B: Formats of the Open-Loop Transfer Function $G(s)$ / 56			
	3B.1	Proportional-Plus-Integral Section / 56			
	3B.2	High-Frequency Section / 60			
	3B.3	Calculations / 60			

CONTENTS

Appendix 3C: Closed-Loop Frequency Responses / 61

4

	3C.1	Frequency-Response Formulas / 61	
	3C.2	Example Frequency-Response Graphs / 61	
	Referer	nces / 64	
	TAL PLI ATED TO	s: Transfer functions and Dols	65
4.1	Distinc	tive Properties of Digital PLLs / 65	
4.2	Digital	Transfer Function / 66	
	4.2.1	Configuration of a Digital PLL / 66	
	4.2.2	Difference Equations / 67	
	4.2.3	z-Transforms of the Loop Elements / 69	
	4.2.4	Loop Filter / 70	
	4.2.5	Loop Transfer Functions / 71	
	4.2.6	Poles and Zeros / 71	
4.3	Loop S	tability / 73	
	4.3.1	Type 1 DPLLs / 73	
	4.3.2	Type 2 DPLLs / 73	
	4.3.3	Type 3 DPLLs / 74	
4.4	Root-L	ocus Plots / 74	
	4.4.1	Root Loci of Type 1 DPLLs / 75	
	4.4.2	Root Loci of Type 2 DPLLs / 75	
	4.4.3	Root Loci of Type 3 DPLLs / 78	
4.5		Frequency Responses: Formulation / 79	
4.6		Plots and Nichols Charts / 80	
		Basis of Bode Plots / 80	
		Bode Stability Criteria / 81	
		Bode Plots of Example DPLLs / 81	
		Nichols Chart Example / 83	
4.7		Continuous Approximation for a DPLL / 85	
4.8	-	ncy-Response Examples / 86	
	4.8.1	Effect of Delay / 86	
	4.8.2	Effect of Bandwidth / 87	
4.9	-	ss Filters in the Loop / 88	
	4.9.1	Infinite Impulse Response Lowpass Filter / 88	
	4.9.2	Finite Impulse Response Lowpass Filter / 90	
		dix 4A: Stability of Digital Phaselock Loops / 91	
	4A.1	Type 1 DPLL / 92	
	4A.2	Type 2 DPLL / 93	
	Referen	nce / 96	

X CONTENTS

5	TRAC	CKING		97	
	5.1	Linear	Tracking / 97		
		5.1.1	Steady-State Phase Errors / 98		
		5.1.2	Transient Response / 100		
		5.1.3	Response to Sinusoidal Angle Modulation / 109		
	5.2	Nonline	ear Tracking: Lock Limits / 112		
		5.2.1	Phase-Detector Nonlinearity / 112		
		5.2.2	Steady-State Limits / 112		
		5.2.3	Transient Limits / 114		
		5.2.4	Modulation Limits / 118		
		References / 121			
6	EFFE	CTS OF	ADDITIVE NOISE	123	
	6.1	Linear	Operation / 123		
	0.1		Noise Model of a Phase Detector / 123		
			Noise Transfer Function / 129		
			Noise Bandwidth / 129		
			Signal-to-Noise Ratio in a PLL / 131		
			Optimality / 132		
	6.2		ear Operation / 132		
			Observed Behavior / 133		
		6.2.2	Nonlinear Analysis of Phase Error / 135		
			Probability Density and Variance / 136		
			Cycle Slips / 137		
			Experimental and Simulation Results / 138		
			Approximate Analyses / 138		
			Miscellaneous Features / 139		
		Referen	nces / 141		
7	EFFE	CTS OI	F PHASE NOISE	143	
	7.1	Propert	ies of Phase Noise / 144		
		7.1.1	Oscillator Model / 144		
		0.0 500 50	Neglect of Amplitude Noise / 144		
		7.1.3	Variance / 144		
		7.1.4	Nonstationarity / 144		
	7.2		of Phase Noise / 146		
		7.2.1	Theoretical Spectrum $W_{vo}(f)$ / 146		
		7.2.2	Normalized Spectrum $\mathcal{L}(\Delta f)$ / 147		
		7.2.3	RF Spectra $W_{RF}(f)$ and $P_{RF}(f)$ / 147		
			Phase-Noise Spectrum $W_{+}(f)$ / 149		

CONTENTS Xi

	7.2.5 Frequency-Noise Spectrum $W_{\omega}(f)$ / 152		
	7.2.6	Example Phase-Noise Spectrum / 152	
7.3	-	ies of Phase-Noise Spectra / 153	
		Typical Continuous Spectra / 154	
	7.3.2	Meaning of $W_{\phi}(f)$ / 155	
	7.3.3	Interpretation of Spectral Displays / 156	
		Relationship Between $W_{\phi}(f)$ and $\mathcal{L}(\Delta f)$ / 157	
7.4	Propaga	ation of Phase Noise / 159	
	7.4.1	Phase-Noise Propagation in Auxiliary Devices / 159	
	7.4.2	Phase-Noise Propagation in PLLs / 161	
7.5	Integrat	ted Phase Noise in PLLs / 162	
	7.5.1	Basic Formulas / 162	
	7.5.2	Excessive Phase Noise / 163	
	7.5.3	Effect on Coherent Demodulation / 163	
	7.5.4	Bandwidth Trade-off / 163	
	7.5.5	Integration / 164	
		A Paradox / 165	
	7.5.7	Integration of Spectral Lines / 166	
		Phase-Noise Specifications / 166	
7.6 Timing Jitter / 167		Jitter / 167	
	Append	lix 7A: Analysis of Interference in a Hard	
		Limiter / 168	
	Appendix 7B: Integrals of Untracked Phase Noise / 169		
7B.1 Integration Procedures / 169			
	7B.2	Results of Integrations / 169	
	7B.3	Discussion / 171	
	Append	lix 7C: Numerical Integration of PLL Phase	
		Noise / 171	
	7C.1	Definition and Application of Integrated Phase	
		Noise / 172	
		Data Formats / 172	
		Data Adjustments / 173	
	7C.4	Data Filtering / 174	
	7C.5		
	Append	lix 7D: Integration of Discrete Lines in the	
Phase-Noise Spectrum / 175			
	70.7	dix 7E: Timing Jitter / 177	
	7E.1	Jitter Definitions / 177	
	7E.2	0.0001 III 1 === 0 , 1,7	
	Referer	nces / 180	

Xİİ CONTENTS

8	ACQ	UISITION OF PHASELOCK	183	
	8.1	Characterization / 183		
	8.2	Phase Acquisition / 184		
		8.2.1 First-Order Loop / 184		
		8.2.2 Hang-up / 186		
		8.2.3 Lock-in / 186		
		8.2.4 Aided Phase Acquisition / 188		
	8.3	Frequency Acquisition / 189		
		8.3.1 Frequency Pull-in / 189		
		8.3.2 Frequency Sweeping / 195		
		8.3.3 Discriminator-Aided Frequency Acquisition / 199		
		8.3.4 Implementation of Frequency		
		Discriminators / 203		
	8.4	Diverse Matters / 204		
		8.4.1 Lock Indicators / 204		
		8.4.2 Wide-Bandwidth Methods / 205		
8.4.3 Memory / 206				
	References / 206			
9	9 OSCILLATORS		209	
9.1 Desired Properties / 209		Desired Properties / 209		
	9.2 Classes of Oscillators / 210			
	9.3 Phase Noise in Oscillators: Simplified Approach / 210			
	9.3.1 Leeson's Model / 210			
		9.3.2 Guides for Oscillator Design / 212		
		9.3.3 Example Phase-Noise Spectra / 213		
		9.3.4 Shortcomings of Leeson's Model / 214		
	9.4	Classifications of Oscillators / 215		
	9.5	Phase Noise in Oscillators: Advanced Analysis / 217		
		9.5.1 Impulse Sensitivity Function / 218		
	0.6	9.5.2 Nonlinear Analyses for Phase Noise / 219		
	9.6	Other Disturbances / 221		
	9.7	- T-7		
		9.7.1 Continuous-Tuning Oscillators / 223		
	0.0	9.7.2 Discrete-Tuning Oscillators / 224		
	9.8	Tuning of Analog VCOs / 226 9.8.1 Tuning Curve / 227		
		8		
		9.8.2 Tuning Methods / 228 9.8.3 Speed of Tuning / 231		
		References / 232		
		References / LJL		

CONTENTS

10	PHAS	HASE DETECTORS		
	10.1	Multiplier Phase Detectors / 237		
			ching Phase Detectors: Principles / 238	
			ching Phase Detectors: Examples / 240	
			rid-Transformer PD / 244	
		· ·	sinusoidal s-Curves / 245	
	10.2	Sequential Ph	nase Detectors / 246	
	10.3	0.3 Phase/Frequency Detector / 248		
		_	Configuration / 248	
		10.3.2 Dela	y in PFD / 250	
		10.3.3 PFD	State Diagram / 251	
		10.3.4 PFD	s-Curve / 252	
		10.3.5 Freq	uency Detection in a PFD / 253	
		10.3.6 Effec	cts of Delay in a PFD / 254	
		10.3.7 Extra	a or Missed Transitions / 255	
		10.3.8 Lock	Indicator for a PFD / 256	
	10.4	Behavior of l	Phase Detectors in Noise / 256	
		10.4.1 Band	lpass Limiters / 256	
		10.4.2 Phas	e-Detector Noise Threshold / 258	
		10.4.3 s-Cu	rve Shape in Noise / 259	
		10.4.4 Jitter	Dependence on s-Curve Shape / 260	
	10.5 Two-Phase (Complex) Phase Detectors / 2		Complex) Phase Detectors / 260	
Appendix 10A: Phase Modulation Due to Phase-Detector Ripple / 262				
			ole Model / 262	
		10A.2 Basi	s of Analysis / 263	
		10A.3 Ripp	ole Examples / 263	
			ole Filters / 264	
	References / 265			
11	LOO	P FILTERS		267
	11.1	11.1 Active vs. Passive Loop Filters / 267		
	11.2	DC Offset /	•	
	11.3	Transient Ov	erload / 269	
		11.3.1 Over	rload from PD Ripple / 269	
		11.3.2 Over	rload During Acquisition / 269	
12	СНА	RGE-PUMP I	PHASELOCK LOOPS	271
	12.1	Model of a C	Charge Pump / 271	
	12.2 Loop Filter / 273			

XÍV CONTENTS

	12.3	2.3 Static Phase Error / 274		
	12.4 Stability Issues / 27512.5 Nonlinearities / 276			
	12.6	Ripple Suppression / 278		
	12.7 Late Developments / 280		evelopments / 280	
		Referen	nces / 281	
13	DIGITAL (SAMPLED) PHASELOCK LOOPS			282
	13.1	QuasiLinear Sampled PLLs / 283		
		13.1.1	Digital-Controlled Oscillators / 283	
		13.1.2	Hybrid Phase Detectors / 286	
		13.1.3	Complex-Signal Digital Phase Detector / 289	
		13.1.4	DPLLs in Digital Data Receivers / 290	
		13.1.5	Loop Stability / 294	
	13.2 Quantization / 294		zation / 294	
		13.2.1	Lessons from Related Studies / 294	
		13.2.2	Quantization Considerations in Hybrid PLLs / 295	
		13.2.3	Effects of Frequency (NCO) Quantization / 296	
		13.2.4	Quantization in a Phase Detector and an Integrator / 311	
	13.3 Irremediably Nonlinear PLLs / 312		liably Nonlinear PLLs / 312	
		13.3.1	Configuration of a Nonlinear PLL / 312	
		13.3.2	Operation of the PLL Elements / 314	
		13.3.3	PLL State Diagrams / 317	
		13.3.4	Operation of the Nonlinear PLL / 319	
		13.3.5	Type 2 Nonlinear PLL / 322	
		13.3.6	Effects of Additive Noise / 324	
		13.3.7	Application to Bit Synchronizers / 326	
		Appendix 13A: Transfer Function of a Multirate DPLL / 327		
		13A.1	Nomenclature / 327	
		13A.2	Phase-Detector Operation / 327	
		13A.3	Accumulate & Dump and the Loop Filter / 327	
		13A.4	Hold Process / 328	
		13A.5	NCO, Phase Rotator, and $M:1$ Down-Sampling / 329	
		13A.6	Transfer Functions / 330	
		13A.7	Transfer Function of a Hold Filter / 332	
		Referen	nces / 333	