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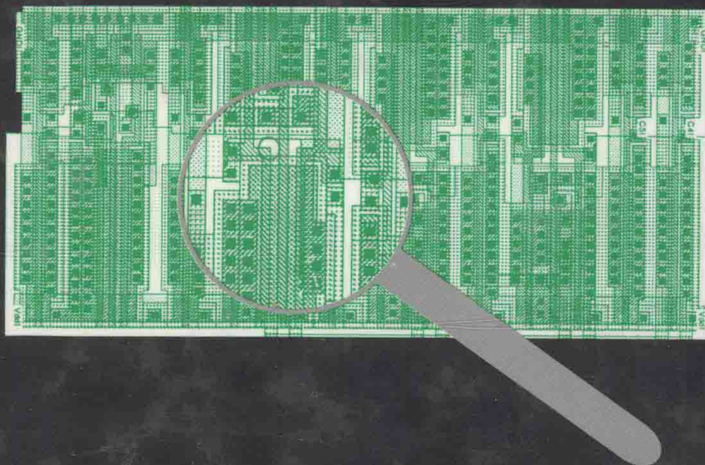
Transistor-Level Fault Modeling and Testing



Rochit Rajsuman

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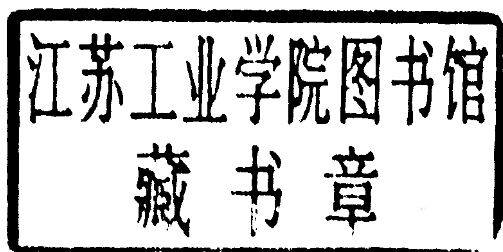

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This book is dedicated to scientists, engineers, and anyone else who seeks knowledge and keeps politics out of that search.

Preface

Generally, one hears that writing a book is an extremely difficult job. Popular belief is that many, many long hours and weekends are needed to finish a book in a timely fashion. Somehow, I was dubious and now I am glad that I did not believe it. I have seen many friends who did not initiate a book writing project because of this belief and sometimes because of a little discouragement from an "old pro." Also, by saying a job is extremely difficult, one may get a little extra credit and respect from the community. There is probably no harm in that (I would like to do so!), as long as first-time writers do not become discouraged. So, I have decided to tell of the actual effort in writing this book.

During my PhD studies, I found some myths regarding certain concepts related to VLSI testing. The idea of writing a book developed during a walk around Case Western Reserve University (CWRU) campus on a summer afternoon in 1990. Because of another research project, I could not do anything during the summer. In the fall, I prepared a proposal and started talking to the publishers.

From the start, I tried to measure the time and effort, but I cannot assign a number to the time spent during my PhD work, where I became acquainted with various topics related to VLSI testing. At that time, I read almost all the papers from the major conferences and journals (the list is given in Appendix B). So, when I prepared the proposal, I had a clear-cut idea about what to write and in how much depth. In the proposal, I also sorted out the sequence of topics and prepared three sample chapters for the publisher. These sample chapters were prepared in a very rough form, intentionally, so that I would receive a critical review. I estimate the total time for proposal and sample chapters as about two months, while performing all my other duties as normal. One may consider that as a full-time job for a month.

The review of the proposal and sample chapters took much more time than the writing itself. For about six months, I sat and waited. The reviews from one publisher were a little surprising and much more negative than I had anticipated.

The reviewer firmly believed that a comprehensive book covering most of the topics could not be written in six months. The publisher was still willing to take a chance, but, due to some other logistical problems, that deal did not go through. When I was looking for a publisher, I accidentally came across the Artech House, Inc. The Artech House staff treated me in such a wonderful manner that I immediately dropped correspondence with everyone else. This whole process took about six months. During this period, there was no work except for some phone calls or filling out a few requisition forms.

The actual writing did not start until June 1991. Before the summer ended, I had reworked the original sample chapters and written two more chapters. In August, when classes started, I scheduled my time to avoid any conflict. I made a policy to work only during regular working hours. I also kept my door open to the students and allowed them to stop by at any time to discuss anything from VLSI to UFOs. This open door policy spoiled the students, but at the time it gave me a break from the work. With all this and my normal duties (although, I could not publish the usual number of papers during this period), I had no problem whatsoever in finishing the whole manuscript by mid-December.

Based on this experience, my advice to anybody considering writing a book is that it does not matter if you are not very serious at this time; prepare an outline of the contents and contact a publisher. The scientific community needs good books. Being in academics, I know; I need good books. Pay no attention if someone says that it is a difficult job and you might exhaust yourself.

Having related this story, let me explain the organization and contents of the book. The first four chapters are devoted to the fault models and complexity of the testing problem. The reason for devoting four chapters to this topic is that it is poorly described in existing books. The complexity and testability analysis are needed in the beginning, but it has been given no consideration in the existing literature. Similarly, the bridging faults and open faults are the most important failure modes, but none of the books covers them. Thus, I was essentially forced to write separate chapters on these topics.

The second part of this book, Chapters 5 and 6, are devoted to the testing of combinational circuits. Chapter 5 includes a general test method applicable to random logic and Chapter 6 includes the testing of PLAs. Although a PLA also may implement a finite state machine, Chapter 6 is restricted to combinational testing. In these chapters, I also tried to include topics that are not covered in other books (i.e., algorithm FAN, switch level test generation, and the testing of EEPLAs).

Chapters 7 to 10 can be considered as the third part of this book, which is devoted to the testing of all types of sequential circuits, with or without extra hardware. Whereas memory testing is one of the most important topics, it is somehow left out of most books. To compensate for this deficiency, Chapter 7 is devoted to memory testing. Similar reasons apply to Chapters 8 and 9. All existing books

include no more than one subsection (describing the checking experiment) on the testing of sequential circuits, while microprocessor testing is virtually ignored. To fill this gap, Chapter 8 is devoted to the testing of sequential circuits and Chapter 9 to the microprocessor testing. Chapter 10 includes the design for testability and built-in self-test methods. This chapter describes all the major testing techniques that use extra hardware. It may appear to be a concise chapter, but it indeed provides complete information.

Chapter 11 covers a new topic, IDDQ or current testing. Apart from brief mention, this topic has not even been referred to in any other book. Chapter 12 covers special test methods related to reliability. These test methods have been used in the industry for a long time. No shipment is made without completing reliability testing, but no book even mentions this topic.

I have tried to capture the basic knowledge in the area of IC testing and include all the major techniques. One topic that I could not include is testing for timing or delay faults. The delay fault model is included in Chapter 2, and Appendix B lists a few basic papers on this topic. One may also find that in some places I have not mentioned a program or the implementation of a particular algorithm. Sometimes, this was intentional, but otherwise due to limited space. However, I tried not to neglect the basic algorithm. I hope readers will be satisfied and able to find most of the concepts in these pages.

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