# Electronic Devices and Circuit Theory

**Eighth Edition** 

Visit the website at www.prenhall.com/boylestad

Robert L. Boylestad Louis Nashelsky

RELOGISTICATE TO SELECTION OF THE PROPERTY OF

### EIGHTH EDITION

# Electronic Devices and Circuit Theory

ROBERT L. BOYLESTAD LOUIS NASHELSKY



Upper Saddle River, New Jersey Columbus, Ohio

#### Library of Congress Cataloging-in-Publication Data

Boylestad, Robert L.

Electronic devices and circuit theory / Robert Boylestad, Louis Nashelsky.—8th ed.

p. cm.

ISBN 0-13-028483-1 (alk. paper)

1. Electronic circuits. 2. Electronic apparatus and appliances.

I. Nashelsky, Louis. II. Title.

TK7867 .B66 2002

621.3815—dc21

2001021973

Editor in Chief: Stephen Helba Product Manager: Scott J. Sambucci Development Editor: Kate Linsner Production Manager: Pat Tonneman Production Editor: Rex Davidson

Design Coordinator: Karrie Converse-Jones

Cover Art: Painting by Sigmund Arseth, Artist and Teacher, Valdres, Norway

This book was set in Times Roman by **TECHBOOKS** and was printed and bound by Courier Kendallville, Inc. The cover was printed by Phoenix Color Corp.

Pearson Education Ltd., London

Pearson Education Australia Pty. Limited, Sydney

Pearson Education Singapore Pte. Ltd.

Pearson Education North Asia Ltd., Hong Kong

Pearson Education Canada, Ltd., Toronto

Pearson Educación de Mexico, S.A. de C.V.

Pearson Education—Japan, Tokyo

Pearson Education Malaysia Pte. Ltd.

Pearson Education, Upper Saddle River, New Jersey

Copyright © 2002, 1999, 1996, 1992, 1987, 1982, 1978, 1972 by Pearson Education, Inc., Upper Saddle River, New Jersey 07458.

All rights reserved. Printed in the United States of America. This publication is protected by Copyright and permission should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. For information regarding permission(s), write to: Rights and Permissions Department.



10 9 8 7 6 5 4 3 2 ISBN: 0-13-028483-1

## SIGNIFICANT EQUATIONS

- **1 Semiconductor Diodes** W = QV, 1 eV =  $1.6 \times 10^{-19}$  J,  $I_D = I_s(e^{kV_D/T_K} 1)$ ,  $R_{DC} = V_D/I_D$ ,  $r_d = \Delta V_d/\Delta I_d = 26$  mV/ $I_D$ ,  $r_{av} = \Delta V_d/\Delta I_d$ ,  $P_D = V_DI_D$ ,  $T_C = \Delta V_z/[V_z(T_1 T_0)] \times 100\%$
- **2 Diode Applications**  $V_{BE} = V_D = 0.7 \text{ V}$ ; half-wave:  $V_{dc} = 0.318 V_m$ ; full-wave:  $V_{dc} = 0.636 V_m$
- 3 Bipolar Junction Transistor  $I_E = I_C + I_B$ ,  $I_C = I_{C_{\rm majority}} + I_{CO_{\rm minority}}$ ,  $I_C \simeq I_E$ ,  $V_{BE} = 0.7 \text{ V}$ ,  $\alpha_{\rm dc} = I_C/I_E$ ,  $I_C = \alpha I_E + I_{CBO}$ ,  $\alpha_{\rm ac} = \Delta I_C/\Delta I_E$ ,  $I_{CEO} = I_{CBO}/(1-\alpha)$ ,  $\beta_{\rm dc} = I_C/I_B$ ,  $\beta_{\rm ac} = \Delta I_C/I_B$ ,  $\alpha = \beta/(\beta+1)$ ,  $\beta = \alpha/(1-\alpha)$ ,  $I_C = \beta I_B$ ,  $I_E = (\beta+1)I_B$ ,  $P_{C_{\rm marg}} = V_{CE}I_C$
- 4 DC Biasing BJTs In general:  $V_{BE} = 0.7 \text{ V}$ ,  $I_C \simeq I_E$ ,  $I_C = \beta I_B$ ; fixed-bias:  $I_B = (V_{CC} V_{BE})/R_B$ ,  $V_{CE} = V_{CC} I_{C}R_{C}$ ,  $I_{C_{sat}} = V_{CC}/R_{C}$ ; emitter-stabilized:  $I_B = (V_{CC} V_{BE})/(R_B + (\beta + 1)R_E)$ ,  $R_i = (\beta + 1)R_E$ ,  $V_{CE} = V_{CC} I_{C}(R_C + R_E)$ ,  $I_{C_{sat}} = V_{CC}/(R_C + R_E)$ ; voltage-divider: exact:  $R_{Th} = R_1 || R_2$ ,  $E_{Th} = R_2 V_{CC}/(R_1 + R_2)$ ,  $I_B = (E_{Th} V_{BE})/(R_{Th} + (\beta + 1)R_E)$ ,  $V_{CE} = V_{CC} I_C(R_C + R_E)$ , approximate:  $V_B = R_2 V_{CC}/(R_1 + R_2)$ ,  $\beta R_E \ge 10R_2$ ,  $V_E = V_B V_{BE}$ ,  $I_C \simeq I_E = V_E/R_E$ ; voltage-feedback:  $I_B = (V_{CC} V_{BE})/[R_B + \beta(R_C + R_E)]$ ; common-base:  $I_B = (V_{EE} V_{BE})/R_E$ ; switching transistors:  $t_{on} = t_r + t_d$ ,  $t_{off} = t_s + t_f$ ; stability:  $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ ; fixed-bias:  $S(I_{CO}) = \beta + 1$ ; emitter-bias:  $S(I_{CO}) = (\beta + 1)(1 + R_B/R_E)/(1 + \beta + R_B/R_E)$ ; voltage-divider:  $S(I_{CO}) = (\beta + 1)(1 + R_{Th}/R_E)/(1 + \beta + R_{Th}/R_E)$ ; feedback-bias:  $S(V_{BE}) = -\beta/[R_B + (\beta + 1)R_E]$ ; voltage-divider:  $S(V_{BE}) = \Delta I_C/\Delta V_{BE}$ ; fixed-bias:  $S(V_{BE}) = -\beta/[R_B + (\beta + 1)R_E]$ ; voltage-divider:  $S(V_{BE}) = -\beta/[R_{Th} + (\beta + 1)R_E]$ ; feedback bias:  $S(V_{BE}) = -\beta/(R_B + (\beta + 1)R_C)$ ,  $S(\beta) = \Delta I_C/\Delta \beta$ ; fixed-bias:  $S(\beta) = I_{C_1}(1 + R_B/R_E)/[\beta_1(1 + \beta_2 + R_B/R_E)]$ ; voltage-divider:  $S(\beta) = I_{C_1}(1 + R_{Th}/R_E)$ ; feedback-bias:  $S(\beta) = I_{C_1}(1 + R_B/R_E)/[\beta_1(1 + \beta_2 + R_B/R_E)]$ ; voltage-divider:  $S(\beta) = I_{C_1}(1 + R_{Th}/R_E)$ ; feedback-bias:  $S(\beta) = I_{C_1}(1 + R_B/R_E)$ .
- **5 Field-Effect Transistors**  $I_G = 0 \text{ A}, I_D = I_{DSS}(1 V_{GS}/V_P)^2, I_D = I_S, V_{GS} = V_P(1 \sqrt{I_D/I_{DSS}}), I_D = I_{DSS}/4$  (if  $V_{GS} = V_P/2$ ),  $I_D = I_{DSS}/2$  (if  $V_{GS} = 0.3V_P$ ),  $P_D = V_{DS}I_D$ ,  $I_D = k(V_{GS} V_T)^2$
- **6 FET Biasing** Fixed-bias:  $V_{GS} = -V_{GG}$ ,  $V_{DS} = V_{DD} I_D R_D$ ; self-bias:  $V_{GS} = -I_D R_S$ ,  $V_{DS} = V_{DD} I_D (R_S + R_D)$ ,  $V_S = I_D R_S$ ; voltage-divider:  $V_G = R_2 V_{DD} / (R_1 + R_2)$ ,  $V_{GS} = V_G I_D R_S$ ,  $V_{DS} = V_{DD} I_D (R_D + R_S)$ ; enhancement-type MOSFET:  $I_D = k(V_{GS} V_{GS(Th)})^2$ ,  $k = I_{D(on)} / (V_{GS(on)} V_{GS(Th)})^2$ ; feedback bias:  $V_{DS} = V_{GS}$ ,  $V_{GS} = V_{DD} I_D R_D$ ; voltage-divider:  $V_G = R_2 V_{DD} / (R_1 + R_2)$ ,  $V_{GS} = V_G I_D R_S$ ; universal curve:  $m = |V_P| / I_{DSS} R_S$ ,  $M = m \times V_G / |V_P|$ ,  $V_G = R_2 V_{DD} / (R_1 + R_2)$
- 7 BJT Transistor Modeling  $Z_i = V_i/I_i$ ,  $I_i = (V_s V_i)/R_{\text{sense}}$ ,  $I_o = (V_s V_o)/R_{\text{sense}}$ ,  $Z_o = V_o/I_o$ ,  $A_v = V_o/V_i$ ,  $A_{v_s} = Z_i A_{v_{NL}}/(Z_i + R_s)$ ,  $A_i = -A_v Z_i/R_L$ ,  $r_e = 26 \text{ mV}/I_E$ ; common-base:  $Z_i = r_e$ ,  $Z_o \simeq \infty \Omega$ ,  $A_v \simeq R_L/r_e$ ,  $A_i \simeq -1$ ; common-emitter:  $Z_i = \beta r_e$ ,  $Z_o = r_o$ ,  $A_v = -R_L/r_e$ ,  $A_i \simeq \beta$ ,  $A_i = \beta r_e$ ,  $A_i = \beta r_e$ ,  $A_i = \beta r_e$ ,  $A_i = -\alpha$ .

- **8 BJT Small-Signal Analysis** Common-emitter:  $A_v = -R_C/r_e$ ,  $Z_i = R_B \| \beta r_e$ ,  $Z_o = R_C$ ,  $A_i \simeq \beta$ ; voltage-divider:  $R' = R_1 \| R_2$ ,  $A_v = -R_C/r_e$ ,  $Z_i = R' \| \beta r_e$ ,  $Z_o = R_C$ ; emitter-bias:  $Z_b = \beta(r_e + R_E) \simeq \beta R_E$ ,  $A_v = -\beta R_C/Z_b = -R_C/(r_e + R_E) \simeq -R_C/R_E$ ; emitter-follower:  $Z_b \simeq \beta(r_e + R_E)$ ,  $A_v \simeq 1$ ,  $Z_o \simeq r_e$ ; common-base:  $A_v \simeq R_C/r_e$ ,  $Z_i = R_E \| r_e$ ,  $Z_o = R_C$ ; collector feedback:  $A_v = -R_C/r_e$ ,  $Z_i = \beta r_e \| R_F/|A_v|$ ,  $Z_o \simeq R_C \| R_F$ ; collector dc feedback:  $A_v = -(R_{F_2} \| R_C)/r_e$ ,  $Z_i = R_{F_1} \| \beta r_e$ ,  $Z_o = R_C \| R_{F_2}$ ; hybrid parameters:  $A_i = h_f/(1 + h_o R_L)$ ,  $A_v = -h_f R_L/[h_i + (h_i h_o h_f h_r)R_L]$ ,  $Z_i = h_i h_f h_r R_L/(1 + h_o R_L)$ ,  $Z_o = 1/[h_o (h_f h_r/(h_i + R_s))]$
- **9 FET Small-Signal Analysis**  $g_m = g_{mo}(1 V_{GS}/V_P)$ ,  $g_{mo} = 2I_{DSS}/|V_P|$ ; basic configuration:  $A_v = -g_m R_D$ ; unbypassed source resistance:  $A_v = -g_m R_D/(1 + g_m R_S)$ ; source follower:  $A_v = g_m R_S/(1 + g_m R_S)$ ; common gate:  $A_v = g_m (R_D || r_d)$
- 10 Systems Approach—Effects of  $R_S$  and  $R_L$  BJT:  $A_v = R_L A_{v_{NL}}/(R_L + R_o)$ ,  $A_i = -A_v Z_i/R_L$ ,  $V_i = R_i V_s/(R_i + R_s)$ ; fixed-bias:  $A_v = -(R_C \| R_L)/r_e$ ,  $A_{v_s} = Z_i A_v/(Z_i + R_s)$ ,  $Z_i = \beta r_e$ ,  $Z_o = R_C$ ; voltage-divider:  $A_v = -(R_C \| R_L)/r_e$ ,  $A_{v_s} = Z_i A_v/(Z_i + R_s)$ ,  $Z_i \approx R_1 \| R_2 \| \beta r_e$ ,  $Z_o = R_C$ ; emitter-bias:  $A_v = -(R_C \| R_L)/R_E$ ,  $A_{v_s} = Z_i A_v/(Z_i + R_s)$ ,  $Z_i \approx R_B \| \beta R_E$ ,  $Z_o = R_C$ ; collector-feedback:  $A_v = -(R_C \| R_L)/r_e$ ,  $A_{v_s} = Z_i A_v/(Z_i + R_s)$ ,  $Z_i = \beta r_e \| R_F/|A_v|$ ,  $Z_o \approx R_C \| R_F$ ; emitter-follower:  $R_E' = R_E \| R_L$ ,  $A_v = R_E'/(R_E' + r_e)$ ,  $A_{v_s} = R_E'/(R_E' + R_s/\beta + r_e)$ ,  $Z_i = R_B \| \beta (r_e + R_E')$ ,  $Z_o = R_E \| (R_s/\beta + r_e)$ ; common-base:  $A_v \approx (R_C \| R_L)/r_e$ ,  $A_i \approx 1$ ,  $Z_i \approx r_e$ ,  $Z_o = R_C$ ; FET: bypassed  $R_S$ :  $A_v = -g_m(R_D \| R_L)$ ,  $Z_i = R_G$ ,  $Z_o = R_D$ ; unbypassed  $R_S$ :  $A_v = -g_m(R_D \| R_L)/(1 + g_m R_S)$ ,  $Z_i = R_G$ ,  $Z_o = R_D$ ; source-follower:  $A_v = g_m(R_S \| R_L)/[1 + g_m(R_S \| R_L)]$ ,  $Z_i = R_G$ ,  $Z_o = R_S \| r_d \| 1/g_m$ ; common gate:  $A_v = g_m(R_D \| R_L)$ ,  $Z_i = R_S \| 1/g_m$ ,  $Z_O = R_O$ ; cascaded:  $A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdot \cdot \cdot A_{v_n}$ ,  $A_{i_T} = \pm A_{v_T} Z_{i_T}/R_L$
- 11 BJT and JFET Frequency Response  $\log_e a = 2.3 \log_{10} a, \log_{10} 1 = 0, \log_{10} a/b = \log_{10} a \log_{10} b, \log_{10} ab = \log_{10} a + \log_{10} b, G_{\text{dB}} = 10 \log_{10} P_2/P_1, G_{\text{dBm}} = 10 \log_{10} P_2/1 \text{ mW}|_{600\Omega}, G_{\text{dB}} = 20 \log_{10} V_2/V_1, G_v = G_{v_1} + G_{v_2} + G_{v_3} + \dots + G_{v_n}, P_{o_{\text{HPF}}} = 0.5P_{o_{\text{mid}}}, \text{BW} = f_1 f_2; \text{low frequency (BJT):} \\ f_{L_s} = 1/2\pi(R_s + R_i)C_s, f_{L_c} = 1/2\pi(R_o + R_L)C_c, f_{L_c} = 1/2\pi R_e C_E, R_e = R_E \| (R_s'/\beta + r_e), R_s' = R_s \| R_1 \| R_2, \text{ FET:} \\ f_{L_G} = 1/2\pi(R_{\text{sig}} + R_i)C_G, f_{L_c} = 1/2\pi R_o C_c, f_{L_s} = 1/2\pi R_{\text{eq}} C_s, R_{eq} = R_s \| 1/g_m (r_d \approx \infty \Omega); \text{ Miller effect: } C_{M_i} = (1 A_v)C_f, C_{M_o} = (1 1/A_v)C_f; \text{ high frequency (BJT): } f_{H_i} = 1/2\pi R_{\text{Th}_1}C_i, R_{\text{Th}_1} = R_s \| R_1 \| R_2 \| R_i, C_i = C_{W_i} + C_{be} + C_{M_i}, f_{H_o} = 1/2\pi R_{\text{Th}_2}C_o, R_{\text{Th}_2} = R_C \| R_L \| r_o, C_o = C_{W_o} + C_{ce} + C_{M_o}, f_{\beta} \approx 1/2\pi \beta_{\text{mid}} r_e (C_{be} + C_{bc}), f_T = \beta_{\text{mid}} f_{\beta}; \text{ FET:} \\ f_{H_i} = 1/2\pi R_{\text{Th}_1}C_i, R_{\text{Th}_1} = R_{\text{sig}} \| R_G, C_i = C_{W_i} + C_{gs} + C_{M_i}, f_{H_o} = 1/2\pi R_{\text{Th}_2}C_o, R_{\text{Th}_2} = R_D \| R_L \| r_d, C_o = C_{W_o} + C_{ds} + C_{M_o}; \\ multistage: f_1' = f_1/\sqrt{2^{1/n} 1}, f_2' = (\sqrt{2^{1/n} 1})f_2; \text{ square-wave testing: } f_{H_i} = 0.35/t_r, \% \text{ tilt } = [(V V')/V] \times 100\%, \\ f_{L_c} = (P/\pi)f_s, P = (V V')/V$
- **12 Compound Configurations** Differential voltage gain:  $A_v = \beta R_C/2r_i$ ; common-mode voltage gain:  $\beta R_C/[r_i + 2(\beta + 1)R_E]$
- **13 Operational Amplifiers** CMRR =  $A_d/A_c$ ; CMRR(log) =  $20 \log_{10}(A_d/A_c)$ ; constant-gain multiplier:  $V_o/V_1 = -R_f/R_1$ ; noninverting amplifier:  $V_o/V_1 = 1 + R_f/R_1$ ; unity follower:  $V_o = V_1$ ; summing amplifier:  $V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$ ; integrator:  $v_o(t) = -(1/R_1C_1)\int v_1dt$
- **14 Op-Amp Applications** Constant-gain multiplier:  $A = -R_f/R_1$ ; noninverting:  $A = 1 + R_f/R_1$ : voltage summing:  $V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$ ; high-pass active filter:  $f_{oL} = 1/2\pi R_1 C_1$ ; low-pass active filter:  $f_{oH} = 1/2\pi R_1 C_1$

#### 15 Power Amplifiers

Power in:  $P_i = V_{CC}I_{CQ}$ 

power out:  $P_o = V_{CE}I_C = I_C^2 R_C = V_{CE}^2 / R_C \text{ rms}$ 

 $= V_{CE}I_C/2 = (I_C^2/2)R_C = V_{CE}^2/(2R_C)$  peak

 $= V_{CE}I_C/8 = (I_C^2/8)R_C = V_{CE}^2/(8R_C)$  peak-to-peak

efficiency:  $\%\eta = (P_o/P_i) \times 100\%$ 

maximum efficiency: Class A, series-fed = 25%

Class A, transformer-coupled = 50%

Class B, push-pull = 78.5%

transformer relations:  $V_2/V_1 = N_2/N_1 = I_1/I_2$ ,  $R_2 = (N_2/N_1)^2 R_1$ ; power output:  $P_o = [(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})]/8$ ; class B power amplifier:  $P_i = V_{CC}[(2/\pi)I_{peak}]$ ;  $P_o = V_L^2(peak)/(2R_L)$ ; %  $\eta = (\pi/4)[V_L(peak)/V_{CC}] \times 100\%$ ;  $P_Q = P_{2Q}/2 = (P_i - P_o)/2$ ; maximum  $P_o = V_{CC}^2/2R_L$ ; maximum  $P_i = 2V_{CC}^2/\pi R_L$ ; maximum  $P_{2Q} = 2V_{CC}^2/\pi^2 R_L$ ; % total harmonic distortion (% THD) =  $\sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$ ; heat-sink:  $T_j = P_D\theta_{JA} + T_A$ ,  $\theta_{JA} = 40$ °C/W (free air);  $P_D = (T_J - T_A)/(\Theta_{JC} + \Theta_{CS} + \Theta_{SA})$ 

- **16 Linear-Digital ICs** Ladder network:  $V_o = [(D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + \dots + D_n \times 2^n)/2^n]V_{\text{ref}};$  555 oscillator:  $f = 1.44(R_A + 2R_B)C$ ; 555 monostable:  $T_{\text{high}} = 1.1R_AC$ ; VCO:  $f_o = (2/R_1C_1)[(V^+ V_C)/V^+];$  phase-locked loop (PLL):  $f_o = 0.3/R_1C_1$ ,  $f_L = \pm 8f_o/V$ ,  $f_C = \pm (1/2\pi)\sqrt{2\pi f_L/(3.6 \times 10^3)C_2}$
- 17 Feedback and Oscillator Circuits  $A_f = A/(1 + \beta A)$ ; series feedback;  $Z_{if} = Z_i(1 + \beta A)$ ; shunt feedback:  $Z_{if} = Z_i/(1 + \beta A)$ ; voltage feedback:  $Z_{of} = Z_o/(1 + \beta A)$ ; current feedback:  $Z_{of} = Z_o(1 + \beta A)$ ; gain stability:  $dA_f/A_f = 1/(|1 + \beta A|)(dA/A)$ ; oscillator;  $\beta A = 1$ ; phase shift:  $f = 1/2\pi RC\sqrt{6}$ ,  $\beta = 1/29$ , A > 29; FET phase shift:  $|A| = g_m R_L$ ,  $R_L = R_D r_d/(R_D + r_d)$ ; transistor phase shift:  $f = (1/2\pi RC)[1/\sqrt{6 + 4(R_C/R)}]$ ,  $h_{fe} > 23 + 29(R_C/R) + 4(R/R_C)$ ; Wien bridge:  $R_3/R_4 = R_1/R_2 + C_2/C_1$ ,  $f_o = 1/2\pi\sqrt{R_1C_1R_2C_2}$ ; tuned:  $f_o = 1/2\pi\sqrt{LC_{eq}}$ ,  $C_{eq} = C_1C_2/(C_1 + C_2)$ , Hartley:  $L_{eq} = L_1 + L_2 + 2M$ ,  $f_o = 1/2\pi\sqrt{Lc_{eq}C}$
- 18 Power Supplies (Voltage Regulators) Filters:  $r = V_r(\text{rms})/V_{\text{dc}} \times 100\%$ , V.R. =  $(V_{NL} V_{FL})/V_{FL} \times 100\%$ ,  $V_{\text{dc}} = V_m V_r$  (p-p)/2,  $V_r(\text{rms}) = V_r$  (p-p)/2 $\sqrt{3}$ ,  $V_r(\text{rms}) \simeq (I_{\text{dc}}/4\sqrt{3})(V_{\text{dc}}/V_m)$ ; full-wave, light load  $V_r(\text{rms}) = 2.4I_{\text{dc}}/C$ ,  $V_{\text{dc}} = V_m 4.17I_{\text{dc}}/C$ ,  $r = (2.4I_{\text{dc}}CV_{\text{dc}}) \times 100\% = 2.4/R_LC \times 100\%$ ,  $I_{\text{peak}} = T/T_1 \times I_{\text{dc}}$ ; RC filter:  $V_{\text{dc}}' = R_L V_{\text{dc}}/C$  ( $R + R_L$ ),  $X_C = 2.653/C$  (half-wave),  $X_C = 1.326/C$  (Full-wave),  $V_r'(\text{rms}) = (X_C/\sqrt{R^2 + X_C^2})$ ; regulators:  $IR = (I_{NL} I_{FL})/I_{FL} \times 100\%$ ,  $V_L = V_Z(1 + R_1/R_2)$ ,  $V_o = V_{\text{ref}}(1 + R_2/R_1) + I_{\text{adj}}R_2$
- 19 Other Two-Terminal Devices Variation diode:  $C_T = C(0)/(1 + |V_r/V_T|)^n$ ,  $T_{C_c} = (\Delta C/C_o(T_1 T_0)) \times 100\%$ ; photodiode:  $W = M_f$ ,  $\lambda = v/f$ ,  $1 \text{ Im} = 1.496 \times 10^{-10} \text{ W}$
- **20 pnpn and Other Devices** UJT:  $R_{BB} = (R_{B_1} + R_{B_2})|_{I_E = 0}$ ,  $V_{R_{B_1}} = \eta V_{BB}|_{I_E = 0}$ ,  $\eta = R_{B_1}/(R_{B_1} + R_{B_2})|_{I_E = 0}$ ,  $V_P = \eta V_{BB} + V_D$ ; phototransistor:  $I_C \simeq h_{fe}I_{\lambda}$ ; PUT:  $\eta = R_{B_1}/(R_{B_1} + R_{B_2})$ ,  $V_P = \eta V_{BB} + V_D$

#### Dedicated to

ELSE MARIE; ALISON, MARK, KELCY, and MORGAN; ERIC, RACHEL, and SAMANTHA; STACEY, JONATHAN, and BRITT; JOHANNA and to

KATRIN; KIRA, TOMMY, JUSTIN, and TYLER; LARREN, PATTY, BRENDAN, and OWEN

# **Preface**

In this edition we have written additional practical examples and summaries at the end of each chapter, and have expanded coverage of computer software. The chapter on IC construction was deleted and replaced with a well-written description of the process that first appeared in *Smithsonian Magazine*. It has some stunning photographs and content that is excellent for the new students of this rapidly changing field.

Over the years we have learned that improved readability can be obtained through the general appearance of the text, so we are committed to the format you find in this and recent editions of the text. We hope you agree that it makes the text material appear "friendlier" to the broad range of students using the text. As in the past, we continue to be committed to the strong pedagogical sense of the text, accuracy, completeness, and a broad range of ancillary materials that support the educational process.

#### **PEDAGOGY**

Reviewers and current users appear to be quite satisfied with the manner in which the content lends itself to a typical course syllabus. The improved pedagogy of the last two editions seems to support the instructor's lecture and helps students build the foundation necessary for future studies. The number of examples continues to grow, and isolated boldface statements continue to identify important concepts and conclusions. Color continues to be employed in a manner that helps define important regions of characteristics, or identifies important regions or parameters of a network. Icons at the top of the page, developed for each chapter of the text, facilitate referencing a particular area of text as quickly as possible. Problems, which have been developed for each section of the text, progress from the simple to the more complex. The title of each section is repeated in the problem section to identify the problems associated with a particular subject matter.

#### SYSTEMS APPROACH

There is no question that the growing development of packaged systems requires that the student become aware at the earliest opportunity of a "systems approach" to the design and analysis of electronic systems. Isolated no-load networks are first discussed in Chapters 8 and 9 to introduce the important parameters of any package and

develop the important equations for the configuration. The impact of a source or load impedance on the individual package is then defined in Chapter 10 on a general basis before examining specific networks. Finally, the impact of tying the individual packages together is examined in the same chapter to establish some understanding of the systems approach. The later chapters on op-amps and IC units further develop the concepts introduced in these early chapters.

#### **ACCURACY**

The goal of any educational publication is to be absolutely free of errors. There is nothing more distressing to a student than to find that he or she has suffered for hours over a simple printing error. In fact, after all the hours that go into preparing a manuscript and checking every word, number, or letter there is nothing more distressing to an author than to find that errors have crept into the publication. Based on past history and the effort put into this publication, we believe you will find the highest level of accuracy obtainable for a publication of this kind.

#### **SUMMARIES**

In response to current users, summaries are added at the end of each chapter, reviewing the salient concepts and conclusions. To emphasize specific words and phrases, boldface lettering is used in much the same manner as a student would use a highlighting marker. The list of equations appearing with each summary was limited to those an instructor realistically hopes the student will bring away from the course.

#### PRACTICAL EXAMPLES

While the text now has over 80 practical examples, over 40 were added to this edition and they appear in their own sections. They provide an understanding of the design process that is normally not available at this level. Practical considerations associated with using the electronic devices introduced in this text are discussed as experienced by professionals in the field. The level of coverage is well beyond the surface description of the operation of a particular product. Networks are reduced for clarity and equations are developed to explain why specific response levels are obtained. An effort was made to give some idea of the range of application for each device introduced. Too often the student believes that each electronic device serves a particular purpose, and that's it. In general, the authors are pleased with the results of this demanding effort and invite your comments and suggestions so that the content can be improved upon in the future.

#### TRANSISTOR MODELING

BJT transistor modeling is an area that can be approached in a variety of ways. Some institutions employ the  $r_e$  model exclusively, while others lean toward the hybrid approach or to a combination of the two. This edition will emphasize the  $r_e$  model with sufficient coverage of the hybrid model to permit a comparison between the results obtained with each approach. An entire chapter (Chapter 7) has been devoted to the introduction of the models to ensure a clear, correct understanding of each and the relationships that exist between the two.

#### **EQUATION DEVELOPMENT**

For years the development of the equations for small-signal BJT and JFET networks avoided the impact of the output parameter  $r_o$ . In addition, results were often provided with no idea how they were obtained. Further, approximate equations were provided with no idea what conditions had to be satisfied to permit use of the equations. For these reasons, and probably others, the details of each derivation are provided in this text. The effect of  $r_o$  was separated for each development to first permit a less complex development. The effect of  $r_o$  was then demonstrated and the conditions under which the effect of  $r_o$  can be ignored were introduced. In most cases, the derivations are unique to any publication of this type. They were the result of extensive hours searching for the best path for the analysis. However, the result is a complete development of each equation that we hope will remove any doubt as to their validity.

#### **COMPUTER SOFTWARE**

In recent editions, both PSpice and Electronics Workbench examples were included. For this edition Mathcad was added to demonstrate the versatility of the package for an area such as electronics. Not only can it be used to quickly solve simultaneous equations, but also long series of calculations can be placed in storage for retrieval when a particular configuration is encountered. Numerous examples appear throughout the text, and we believe the student and instructor will find them quite interesting. The detailed coverage of PSpice was expanded slightly, but there is a larger expansion of the coverage of Electronics Workbench due to its growing popularity. For all the software packages there is no requirement that the student become versed in their use to proceed through the text. Although sufficient detail is provided for each application to permit a student to apply each to a variety of configurations, there is no requirement that the packages actually be used.

#### TROUBLESHOOTING

Troubleshooting is undoubtedly one of the most difficult subjects to discuss and develop in an introductory text. A student is just becoming familiar with the characteristics and operation of a device and now is asked to find an answer to an unexpected result. It is an art that has to develop with experience and exposure. The content of this text is essentially a review of situations that frequently occur in the laboratory environment. Some general hints as to how to isolate a problem are introduced along with a list of typical causes.

#### **ANCILLARIES**

The range of ancillary material is quite extensive, including a laboratory manual to which new experiments have been added. There is also an instructor's resource manual, which contains solutions to the in-text problems and the laboratory experiments as well as a test item file. PowerPoint<sup>®</sup> transparencies and a Prentice Hall Test Manager are also available.

The CD-ROM included with every copy of the book contains Electronics Workbench Version 5 and Multisim circuit files and CircuitMaker Student Version Software and circuit files. Circuits appearing on the CD-ROM are designated in the text by a special icon next to the selected illustration.



Preface vii

Additional support for the student can be found at www.prenhall.com/boylestad in the form of an online student study guide. CourseCompass and Blackboard complete the supplements package.

#### **USE OF THE TEXT**

In general the text is divided into two main components: the dc analysis and the ac or frequency response. For some schools the dc section is sufficient for a one-semester introductory sequence, while for others the entire text may be covered in one semester by picking and choosing specific topics. In any event, the text is one that "builds" from the earlier chapters. Superfluous material is relegated to the later chapters to avoid excessive content on a particular subject early in the development stage. For each device the text covers a majority of the important configurations and applications—the text is very complete! By choosing specific examples and applications the instructor can reduce the content of a course without losing the progressive building characteristics of the text. Then again, if an instructor feels that a specific area is particularly important, the detail is provided for a more extensive review.

> Robert L. Boylestad Louis Nashelsky

# Acknowledgments

Our sincerest appreciation must be extended to the instructors who have used the text and sent in comments, corrections, and suggestions. We also want to thank Rex Davidson, Production Editor at Prentice Hall, for keeping together the many detailed aspects of production, and Maggie Diehl for the copyediting. Our sincerest thanks to Scott Sambucci, Product Manager, and Kate Linsner, Development Editor, at Prentice Hall for their editorial support of the eighth edition of this text.

For the new Appendix A, "Making the Chips that Run the World," we thank Jake Page (author) and Kay Chernush (photographer) for their article from Smithsonian Magazine.

For the cover art, we thank Sigmund Arseth.

We wish to thank those individuals who have shared their suggestions and evaluations of this text throughout its many editions. The comments from these individuals have enabled us to present Electronic Devices and Circuit Theory in this eighth edition:

Ernest Lee Abbott Phillip D. Anderson

Napa College

Al Anthony

Muskegon Community College EG&G VACTEC Inc.

A. Duane Bailey

Joe Baker

Southern Alberta Institute of Technology University of Southern California

Jerrold Barrosse

Pennsylvania State University

**Ambrose Barry** Arthur Birch University of North Carolina Hartford State Technical College

Scott Bisland

**SEMATECH** The Perkin-Elmer Corporation

**Edward Bloch** Gary C. Bocksch

Charles S. Mott Community College Bunker Hill Community College

Jeffrey Bowe Alfred D. Buerosse

Waukesha County Technical College

Lila Caggiano

MicroSim Corporation Hofstra University

Mauro J. Caputi Robert Casiano

International Rectifier Corporation

Nathan Chao Alan H. Czarapata Mohammad Dabbas Queensborough Community College, CUNY Montgomery College

John Darlington

ITT Technical Institute Humber College

Lucius B. Day Mike Durren Metropolitan State College Lake Michigan College

Dr. Stephen Evanson Bradford University George Fredericks Northeast State Technical Community College F. D. Fuller Humber College Phil Golden DeVry Institute of Technology Joseph Grabinski Hartford State Technical College Thomas K. Grady Western Washington University Mohamad S. Haj-Mohamadi North Carolina A & T State University William Hill ITT Technical Institute Albert L. Ickstadt San Diego Mesa College Jeng-Nan Juang Mercer University Karen Karger Tektronix Inc. Kenneth E. Kent DeKalb Technical Institute Donald E. King ITT Technical Institute Charles Lewis APPLIED MATERIALS, INC. Donna Liverman Texas Instruments Inc. William Mack Harrisburg Area Community College Robert Martin Northern Virginia Community College George T. Mason Indiana Vocational Technical College William Maxwell Nashville State Technical Institute Abraham Michelen Hudson Valley Community College John MacDougall University of Western Ontario Donald E. McMillan Southwest State University Thomas E. Newman L. H. Bates Vocational-Technical Institute **Byron Paul** Bismarck State College Dr. Robert Payne University of Glamorgan Dr. Robert A. Powell Oakland Community College E. F. Rockafellow Southern-Alberta Institute of Technology Saeed A. Shaikh Miami-Dade Community College Dr. Noel Shammas School of Engineering Ken Simpson Stark State College of Technology Jerry Sitbon Queensborough Community College Eric Sung Computronics Technology Inc. Donald P. Szymanski Owens Technical College Parker M. Tabor Greenville Technical College Peter Tampas Michigan Technological University Chuck Tinney University of Utah Katherine L. Usik Mohawk College of Applied Art & Technology Domingo Uy Hampton University Richard J. Walters DeVry Institute of Technology Larry J. Wheeler PSE&G Nuclear Julian Wilson Southern College of Technology Syd R. Wilson Motorola Inc. **Jean Younes** ITT Technical Institute Charles E. Yunghans Western Washington University Ulrich E. Zeisler Salt Lake Community College

We thank the following individuals for assisting in the review process for this eighth edition:

Joseph Booker
Charles F. Bunting
Mauro J. Caputi
Kevin Ford
David Krispinsky
William Mack
John Sherrick

DeVry Institute of Technology
Old Dominion University
Hofstra University
Alvin Community College
Rochester Institute of Technology
Harrisburg Area Community College
Rochester Institute of Technology

# **Contents**

	PREFACE	$\mathbf{V}$	
	ACKNOWLEDGMENTS	ix	
1	SEMICONDUCTOR DIODES	1	
1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 1.10 1.11 1.12 1.13 1.14 1.15 1.16 1.17	Introduction 1 Ideal Diode 1 Semiconductor Materials 3 Energy Levels 6 Extrinsic Materials—n- and p-Type 7 Semiconductor Diode 10 Mathcad 17 Resistance Levels 20 Diode Equivalent Circuits 26 Diode Specification Sheets 29 Transition and Diffusion Capacitance 33 Reverse Recovery Time 34 Semiconductor Diode Notation 34 Diode Testing 35 Zener Diodes 37 Light-Emitting Diodes (LEDs) 40 Diode Arrays—Integrated Circuits 45 Summary 46 Computer Analysis 47		
2	DIODE APPLICATIONS	55	
2.1 2.2 2.3	Introduction 55 Load-Line Analysis 56 Diode Approximations 62		

2.8 2.9 2.10 2.11 2.12 2.13 2.14 2.15	Full-Wave Rectification 77 Clippers 81 Clampers 88 Zener Diodes 92 Voltage-Multiplier Circuits 98 Practical Applications 100 Summary 112 Computer Analysis 113	
3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9 3.10 3.11 3.12 3.13	BIPOLAR JUNCTION TRANSISTORS  Introduction 131 Transistor Construction 132 Transistor Operation 132 Common-Base Configuration 134 Transistor Amplifying Action 138 Common-Emitter Configuration 139 Common-Collector Configuration 146 Limits of Operation 147 Transistor Specification Sheet 149 Transistor Testing 153 Transistor Casing and Terminal Identification 155 Summary 156 Computer Analysis 158	131
4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 4.10 4.11 4.12 4.13 4.14 4.15	DC BIASING—BJTs  Introduction 163 Operating Point 164 Fixed-Bias Circuit 166 Emitter-Stabilized Bias Circuit 173 Voltage-Divider Bias 177 DC Bias with Voltage Feedback 186 Miscellaneous Bias Configurations 189 Design Operations 195 Transistor Switching Networks 201 Troubleshooting Techniques 206 PNP Transistors 209 Bias Stabilization 210 Practical Applications 220 Summary 228 Computer Analysis 231	163

Series Diode Configurations with DC Inputs 64 Parallel and Series–Parallel Configurations 69

Sinusoidal Inputs; Half-Wave Rectification 74

AND/OR Gates 72

2.4 2.5 2.6

2.7

xii

5	FIELD-EFFECT TRANSISTORS	245
5.1 5.2 5.3 5.4 5.5 5.6 5.7 5.8 5.9 5.10 5.11 5.12 5.13	Introduction 211 Construction and Characteristics of JFETs 246 Transfer Characteristics 253 Specification Sheets (JFETs) 259 Instrumentation 260 Important Relationships 262 Depletion-Type MOSFET 265 Enhancement-Type MOSFET 268 MOSFET Handling 276 VMOS 277 CMOS 278 Summary Table 280 Summary 281 Computer Analysis 282	
6	FET BIASING	289
6.1 6.2 6.3 6.4 6.5 6.6 6.7 6.8 6.9 6.10 6.11 6.12 6.13 6.14	Introduction 289 Fixed-Bias Configuration 290 Self-Bias Configuration 294 Voltage-Divider Biasing 301 Depletion-Type MOSFETs 307 Enhancement-Type MOSFETs 311 Summary Table 317 Combination Networks 319 Design 322 Troubleshooting 324 P-Channel FETs 325 Universal JFET Bias Curve 328 Practical Applications 331 Summary 343 Computer Analysis 344	
7	BJT TRANSISTOR MODELING	355
7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8	Introduction 355 Amplification in the AC Domain 355 BJT Transistor Modeling 356 The Important Parameters: $Z_i$ , $Z_o$ , $A_v$ , $A_i$ 358 The $r_e$ Transistor Model 364 The Hybrid Equivalent Model 371 Graphical Determination of the $h$ -Parameters 377 Variations of Transistor Parameters 381	

Contents xiii

8	BJT SMALL-SIGNAL ANALYSIS	389
8.1	Introduction 389	303
8.2	Common-Emitter Fixed-Bias Configuration 389	
8.3 8.4	Voltage-Divider Bias 393	
8.5	CE Emitter-Bias Configuration 396 Emitter-Follower Configuration 404	
8.6	Common-Base Configuration 409	
8.7	Collector Feedback Configuration 411	
8.8 8.9	Collector DC Feedback Configuration 417	
8.10	Approximate Hybrid Equivalent Circuit 420 Complete Hybrid Equivalent Model 426	
8.11	Summary Table 433	
8.12	Troubleshooting 433	
8.13 8.14	Practical Applications 436 Summary 444	
8.15	Computer Analysis 446	
9	FET SMALL-SIGNAL ANALYSIS	461
9.1		461
9.1	Introduction 461 FET Small-Signal Model 462	
9.3	JFET Fixed-Bias Configuration 469	
9.4	JFET Self-Bias Configuration 472	
9.5	JFET Voltage-Divider Configuration 479	
9.6 9.7	JFET Source-Follower (Common-Drain) Configuration 480 JFET Common-Gate Configuration 483	
9.8	Depletion-Type MOSFETs 487	
9.9	Enhancement-Type MOSFETs 489	
9.10	E-MOSFET Drain-Feedback Configuration 490	
9.11 9.12	E-MOSFET Voltage-Divider Configuration 493	
9.13	Designing FET Amplifier Networks 494 Summary Table 497	
9.14	Troubleshooting 500	
9.15	Practical Applications 500	
9.16 9.17	Summary 510	
9.17	Computer Analysis 512	
1 (	SYSTEMS APPROACH—	
T	SYSTEMS APPROACH— EFFECTS OF $R_s$ AND $R_L$	525
10.1	Introduction 525	
10.2	Two-Port Systems 525	
10.3	Effect of a Load Impedance $(R_L)$ 527	
10.4 10.5	Effect of a Source Impedance $(R_s)$ 532	
10.5	Combined Effect of $R_s$ and $R_L$ 534 BJT CE Networks 536	
10.7	BJT Emitter-Follower Networks 542	