

Lynn Margaret Batten  
Reihaneh Safavi-Naini (Eds.)

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# Information Security and Privacy

11th Australasian Conference, ACISP 2006  
Melbourne, Australia, July 2006  
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# Preface

The 11th Australasian Conference on Information Security and Privacy (ACISP 2006) was held in Melbourne, 3–5 July, 2006. The conference was sponsored by Deakin University, the Research Network for a Secure Australia, and was organized in cooperation with the University of Wollongong. The conference brought together researchers, practitioners and a wide range of other users from academia, industries and government organizations.

The program included 35 papers covering important aspects of information security technologies. The papers were selected from 133 submissions through a two-stage anonymous review process. Each paper received at least three reviews by members of the Program Committee, and was then scrutinized by the whole committee during a two-week discussion. There were 19 papers eligible for the “best student paper” award. The award was given to Yang Cui from the University of Tokyo for the paper “Tag-KEM from Set Partial Domain One-Way Permutations.”

In addition to the regular papers the program also included three invited talks. Bart Preneel gave an invited talk entitled “Electronic Identity Cards: Threats and Opportunities.” Mike Burmester’s talk was “Towards Provable Security for Ubiquitous Applications.” The details of the third talk had not been finalized at the time of publication of these proceedings.

We wish to thank all the authors of submitted papers for providing the content for the conference; their high-quality submissions made the task of selecting a program very difficult. We are indebted to the diligence and enthusiasm of the Program Committee members in ensuring selection of the most deserving papers and to the external reviewers who helped in the refereeing process. We wish to thank our sponsors, Research Network for a Secure Australia, for their support of the main speakers and students as well as Springer for their continued support of ACISP. We further wish to thank Judy Chow, the conference secretary, for her many organizational skills and patience with the registration process, and our Technical Chair, Jeffrey Horton, for his continuous effort and meticulous attention to every detail, which made the task of the Program Co-chairs so much easier.

Without the help of all the above this conference would not have been a possibility.

July 2006

Lynn Batten  
Reihaneh Safavi-Naini



# ACISP 2006

July 3–5, 2006, Melbourne, Australia

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# Algebraic Attacks on Clock-Controlled Stream Ciphers

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**Abstract.** We present an algebraic attack approach to a family of irregularly clock-controlled bit-based linear feedback shift register systems. In the general set-up, we assume that the output bit of one shift register controls the clocking of other registers in the system and produces a family of equations relating the output bits to the internal state bits. We then apply this general theory to four specific stream ciphers: the (strengthened) stop-and-go generator, the alternating step generator, the self-decimated generator and the step1/step2 generator. In the case of the strengthened stop-and-go generator and of the self-decimated generator, we obtain the initial state of the registers in a significantly faster time than any other known attack. In the other two situations, we do better than or as well as all attacks but the correlation attack. In all cases, we demonstrate that the degree of a functional relationship between the registers can be bounded by two. Finally, we determine the effective key length of all four systems.

**Keywords:** clock control, stream cipher, linear feedback shift register, irregular clocking, algebraic attack.

## 1 Introduction

Algebraic attacks, in which the generation of equations assists in determining the initial state or the key-stream of a cipher, were first applied to block ciphers and public key cryptosystems by Courtois and Pieprzyk [8, 13]. Algebraic attacks have been effectively applied to linear feedback shift register (LFSR) based systems as demonstrated in [1, 2, 6, 9, 10, 11, 12]. Our interest in this paper is their application to a class of bit-based LFSRs, which has not yet been examined from this direction — the irregularly clocked LFSR systems. We show that algebraic attacks are effective against this class of stream ciphers and we provide improvements to currently known attacks. In particular, known attacks against the Beth-Piper [3] strengthened stop-and-go cipher depend on the generation of weight three polynomials which cannot be done efficiently. We present a fast attack that is independent of the weight of the polynomial used.

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Irregular clocking in LFSRs is used to enhance their complexity and consequent security. Zenner [27] has developed a general approach to attacking such ciphers by guessing at the clocking through a clock cycle and applies this approach to several ciphers including A5/1, the stop-and-go generator, the alternating step generator and the step1/step2 generator with varying levels of success. Molland [20] introduces a general approach for dealing with LFSR systems with two registers where one register controls the clocking of the other. This applies to the basic stop-and-go generator, LILI-128 and step1/step2 generator. To our knowledge, the only algebraic attack on such a cipher is that on LILI-128 in [12], but guessing the clock control is an integral part of the approach.

Clock-controlled ciphers assume the existence of an underlying clock that maintains a consistent set of basic time intervals against which a register and its output can be compared. A bit-based LFSR system can then be established in a number of ways. A register can be stepped in synchrony with the underlying clock; it may move more slowly than the underlying clock, taking more than one basic unit to shift the registers; but it can be assumed that it will never shift faster than the clock as otherwise we can adjust the basic clocking time to the step time of the register. Similarly, the output from a system of clock-controlled LFSRs can be synchronized with the clock time or can be slowed down or varied against the clock time. If a register shifts with the basic time interval, we refer to it as *regularly clocked*. If the output is delivered with the basic time interval, we refer to it as *regular output*.

We shall focus on four systems, which fall into the above types. The Beth-Piper strengthened stop-and-go generator uses two regularly clocked registers and one irregularly clocked register along with regular output. The alternating step generator has one regularly clocked register and two which are irregularly clocked. Again, the output is regular. In the self-decimated generator, the output is irregular while the sole register actually clocks regularly. The step1/step2 generator has two irregularly clocked LFSRs with irregular output.

In the next section, we introduce the notation standardized throughout the paper and present our generic approach to determining algebraic equations involving the initial state bits from bit-based clock-controlled ciphers in which a linear combination of bits from regularly clocked registers determines the clocking of the others. Our aim is to recover the initial state bits. We ignore key initialization schemes altogether and compute effective key length assuming that the key and initial state of the registers are one and the same. We therefore use the phrase *effective key length*, and make the assumption that for computational purposes eighty bit registers are safe from a brute force attack. In subsequent sections, we use the equations to find the initial states of the four ciphers mentioned above. In the case of the strengthened stop-and-go generator and of the self-decimated generator, we obtain the initial state of the registers in a significantly faster time than any other known attack. In the other two situations, we do better than or as well as all attacks but the correlation attack. In all cases, we demonstrate relationships between the registers indicating that a low degree multiple of the polynomials corresponding to irregularly clocked registers can



be bounded by two. Finally, we determine the effective key length of all four systems and present our computational results.

## 2 The General Set-Up

We consistently label registers  $A$ ,  $B$  and  $C$  with lengths  $l$ ,  $m$  and  $n$ . The  $i^{th}$  bit of register  $A$  at time  $t$  is denoted by  $A_i^t$  and so the output bit is  $A_l^t$ . Similarly for registers  $B$  and  $C$ . We use  $z^t$  to denote the output from the entire system at time  $t$ .  $M$  denotes the number of monomials occurring in a given system of equations. If this system is linear, the complexity of solving the system is in general about  $M^3$ ; if the system is sparse, this reduces to  $M^2$  [25]. If the system is quadratic, the complexity of using the linearisation methods in [12] is about  $\binom{M}{2}^3$ . In this paper, we make use of both linear algebra and Gröbner bases methods of solving equations. All computations are performed using the  $F_4$  algorithm in Magma 2.11 [19] on the SGI Origin 3000 using CPU at 600 MHz.

In setting up a general approach to acquiring an equation from a clock-controlled stream cipher of our type, we need to consider three things: first of all, which LFSR controls the clocking (we always use the letter  $A$  for this register), secondly, which bits of the controlling register are used to determine the clocking, and thirdly, the effect on the shift of the controlled register. Suppose that the  $i^{th}$  bit of  $A$  controls the clocking of  $B$  in such a way that if it is 0,  $B$  does not clock and if it is 1,  $B$  clocks  $j$  times. In this case, we can express the change to the  $k^{th}$  position of  $B$  as follows:

$$B_k^t = B_k^{t-1}(A_i^{t-1} \oplus 1) \oplus B_{k-j}^{t-1}A_i^{t-1}. \quad (1)$$

Of course, this applies if  $(k - j) > 0$  as otherwise, we need to accommodate the feedback polynomial into the equation, which is easily done. Modifications can also be made to take into consideration the use of several bits of  $A$  being used to determine the clocking of  $B$  and in cases where more than one register is used in determining the clocking of other registers. As we shall see in the basic stop-and-go generator, a system as simple as the above is inherently weak because if the sum of two consecutive output bits is 1, we already get information about bits in register  $A$ . In the more general situation of a polynomial  $P$  in the bits of  $A$  controlling the clocking of the register  $B$ , equation (1) becomes

$$B_k^t = B_k^{t-1}(P \oplus 1) \oplus B_{k-j}^{t-1}P. \quad (2)$$

We state and prove the following theorem involving several regularly clocked registers  $A_i$ .

**Theorem.** *Consider a bit-based LFSR system with  $k$  regularly clocked LFSRs  $A_i$  of length  $l_i$  respectively,  $1 \leq i \leq k$ , in which a linear polynomial  $L$  involving bits of the  $A_i$  determines the clocking of a register  $B$  of length  $m$  as described in (2). Suppose the output  $z^t$  at time  $t$  is the binary sum of the outputs of all registers. Then the initial state of all  $A_i$  can be recovered from a system of quadratic equations, and can subsequently be used to recover the output of  $B$ .*

**Proof.** We have  $z^t = B_m^t \oplus \sum_i A_{l_i}^t$ , and using (2), can write

$$z^{t+1} = B_m^t(L \oplus 1) \oplus B_{m-j}^t L \oplus \sum_i A_{l_i}^{t+1}. \quad (3)$$

$$\text{Therefore, } z^t \oplus z^{t+1} = L(B_m^t \oplus B_{m-j}^t) \oplus \sum_i (A_{l_i}^t \oplus A_{l_i}^{t+1}). \quad (4)$$

Multiplying by  $L \oplus 1$ , this results in an equation of degree at most two involving the bits of the  $A_i$ :

$$(L \oplus 1)(z^t \oplus z^{t+1}) = (L \oplus 1) \sum_i (A_{l_i}^t \oplus A_{l_i}^{t+1}). \quad (5)$$

This quadratic system can be solved for all bits of the registers  $A_i$  by running off sufficiently many output bits from the system. The output of  $B$  can then be calculated from

$$B_m^t = z^t \oplus \sum_i A_{l_i}^t. \quad \square$$

The above theorem indicates that using more than one regularly clocked register in a linear way to produce the output of the system adds no additional security, as one sufficiently long such register will suffice. This confirms, as a special case, the result of [23]. Although the assumptions of the Theorem apply only to the stop-and-go generator in our list of target ciphers, the method used in the proof applies to a general class of clock-controlled LFSR based systems, those in which a linear function of register bits controls the clocking of several registers. The alternating step and step1/step2 ciphers fall into this category. As we shall see in section 4, the method also works on a system with only one register - the self-decimated generator.

The generation of the equations (sufficiently many to be able to derive a solution from them for the unknowns) is independent of the register values, and so is assumed to be a precomputation procedure. In all cases below, we use a maximum of approximately 2 GB of memory for equation generation. While  $A$  produces linear equations from its feedback polynomial,  $B$  is producing higher degree equations and so its output is always used in the output of the entire system, which is therefore also highly non-linear. Our aim is therefore to reduce the high degree of the output equations. In each of the four systems discussed below, we take combinations of consecutive output bits in order to obtain reduced degree equations. We compare our attack against each system with other best attacks, based on the keystream requirements, the attack complexity, and the precomputation complexity. We also determine the effective key length for securing the system against the attacks.