PROCEEDINGS
Of SPIE-The International Society for Optical Engineering

Volume 948

High-T_c Superconductivity: Thin Films and Devices

R. Bruce van Dover, Cheng-Chung Chi
Chairs/Editors

Sponsored by
SPIE—The International Society for Optical Engineering
Cooperating Organization
The Metallurgical Society

16-17 March 1988
Newport Beach, California

Proceedings of SPIE—The International Society for Optical Engineering

Volume 948

High-T_c Superconductivity: Thin Films and Devices

R. Bruce van Dover, Cheng-Chung Chi
Chairs/Editors

Sponsored by
SPIE—The International Society for Optical Engineering
Cooperating Organization
The Metallurgical Society

16-17 March 1988
Newport Beach, California

Published by
SPIE—The International Society for Optical Engineering
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone 206/676-3290 (Pacific Time) • Telex 46-7053

The papers appearing in this book comprise the proceedings of the meeting mentioned on the cover and title page. They reflect the authors' opinions and are published as presented and without change, in the interests of timely dissemination. Their inclusion in this publication does not necessarily constitute endorsement by the editors or by SPIE.

Please use the following format to cite material from this book:
Author(s), "Title of Paper," *High-T_c Superconductivity: Thin Films and Devices,* R. Bruce van Dover, Cheng-Chung Chi, Editors, Proc. SPIE 948, page numbers (1988).

Library of Congress Catalog Card No. 88-60786
ISBN 0-89252-983-0

Printed in the United States of America.

Preface

In a continuing effort to improve the quality and scope of the technical program and the resulting proceedings, the organizers of the 1988 Symposium on Advances in Semiconductors and Superconductors: Physics and Device Applications decided that the manuscripts submitted for the conference proceedings should undergo a peer-review process. A mechanism was thus set up to implement the review procedure without creating a significant delay in publication.

Each manuscript was refereed by at least one reviewer, and the evaluations of the reviewers were considered in the final selection process for papers to be included in the proceedings. In order to improve quality, reviewer comments were provided to the authors for incorporation into their final camera-ready manuscripts for the conference proceedings.

The organizers appreciate the timely cooperation of the authors, reviewers, and program committees of each of these conferences, which enabled the manuscript review process to be conducted expeditiously and effectively. We believe that this review process has considerably enhanced the quality of the papers and hope that the results presented herein stimulate new advances in semiconductor and high-T_c superconductor physics and application.

The following is a list of the seven peer-reviewed proceedings resulting from this symposium:

Volume 942: *Ultrafast Laser Probe Phenomena in Bulk and Microstructure Semiconductors II,* Robert R. Alfano, ed.
Volume 943: *Quantum Well and Superlattice Physics II,* Federico Capasso, Gottfried H. Döhler, and Joel N. Schulman, eds.
Volume 944: *Growth of Compound Semiconductor Structures,* Anupam Madhukar, ed.
Volume 945: *Advanced Processing of Semiconductor Devices II,* Harold G. Craighead and J. Narayan, eds.
Volume 946: *Spectroscopic Characterization Techniques for Semiconductor Technology III,* Orest J. Glembocki, Fred H. Pollak, and Fernando Ponce, eds.
Volume 947: *Interconnection of High Speed and High Frequency Devices and Systems,* Alfred P. De Fonzo, ed.
Volume 948: *High-T_c Superconductivity: Thin Films and Devices,* R. Bruce van Dover and Cheng-Chung Chi, eds.

Federico Capasso, AT&T Bell Laboratories
Fred H. Pollak, Brooklyn College/City University of New York
Symposium Chairs

Related SPIE Publications

Vol.	Title	Editor(s)	Year
276*	*Optical Characterization Techniques for Semiconductor Technology*	D. E. Aspnes, S. So, R. F. Potter	1981
439*	*Picosecond Optoelectronics*	G. Mourou	1983
452*	*Spectroscopic Characterization Techniques for Semiconductor Technology I*	F. H. Pollak, R. S. Bauer	1983
387	*Technology of Stratified Media (Critical Reviews of Optical Science and Technology)*	R. F. Potter	1983
463	*Advanced Semiconductor Processing and Characterization of Electronic and Optical Materials*	D. K. Sadana, C. M. Lampert	1984
524	*Spectroscopic Characterization Techniques for Semiconductor Technology II*	F. H. Pollak	1985
530	*Advanced Application of Ion Implantation*	M. I. Current, D. K. Sadana	1985
611	*Laser Processing of Semiconductors and Hybrids (Critical Reviews of Optical Science and Technology)*	E. J. Swenson	1986
617	*Amorphous Semiconductors for Microelectronics*	D. Adler	1986
623	*Advanced Processing and Characterization of Semiconductors III*	D. K. Sadana, M. I. Current	1986
763	*Physics of Amorphous Semiconductor Devices*	D. Adler	1987
792	*Quantum Well and Superlattice Physics*	G. H. Döhler, J. N. Schulman	1987
793	*Ultrafast Laser Probe Phenomena in Bulk and Microstructure Semiconductors*	R. R. Alfano	1987
794	*Modern Optical Characterization Techniques for Semiconductors and Semiconductor Devices*	O. J. Glembocki, J. J. Song, F. H. Pollak	1987
795	*Characterization of Very High Speed Semiconductor Devices and Integrated Circuits (Critical Reviews of Optical Science and Technology)*	R. Jain	1987
796	*Growth of Compound Semiconductors*	R. L. Gunshor, H. Morkoç	1987
797	*Advanced Processing of Semiconductor Devices*	S. D. Mukherjee	1987
800	*Novel Optoelectronic Devices*	M. J. Adams	1987
861	*Quantum Wells and Superlattices in Optoelectronic Devices and Integrated Optics*	A. A. Adams	1988
879	*Sensing, Discrimination, and Signal Processing and Superconducting Materials and Instrumentation*	R. Nichols, J. A. Ionson	1988

Note: The volumes marked with an asterisk are out of print. The others are available from SPIE.

HIGH-T_C SUPERCONDUCTIVITY: THIN FILMS AND DEVICES

Volume 948

Conference Committee

Chairs

R. Bruce van Dover
AT&T Bell Laboratories

Cheng-Chung Chi
IBM/Thomas J. Watson Research Center

Session Chairs

Session 1—Properties of Films and Devices
Robert A. Buhrman, Cornell University

Session 2—Film Preparation and Properties
M. R. Beasley, Stanford University

Session 3—Novel Film Preparation
A. I. Braginski, Westinghouse Electric Corporation

INTRODUCTION

This conference brought experts on high-T_c superconducting materials together with scientists and engineers interested in using these materials to create a viable technology for the future. The promise of such a technology is enhanced performance in known devices and the potential for new applications; the downside is the difficulty of working with exotic materials under exotic conditions. The nascent science of high-T_c superconductivity is only 12 months old, and the emphasis of research has largely been on the materials and their properties per se. This emphasis is reflected in the dominant concern expressed at this conference—preparation and characterization of thin films. Device concepts have been actively pursued since early 1987, although experiments to date have served mainly to underline the difficulty of working with the new materials.

This conference presented a broad and deep perspective on thin film preparation. A number of themes wove through the presentations, and we summarize here some of the significant and novel concepts that were discussed.

The growth of thin films of a new 80 K superconductor, identified as $Ba_4Y_2Cu_8O_{20-x}$, was described by Beasley (Stanford) and Mandich (AT&T Bell Labs.). In-situ growth, i.e., deposition of fully superconducting oxides, rather than amorphous or semicrystalline precursor films, is the primary approach taken by Lathrop (Cornell) and Braginski and Talvacchio (Westinghouse), although there seems to be movement in this direction by most of the groups involved in thin film preparation. There is a consensus, also, that growth at lower temperatures ($<700°$ C) is desirable as it leads to films with better (smoother) and more reproducible morphology. Results along these lines were emphasized by Beasley, Mankiewich (AT&T Bell Labs.), and Wu (Rutgers). Low-temperature deposition also reduces chemical reaction with substrates, as pointed out by these authors and by Koinuma (Tokyo Institute of Technology). It is known that the oxidation state of materials in this class of superconductors has a strong effect on T_c. Photoemission study of superconducting thin films has provided some details of the Cu and O valence band under various annealing conditions (Shen, Stanford). Patterning is a crucial step in device fabrication, and two alternatives were described: wet processing (i.e., liftoff) by Mankiewich, and laser ablation yielding linewidths as small as one micron, by Scheuermann (IBM). A variety of deposition techniques, alternatives to the coevaporation of Ba, Y, and Cu, which gave the original successful thin films (Laibowitz, IBM), were described, including cosputtering from BaCu and YCu targets (Scheuermann), laser ablation (Wu, Mandich, and Kwok, SUNY/Buffalo), ion-beam sputtering (Yoshimura, Government Industrial Research Institute, Japan), and coevaporation with BaF_2 (Mankiewich). Thick films are also of potential importance for chip-to-chip interconnects and present some special problems, as discussed by Rautioaho (Univ. of Oulu, Finland).

The development of superconducting devices, passive and active, is an obvious motivation behind much of the activity in thin-film and thick-film high-T_c materials, and the importance of devices was an unstated assumption in most of the work discussed at the conference. Specific devices such as SQUIDs and S-N-S microbridges were discussed by Laibowitz and Mankiewich, respectively. Optical detectors based on granular films were the subject of the talk by Strom (Naval Research Lab.), and Braginski and Talvacchio reported a significant advance in the detectivity of such devices, a result that encourages us to expect further improvement with advances in understanding the behavior of high-T_c films.

(continued)

Finally, a series of presentations evaluated the potential of high-T_c superconductivity for applications involving both superconductors and semiconductors. In the related SPIE conference (Conf. 947) on Interconnection of High Speed and High Frequency Devices and Systems, Soloman (IBM) pointed out that the role superconducting interconnects and transmission lines might play in future high-performance systems is still controversial, but the work described by Russek (Cornell) and Mourou (Rochester) demonstrates the viability of passive high-T_c devices. In this conference, Singh (Oklahoma) suggested uses for superconductors as elements in active semiconductor devices to enhance their performance.

The response to this conference on superconducting thin films and devices was enthusiastic and gratifying. The chairs are grateful to the speakers and authors for delivering a first-rate program, and would like to especially thank M. R. Beasley for the excellent and well-received tutorial he prepared on superconducting electronics, which served as a splendid introduction to and backbone for the technical program.

R. Bruce van Dover
AT&T Bell Laboratories

Cheng-Chung Chi
IBM/Thomas J. Watson Research Center

HIGH-T_C SUPERCONDUCTIVITY: THIN FILMS AND DEVICES

Volume 948

Contents

HIGH-T_C SUPERCONDUCTIVITY: THIN FILMS AND DEVICES

Volume 948

Session 1

Properties of Films and Devices

Chair
Robert A. Buhrman
Cornell University

Abstract only

High T_c Superconducting Thin Films and Devices made from $YBa_2Cu_3O_y$

Robert B. Laibowitz and Roger H. Koch
IBM Research Division, P.O. Box 218, Yorktown Heights, NY 10598

We have used both electron-beam vapor deposition and sputtering systems to deposit superconducting thin films of the compound $YBa_2Cu_3O_y$. In the e-beam deposition system the three metals are individually evaporated in an oxygen partial pressure while the sputtering system uses composite targets. After a high temperature furnace anneal in flowing oxygen these films can have transition temperatures as high as 91 K. The films in thicknesses ranging from 0.07 to several microns are deposited on a variety of substrates such as alumina, Si, MgO, zirconia and $SrTiO_3$. The epitaxial films which are grown on polished $SrTiO_3$ single crystals generally show the highest critical current density, around 10^7 A/cm^2 observed at 4 K. Device applications of these films such as SQUIDs and transmission lines will be discussed with particular reference to the processing and patterning techniques used in their fabrication. These techniques include photo-and e-beam lithography, ion implantation and milling and laser ablation.

Ultra high speed electronics based on proposed high T_c superconductor switching devices

B.A. Biegel, R. Singh, and F. Radpour

The University of Oklahoma,
School of Electrical Engineering and Computer Science
202 W. Boyd Street, Norman, OK 73019

ABSTRACT

The development of superconductivity near 100 K allows hybrid superconductor/semiconductor electronic devices to be experimentally investigated as a means of realizing improved ultra high speed very large scale integration (VLSI) electronics. Incorporating superconductors into conventional semiconductor structures will be the most likely approach to developing hybrid VLSI devices. The analysis of passive hybridization (using superconductive interconnects) of semiconductor devices concludes that this approach might produce significant benefits in at least some cases. Active hybridization of semiconductor devices, in which the inclusion of superconductors in a semiconductor device significantly alters device operation, is treated briefly. Such devices might be a means of achieving revolutionary rather than evolutionary improvement of electronic systems. The hybridization schemes are illustrated with a proposed ultra high speed resonant tunneling transistor (RTT) structure and with hybrid MOSFET structures. From the processing perspective, rapid isothermal processing (RIP) based on incoherent light sources is a promising technology for the fabrication of hybrid devices.

1. INTRODUCTION

Electronic devices operating on the effects of superconductivity have been envisioned for many years as a possible means of producing the ultimate speed in solid state electronics. In fact, the best demonstrated switching time[1] of of 2 5 ps for a superconducting OR gate is more than a factor of 2 better than the 5.8 ps switching time of the fastest semiconductor device demonstrated to date.[2] However, in almost all ultra high speed applications, the technology alternatives must be compared on a broader scale than simply the speed of an isolated device. As discussed by Gallagher[3] in 1985, the tremendous speed potential of superconducting electronics (SuE) has been outweighed by other challenges and limitations of proposed or demonstrated superconducting devices. Thus, SuE has never been chosen over semiconductor electronics (SeE) for any general purpose application, even where high speed is the primary goal (e.g., in a supercomputer CPU).

The discovery[4] that certain copper oxides, notably $YBa_2Cu_3O_{7-\delta}$, have superconducting transition temperatures (T_c) of nearly 100 K has initiated a re-evaluation of the status and prospects of SuE. Although decreased cooling costs are likely in higher temperature SuE systems, it is clear that unless new devices are developed, SuE will still face the same limitations and challenges. However, this development has opened another approach to utilizing superconductors that could bypass these problems - that of hybrid superconductor/semiconductor systems. The lure of such a system is that the advantages of one technology might be able to ease the limitations of the other. This would certainly be a non-traditional occurrence, since advances in either technology would benefit, rather than threaten, the other. Such systems have been considered for some time with low temperature superconductors, for instance by Gallagher.[3] The very low operating temperatures required for these superconductors and the relatively high power dissipation densities of SeE, among other problems, relegate the two technologies to operating in separate systems.

However, using a 100 K (or higher) superconductor, sufficient heat can be feasibly removed from a liquid nitrogen cooled (77K) system to make hybrid devices and systems realizeable. This paper addresses those issues that are relevant to the development of hybrid devices which attempt to combine the advantages of superconductor and semiconductor technologies, yielding devices which are superior to either separate technology. The next section discusses the general considerations of hybrid systems and devices, concluding that hybrid devices will most likely be conventional SeE devices, "hybridized" by the inclusion of superconductors. The third section treats passive hybridization of SeE devices, in which superconductors act as (little more than) improved interconnects between SeE devices. The fourth section illustrates this concept in terms of a proposed ultra high speed resonant tunneling transistor. The fifth section presents briefly the concept of active hybridization, where hybridization causes a significant modification of the operating mechanism of the SeE-type device. This approach is illustrated in terms of the resonant tunneling transistor and hybrid MOSFET devices. Key materials and processing issues are presented briefly in the final section, focusing on the ability of rapid isothermal processing (RIP) to meet the unique challenges of hybrid device fabrication.

2. GENERAL HYBRID SYSTEM CONSIDERATIONS

In spite of the dominance of SeE, the competition between it and SuE is not likely to end. This is true not only because of speed considerations, but also due to the fact that the strengths and weaknesses of the two technologies are often diametric opposites as displayed in Table 1. For example, SuE devices (including the most popular SuE devices, which are based on Josephson junctions) have low-loss interconnects and ultra low power operation, but have low (if any) signal gain and lack many of the device characteristics which have proven so useful in transistors. SeE devices, of course, do have transistor characteristics and also produce a signal gain, but are increasingly plagued, in high speed applications, by the limitations of normally conducting interconnects and by relatively high power dissipation densities.

Table 1. Characteristics of SuE and SeE devices

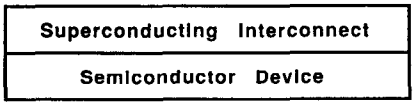
Technology	Advantages	Limitations
Superconducting Devices:	Speed: sub-picosecond delays attainable Power dissipation: low; ~ 1 μW/gate Interconnects: low-loss, fast, non-dispersive	Non-transistor-like: non-inverting latching: must be reset poor I/O isolation use threshold logic Power gain: low (if any)
Semiconductor Devices:	Transistor Qualities: inverting non-latching I/O isolation non-threshold logic Power gain: adequate	Speed: present devices limited to ≥ 1 ps delay Power dissipation: high; ~ 1 mW/gate Interconnects: lossy, low speed, dispersive

The complimentarity of SuE and SeE has traditionally meant that advances in one technology were directly deleterious to the other. Thus, the orders of magnitude improvement in SeE technology over the past 40 years have done more to keep superconductors out of general purpose high speed electronics than any other single factor. Another central cause of the dominance of SeE is that those systems which require ultimate speed also virtually always require VLSI circuit densities. In compensating for undesired SuE device characteristics, both in-

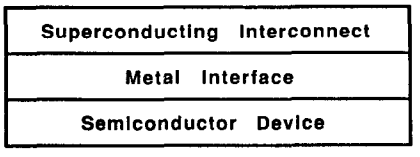
tegration density and speed must be sacrificed. Since the copper oxide superconductors are not likely to significantly modify the limitations of traditional SuE devices, we have turned to consider hybrid SuE/SeE systems. Given the dominance of SeE, we can be assured that proposed hybrid devices are superior to both separate technologies (for real applications) if they are superior to the best SeE devices

Considering the respective advantages given above for SeE and SuE, it is not dificult to determine the types of hybrid devices that should be researched in order to combine these advantages. Note that the advantages of SuE are the result of the properties and mechanisms that occur in superconductors, while those of SeE concern device characteristics. Thus, it makes sense to consider hybrid devices with a structure and operating mechanism similar to that of a SeE device, while incorporating superconducting materials into those structures. Incidentally, this approach greatly simplifies the comparison of the capabilities of a SeE device and its hybrid counterpart.

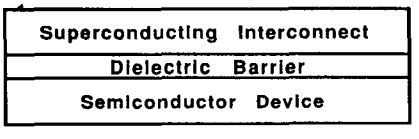
Regardless of whether hybridization is an active or passive modification of the SeE device, every hybrid device proposed will inherently require that superconductors be fabricated in close proximity to semiconductors. In interfacing any two dissimilar materials, the issues of lattice mis-match, thermal expansion coefficients, interdiffusion, surface states, and other characteristics of the interface must be confronted. The fabrication and processing of either material in the presence of the other could be fatal to the integrity of the device being constructed. It is possible at least for some devices, however, to configure the structure of interfaces and contacts such that these concerns are inherently lessened. There are actually three possible contact configurations, as depicted in Figure 1, that can be used to interface the superconductor and semiconductor. The first (Fig. 1a) is direct contact between the two materials. Theoretically, this is the ideal configuration, since it is the most likely of the three to produce the desired result of a reduced specific contact resistance. However, processing challenges concerning the copper oxides or poor interface characteristics may not allow direct contact.



a) Direct contact



b) Metal intermediary



c) Dielectric barrier

Figure 1. Hybrid system interface configurations

A second possibility (Fig. 1b) is to use a metal (or other conventional interconnect material) as an intermediate "interface matching" material. Because this configuration places the superconductor/metal contact in series with the usual metal/semiconductor contact, the net contact resistance will increase. Tzeng et al.[5] have investigated silver/$YBa_2Cu_3O_{7-\delta}$ contacts, which demonstrated a specific contact resistance more than an order of magnitude ($4x10^{-8}$ Ωcm^2 vs. $8x10^{-7}$ Ωcm^2) less than the best metal/semiconductor contacts.[6] Thus, superconductor/metal/semiconductor contacts should achieve almost the same specific contact resistance as metal/semiconductor contacts. The use of low contact resistance materials (e.g., silicides and polysilicon) as a "matching" layer should be investigated as well.

The third possible contact configuration (Fig. 1c) is to place a Schottky barrier or tunnel barrier dielectric between the superconductor and semiconductor. With this configuration, the interviening dielectric protects the underlying layer, be it semiconductor or superconductor, against the fabrication, processing, and proximity of the other material, which should ease processing challenges. Thin film epitaxial dielectrics that can serve as an effective substrate for the growth of both semiconductors and the copper oxide materials have been investigated by Singh et al.[7] A barrier contact might be nearly as lossless as a direct contact for some devices. In fact, the tunnel barrier configuration is used in the high speed resonant tunneling transistor discussed in the section 4.

The nature of electronic system for which hybrid devices might be a feasible alternative remains to be determined. This information will provide further specification as to the type of devices that should be investigated. From the short discussion above, it is apparent that the fabrication of hybrid devices is not only less established than silicon processing technology, but also more challenging Both the materials and processing will be more expensive. For this reason, as with GaAs devices, since hybrid devices are not superior in terms of cost, they will only be used in applications which require superior performance - high speed electronics. Knowing the trend in electronics toward higher density and integration levels, we should also realize the importance of device scaleability. A hybrid device must have both superior speed and be highly integrable to be practical in future market applications. It is with this understanding that hybridization is treated in the following sections.

3. PASSIVE HYBRIDIZATION - INTERCONNECTS

Passive hybridization indicates that the addition of superconductors to a conventional SeE device does not modify its operating mechanisms, although the system itself (e.g., speed, power consumption, or integration density) will hopefully be improved The most obvious approach to passive hybridization is to use superconductors as interconnects between the SeE devices. As mentioned, high speed SeE are increasingly facing limitations due to presently used resistive interconnects (metals, silicides, and polysilicon). It is the purpose of this section to determine the nature and amount of improvement that are afforded by switching from normal to superconducting interconnects.

To illustrate the problems that arise for normal interconnects as devices are scaled to ever-smaller dimensions, consider the conventional method of scaling called constant field (CF) scaling.[8] The CF scaling method and its effects on interconnects are summarized in Table 2. Ideally, all dimensions and the supply voltage(s) are reduced by a factor of S, with S > 1, resulting in an improved (i.e., reduced) device propagation delay by a factor of S. However, Table 2 indicates that CF scaling degrades the characteristics of normal interconnects.

Table 2. CF scaling: effects on local interconnects

Scaled Parameter	Absolute Increase	Relative Increase	With Respect to Scaled ..
All distances	1/S	1	Distances
Doping density	S	-	----
Voltage supply	1/S	1	Voltage supply
Device current	1/S	-	----
Device delay	1/S	1	Device delay
Interconnects:			
Delay	1	S	Device delay
Current density	S	-	----
IR voltage drop	S	S^2	Voltage supply
Contact resistance	S^2	-	----
Contact voltage	S	S^2	Voltage supply

Interconnect scaling can be viewed as a competition between integration density, which CF scaling attempts to increase, and other interconnect parameters, which CF scaling degrades. First consider interconnect resistance, which is given by:

$$R_l = \rho L/A \quad (1)$$

where ρ, L, and A are the resistivity, length, and cross-sectional area, respectively, of the interconnect. Thus, in scaling all distances by S, R_l increases by S. With a decrease in total current by S, the interconnect IR voltage drop remains the same, and increases by S relative to the supply voltage. Even more serious for high speed devices is the effect of R_l on the interconnect propagation delay. Since interconnect and load capacitances decrease by S with CF scaling, the intrinsic RC delay tends to remain approximately constant. Relative to the device delay, the interconnect delay actually increases by a factor of S. Worse still, as noted by Gallagher,[3] scaling in real IC's results in more degradation than that predicted by these simple calculations.

For devices with low current capability (to charge capacitances), or for any device that operates in the picosecond or sub-picosecond range, the propagation delay of interconnects can exceed the device propagation delay. For example, Shibatomi and Yokoyama[9] estimated that an average wiring delay of 2 ps per gate would result in a 2000 gate high electron mobility transistor (HEMT) IC in which the individual gates could achieve a delay as small as 1 ps. Regardless of the particular numbers, it is clear that faster devices will yield ever more marginal improvements unless more ideal interconnects are realized. For existing devices and interconnect materials, the cross-over between device-dominated and interconnect-dominated high-density IC's appears to occur when devices reach intrinsic propagation delays of 1 ps or more.

Scaling of normal interconnects, and thus VLSI density, is limited by other factors as well. For instance, contacts resistance increases by S^2 with CF scaling, as determined by the specific contact resistance and the contact area. The IR voltage drop of a CF scaled contact increases by S (by S^2 with respect to the supply voltage). We can choose a material (e.g., a silicide or polysilicon) with a reduced specific contact resistance, but these incur an integration density penalty due to higher resistivity ρ. To achieve a acceptably low R_l, the cross-section A must be increased. Finally, since current density increases by S with CF scaling, highly scaled interconnects face reliability concerns. Both speed and integration density are critical parameters in leading edge systems, but both are adversely affected by the scaling of resistive interconnects that is necessary for VLSI circuit density. These concerns of interconnect scaling are discussed in more detail by Meindl.[8]

The copper oxide superconductors present an alternative interconnect material, and their use might ease both the propagation delay and integration density concerns of normal interconnects. The properties of superconducting interconnects have interrelationships and trade-offs at least as complex as those discussed above for normal interconnects. To compare the propagation delays of superconducting and normal interconnects, the results of Bakoglu and Meindl[10] will be used, and their equations adapted to the case of resistanceless interconnects. The assumed circuit configuration was a MOSFET driving an interconnect and the gate of another MOSFET as shown in Figure 2a. The equivalent circuit for the case of a normal interconnect is shown in Figure 2b and for a superconducting interconnect in Figure 2c. The propagation delay was defined as the time between the instantaneous switch to V_{dd} by the power supply and the rise to $0.9V_{dd}$ at the gate of the second transistor.

According to Bakoglu and Meindl, the propagation delay for normal interconnects is closely approximated by:

$$T_n = R_l C_l + 2.3(R_d C_l + R_d C_g + R_l C_g) \quad (2)$$

where R_l is the resistance of the (normally conductive) interconnect, C_l is its capacitance, R_d is the output impedance (including source and drain contact resistances) of the driver transistor, and C_g is the gate

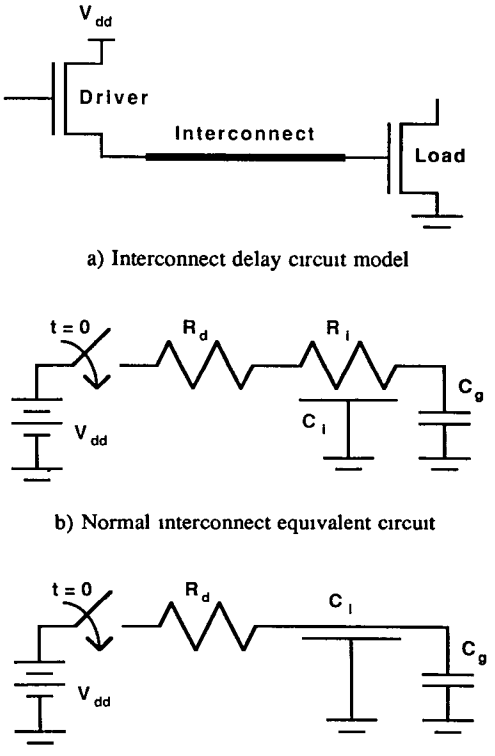


Figure 2 Circuit models for interconnect delay calculations

capacitance of the load transistor. Thus, the propagation delay for the superconducting interconnect case is.

$$T_s = 2.3R_d(C_l + C_g) \quad (3)$$

In order to simplify calculations, the following reduced (or normalized) parameters are introduced·

$$t \equiv T_s/T_n \quad (4)$$

$$r \equiv R_l/R_d \quad (5)$$

$$c \equiv C_l/C_g \quad (6)$$

With these definitions, the reduced time delay can be written:

$$t = [1 + (r/2\,3)(c + 2\,3)/(c + 1)]^{-1} \quad (7)$$

The reduced time delay is rather insensitive to c, especially when it is greater than 10 or less than 0.1. The three curves in Figure 3 thus display the entire range of both parameters (r and c) and the resulting values of the reduced propagation delay from Eq. 7. The important conclusion to be drawn from Eq 7 and Fig. 3 is that the larger the value of r ($\equiv R_l/R_d$), the better the improvement factor Obviously, if the resistance of the interconnect being replaced is comparable to or greater than that of the driver transistor, significant improvement will be observed. However, as will be determined below, reducing R_d may not be an effective method of increasing the improvement factor.

Now it remains to determine typical values of r and c (for VLSI electronics). For C_l, use a typical value[10] of 3 pF/cm (which Bakoglu and Meindl determined would be independent of scaling using proper scaling techniques) Estimate C_g as a parallel plate capacitor, which has a capacitance of.

$$C_g = \varepsilon A_g/t_g \quad (8)$$

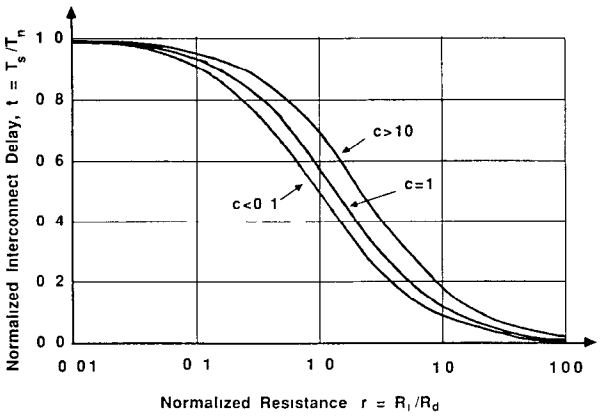
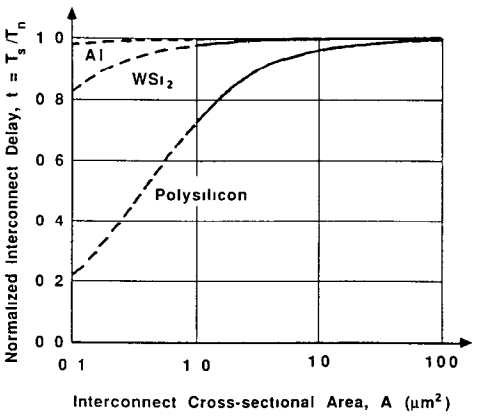
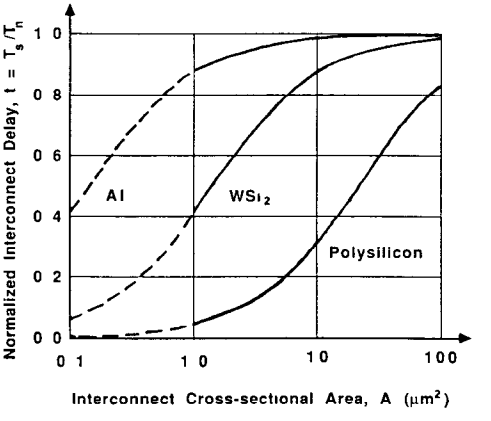


Figure 3. Passive hybridization delay improvement factor



a) 100 μm interconnect



b) 1 cm interconnect

Figure 4. Passive hybridization delay improvement factor

Here, ε is the gate dielectric permittivity, A_g is the area of the gate, and t_g is the gate dielectric thickness. Taking reasonable values for a high speed VLSI MOSFET (A_g = 5 μm^2, t_g = 20 nm), and with SiO_2 as a gate dielectric ($\varepsilon = 3.9\varepsilon_o$), the result is C_g = 17 fF. Thus, for local interconnects (3 μm < L < 300 μm), C_g is approximately equal to the average value of C_t, so the c = 1 curve will be used For non-local interconnects (0.03 cm < L < 3 cm), the interconnect capacitance dominates the gate capacitance, so the c > 10 curve will be used.

Considering resistance values, note that R_d can vary widely, depending on the technology (e g., MOSFET, bipolar, etc.), so a reasonable (MOSFET) value of 1 KΩ will be chosen The effects of this choice are discussed below. The interconnect resistance can vary even more than that of the driver transistor, depending on the cross-sectional area of the interconnect, as given by Eq 1 (the length is much more difficult to reduce). For VLSI electronics, the interconnect cross-section should be reduced as far as possible, but there are limits to the scaling of superconducting interconnects The most significant limitation for the copper oxide superconductors appears to be their critical current density, above which superconductivity is destroyed. The current that the superconductor is required to pass is dependent on the type of devices it connects. In general, the lower R_d, the higher the peak current, I_p, in the interconnect will be. Referring to Figure 2c, it is clear that the largest possible I_p will be:

$$I_{p,max} = V_{dd}/R_d \quad (9)$$

Since current density is current divided by cross-sectional area, the minimum acceptable cross-section, A_{min}, is calculated as the peak current divided by the critical current density, J_c:

$$A_{min} = I_{p,max}/J_c \quad (10)$$

Combining Equations 9 and 10 gives:

$$A_{min} = V_{dd}/(R_d J_c) \quad (11)$$

At 77 K, critical current densities as high as $2x10^6$ A/cm^2 have been reported.[11] Knowing that repeatable results have been difficult to attain, this value will be derated herein by a factor of ten. V_{dd} = 2 V will be used for this analysis. This results in a minimum cross-sectional area of 1 μm^2. With these values, the plots in Figures 4a and 4b were constructed for inter-device interconnects of typical (L = 100 μm) and long (L = 1 cm) lengths, respectively. These plots again give the propagation delay improvement of superconducting interconnects for the configuration of Figure 2a, but here as a function of the interconnect cross-sectional area The results were extended to a cross-sectional area of 0.1 μm^2 (for $J_c = 2x10^6$ A/cm^2 in Eq. 11) with a dashed line. The delay improvement was treated for three normal interconnect materials, aluminum, a silicide (WSi_2), and polysilicon, with assumed resistivities of 3 μΩcm, 30 μΩcm, and 500 μΩcm, respectively.[10]

Now consider again the effect of R_d on the reduced time delay. For example, if we assume an R_d of 10 KΩ, A_{min} is reduced by a factor of 10, so it would appear from Figures 4a and 4b that the improvement factor, t, would be much better (smaller) for this case. However, r (≡ R_t/R_d) is also decreased by 10, so it takes an extra decade of cross-sectional area to reach the same (r and) t values as those achieved with R_d = 1 KΩ. Although the improvement factors are equal (albeit at different areas), the higher resistance case would seem to be of more interest for VLSI because smaller interconnect cross-sections are possible. Do not forget, however, that t is an improvement factor; not the actual delay. It happens that higher output resistances directly reduce the current driving capability of the driver device, thus requiring proportionately more time to charge line and load capacitances In other words, both T_s and T_n increase rapidly with increases in R_d, although T_n does so more swiftly. Since speed is the primary concern in finding appropriate devices for passive hybridization, devices with low output impedance are necessary. In order to accomodate the current driven by these devices, larger interconnect cross-sections and/or higher critical current densities are required.

The conclusions to be drawn from Figures 4a and 4b are summarized in Table 3. Up to the derated critical current density, little improvement would be observed by replacing typical length interconnects of any of these material with superconducting lines. For long (inter-device, on-chip) interconnects, superconducting lines still show little improvement over aluminum lines. The delays of both WSi_2 and polysilicon significantly improve at this length. These latter materials, however, are typically used only for local interconnects, the reason for which is quite apparent from Figure 4b.

Table 3. Summary of passive hybridization improvement factor

Interconnect Material	Interconnect Length Typical (100 μm)	Long (1 cm)
Aluminum	small	small
Silicide (WSi_2)	small	moderate - large
Polysilicon	small - moderate	moderate - large

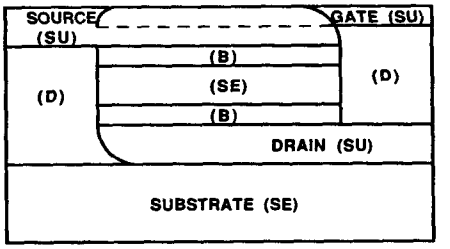
There are yet two reasons why superconducting interconnects represent an opportunity to ease the limitations imposed on high speed VLSI by normal interconnects The first is, of course, the fact that the minimum allowed cross-sectional area was derated by a factor of 10 and, in fact, future improvements in the allowed critical current density are likely. Further, the curves in Figure 4 represent the worst case current load on the superconductors, which may be far from reality. In particular, there will be a small series inductance of the interconnect the main effect of which will be to hold down the magnitude of the initial current spike, the value of which is given by Equation 9 and was used to determine the critical current density limit. Finally, in contrast to scaling of normal interconnects, no penalty is incurred by scaling the cross-section of a superconducting interconnect to its critical current density limit, A_{min} (given a safety margin). (This does not change Figures 4a and 4b, since C_l is independent of A for properly scaled interconnects; i.e., not CF scaling.) Thus, an improvement in interconnect density could also result in the event that higher critical current densities are allowed.

The above discussion assumes that the driver output resistance is unchanged by the adoption of a copper oxide interconnect. Of course, the use of a copper oxide superconductor may change the specific contact resistance, resulting in an accompanying change in R_d and an opposite change in the reduced resistance, r. Thus, if the specific contact resistance increases, r will decrease, and the improvement of the superconducting line will decrease or possibly be negative. On the other hand, if the specific contact resistance decreases, r will increase, and the improvement factor will be greater than the results given above. This would lower the propagation delay and/or allow further scaling of the contacts. Higher device packing densities would result from smaller contacts, especially if the contacts previously accounted for a significant amount of the total device area. Due to the lack of experimental data for the copper oxide superconductors, no definite conclusions can yet be made as to the characteristics of these superconductor/semiconductor contacts (in any of the three configurations discussed).

In summary, passive hybridization of SeE would be most warranted for devices which have picosecond-range switching times, which typically use silicide or polysilicon interconnects, which have a low output impedance to charge capacitances quickly, and in which indirect contact to the interconnect is an acceptable or inherent characteristic of the device. In addition, if the specific contact resistance of copper oxide/semiconductor contacts is lower than that of metal/semiconductor contacts, this scheme would greatly benefit any device, but particularly those in which the contact area is a significant fraction of the total device area.

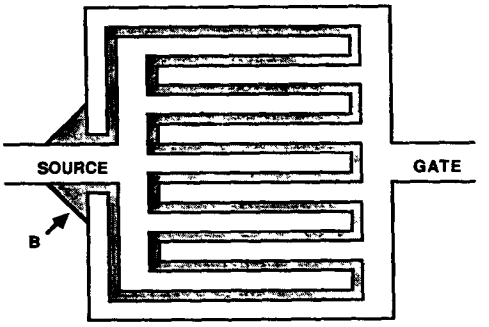
4. AN IDEAL RESONANT TUNNELING TRANSISTOR

A resonant tunneling transistor (RTT) structure proposed previously,[12] and shown in Figures 5a and 5b, has several of the characteristics desirable for passive hybridization This paper discusses only those details of the operation of this device which are relevant to passive hybridization. A review of resonant tunneling (RT) and various RT devices is given by Capasso.[13] Except for the use of a gate potential rather than biasing to modulate the resonant tunneling current, the structure and operation of this device are virtually identical to that of the simplest RT device, the resonant tunneling diode (RTD). Maximum oscillating frequency measurements[14] and numerical simulation[15,16] of the RTD yield a propagation delay or switching time of 100-200 fs. Because of the similarity of the proposed RTT to the RTD, it should achieve a comparable switching time. This fact alone suggests its suitability for passive hybridization - normal interconnect propagation delay would completely dominate the device delay.



SU Superconductor SE· Semiconductor
B Barrier Layer D Dielectric

a) Hybrid RTT side view



b) RTT source/gate configuration

Figure 5. Hybrid resonant tunneling transistor (RTT)

Also, note that the superconductor/semiconductor contacts are inherently indirect in this device - a tunnel barrier separates the semiconductor layer from the superconductor interconnects. This can greatly ease processing and fabrication considerations If conduction band offsets between the superconductor and semiconductor require unreasonably large source-drain biasing, however, additional layers of semiconductor would have to be inserted between the superconductor and barrier layers. This would result in one of the other two contact configurations (Figure 2a or 2b) being used. Note that, in order to be able to effectively modulate the potential of the central layer to switch resonant tunneling on and off, a low density of states material ($n < 1x10^{18}/cm^3$) must be used here. This essentially limits the choice to semiconductors, resulting in the possibility of undesirably large band offsets and biasing.

Finally, the proposed RTT would greatly benefit from passive hybridization in the event that this technique reduces specific contact resistance. Note that the RTT, because of its vertical structure, has no device area beyond the contacts. Thus, it would gain the maximum possible packing density benefit if scaling of interconnects were desired rather than a lower interconnect propagation delay. In summary, it is the speed and packing density considerations that make the proposed RTT a perfect choice for passive hybridization, but it is the fact that tunnel barrier contacts are an inherent feature of the device that helps to make its passive hybridization feasible.

5. ACTIVE HYBRIDIZATION

Active hybridization indicates that the inclusion of superconductors into a SeE structure results in a significant modification of the operating mechanisms of the device. Such superconducting effects as coherence, the proximity effect, superconductive tunneling, and the Josephson phenomena, would act to change (and hopefully improve) device operation. Because these are quantum phenomena, actively hybridized devices could well demonstrate revolutionary capabilities as compared to the original SeE device. The device should still retain most of its original operating characteristics - the proven advantages of

SeE devices should not be forgotten. Because of the multitude of possibilities for activiely hybridized SeE devices, only a cursory treatment of the subject is conducted here.

Considering the RTT, active hybridization could be accomplished if a superconductor could be used as the center layer The copper oxide compounds investigated to date have a density of states[17] of at least $1x10^{21}/cm^3$, so they are not useful for this layer. If new superconductors reported recently,[18] or any discovered in the future, have the desired carrier densities as well as critical temperature, they could be used as the center layer. This would assure very low biasing potentials and thus power dissipation. It also presents the possibility of active hybridization through the use of supercurrent tunneling and resonant tunneling. An ingenious setting of the maximum zero voltage tunneling supercurrent and the resonant energy level(s) might dramatically improve device operation.

Active hybridization has been demonstrated with the MOSFET, using low temperature superconductors, in a structure sometimes called a semiconductor-coupled Josephson junction.[19] A typical structure, which will be called the hybrid MOSFET herein, is shown in Figure 6. This is an actively hybridized device because the gate modulates coherent (superconducting) current flow between the source and drain electrodes. The dependence of the proximity effect on carrier density[20] allows the semiconductor channel to act like a superconductor for appropriate gate potentials.

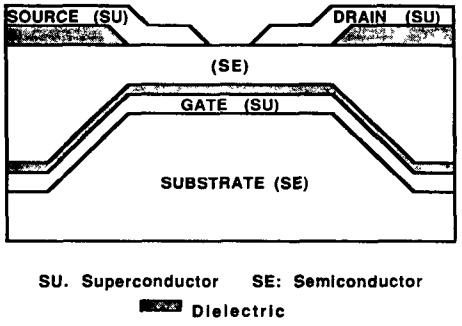


Figure 6. Hybrid MOSFET device

Isolated hybrid MOSFET devices have been fabricated, and propagation delays of 20 ps were reported in 1985.[21] This is about the same as the best reported results at the time for conventional NMOS transistors.[22] The indication from these results is that this relatively new technology is likely to show a significant speed improvement over the conventional device as its technology matures. We propose that this mechanism be used in a MESFET or MODFET structure, which appear to be capable of as much as an order of magnitude shorter propagation delays than a MOSFET. In particuar, the MODFET may be able to produce a 1 ps propagation delay,[9] indicating that a subpicosecond delay might be attainable in the hybrid version. This device does have problems concerning voltage gain, as discussed by Gallagher,[3] but it serves to illustrate the concept of active hybridization

Note that for both the MOSFET and RTT devices, analogous hybrid structures can be designed for use with hole or electron superconductors as necessary.

6. FABRICATION AND PROCESSING RESULTS

Realization of any proposed hybrid device presents challenges in both materials and processing technologies. In particular, lithography and selective deposition of materials are the key processing areas that need to be explored further. An ideal hybrid structure requires crystalline epitaxial layers of high temperature superconductors, semiconductors, and dielectrics in a desired sequence. Simply manufacturing the required quality of copper oxide thin films will be challenging, but hybrid systems add the additional requirement that the integrity of all existing layers of various materials be maintained during this fabrication. Rapid isothermal processing (RIP) based on incoherent optical heating sources is a promising technology for the fabrication of hybrid structures and devices.[23] Starting with silicon as a substrate, epitaxial dielectric films of II-A flourides can be deposited by RIP.[7] Required layers of superconductor and semiconductor can then be deposited using RIP assisted metalorganic chemical vapor deposition (MOCVD). The details of this technique are presented in Ref. 12.

As a gate dielectric material, Y_2O_3 can be used in hybrid devices incorporating the copper oxide superconductors. Thin films of yttrium were evaporated on a p-type (100) silicon substrate. After evaporation, the sample was transferred to a commercial rapid isothermal processor (A.G. Associates heat pulse processor model 410). A two-step oxidation (300°C, 150 sec. and 700°C, 140 sec.) was followed by an 800°C, 10 sec. in-situ anneal in nitrogen The high-frequency C-V curve of the resulting 60 nm Y_2O_3 film is shown in Figure 7. The dielectric constant is $\varepsilon_r = 17.72$, and the flat band charge density is approximately $3.67x10^{11}/cm^2$. The measured leakage current is shown in Figure 8 These are preliminary results, and indicate that process optimazition through a better understanding of oxidation mechanisms can lead to high quality Y_2O_3 films formed by RIP.

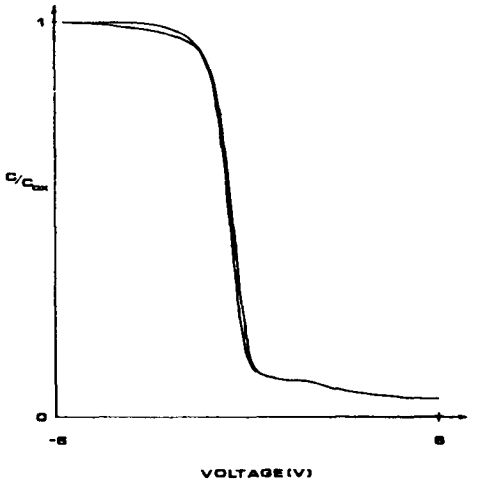


Figure 7. Y_2O_3 film high-frequency C-V curve

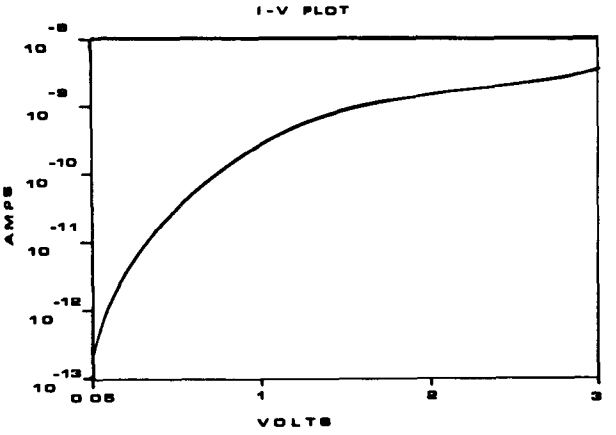


Figure 8. Y_2O_3 film leakage current