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Amorphous Insulating Thin Films II

R.A.B. Devine
W.L. Warren
J. Kanicki
M. Matsumara
editors

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Preface

The contents of this volume of the Journal of Non-Crystalline Solids contains a large fraction of the papers presented at the symposium 'Amorphous Insulating Thin Films II' which took place in Strasbourg, France from 24 to 27 May 1994. The symposium was organized under the auspices of the European Materials Research Society and was a follow-up to one organized in the USA during the Fall 1992 meeting of the Materials Research Society in Boston. 113 participants were registered for the Strasbourg meeting representing more than 20 different countries from around the world. Presentations at the symposium were divided between oral and poster sessions, and for the first time we introduced the concept of an extended panel session entitled 'Microscopic Characterization of the Si/SiO_2 Interface' during which invited speakers were asked to present different characterization methods. This session was well attended and the organizers would like to sincerely acknowledge the efforts made by Tatsumi Mizutani who set up and steered the session and J.-J. Benattar, W.M. Lau, A. Ishitani, B. Drevillon and A. Crossley who kindly accepted to 'defend their causes'.

Of the 112 papers scheduled for presentation either in the poster or as oral format, 73 originated from University laboratories, 28 from national research laboratories and 11 from industrial laboratories. If these statistics can be generalized, they give a good insight into the trends in materials research and indicate that, increasingly, it is being performed in the academic environment rather than in the industrial sector. Finally, we would like to thank all of the participants who made the effort to come to Strasbourg and who made the symposium the success that it was.

Rod Devine
Bill Warren
Jerzy Kanicki
Masakiyo Matsumura

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Section 1. General

Dielectrics in microelectronics – problems and perspectives

P. Balk*

DIMES, Delft University of Technology, P.O. Box 5053, 2600 GB Delft, The Netherlands

Abstract

This review is focussed on the most demanding application of dielectrics in microelectronics, namely that in field effect technology. It is shown that the requirements of this technology can only be met in silicon devices; the developments over the past 30 years indicate that there is no reliable replacement for $Si–SiO_2$ in the gate system. However, for DRAM capacitors the use of alternative dielectrics with higher dielectric constant and of ferroelectrics turns out to be unavoidable but also manageable. The limitations of other semiconductor systems with regards to dielectrics are briefly reviewed.

1. Introduction

Dielectrics fulfill a number of essential functions in the fabrication and operation of semiconductor devices and integrated circuits. The chemical characteristics of these materials are generally decisive when employing them as masks in classical diffusion processes or to define areas of localized growth and when using them as capping layers to prevent loss of material when thermally activating implants. Critical applications are certainly those where a particular dielectric is selected because of its effect on the electrical characteristics of devices and circuits. Typical examples are the application as an insulator between conductors or as a material to passivate the surface of the semiconductor. Particularly demanding are functions as capacitor dielectric or as gate dielectric in the insulated gate field effect device technology. For the gate application the stability of device threshold and transconductance is the prime requirement. On the other hand, the capacitor application demands high storage capacity at very low charge leakage.

For most semiconductors these requirements, particularly for field effect device and capacitor application, are hard to fulfill. A favorable situation in silicon technology, which is related to the properties of thermally grown SiO_2, is the exception rather than the rule. By the same token, this feature of the $Si–SiO_2$ system is the reason for its dominance in the field of microelectronics. A discussion of the requirements of device applications and their fulfillment in Si technology using SiO_2 and, when necessary, also alternative dielectrics will therefore constitute the main theme of this review.

2. Requirements on dielectrics in field effect technology

It is essential for the design and operation of metal-oxide–silicon field effect transistor (MOSFET) circuits to have devices with controlled

* Corresponding author. Tel: +31-15 78 4963. Telefax: +31-15 622163.

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characteristics. In practice this means a well-defined threshold and transconductance obtained by having a minimum amount of charge trapped in the gate dielectric and a minimum density of traps at the semiconductor–dielectric interface. Moreover, these characteristics should not change with time. Injection of carriers into the dielectric will lead to charge capture and generation of new bulk and interface traps, and thus to changes in the device characteristics. This implies that the barrier against injection of carriers into the insulator should be high, which is generally the case for high band gap dielectrics. Moreover, the efficiency for generating bulk and interface states should be as low as possible [1, 2].

In dynamic random access memories (DRAMs) the basic cell consists of a MOSFET in series with a capacitor. In the two logical states of the cell the capacitor is either charged or free of charge. Since the capacitor does not have a channel like the MOSFET, the electrical properties of the interface are not critical. In fact, metal electrodes may be inserted between semiconductor and dielectric. However, the memory only functions if at least a minimum amount of charge is stored, which defines a lower limit of the capacitance of the device [3]. In the ultra large scale integration (ULSI) technology this can be realized by extending the capacitor area in the third dimension (employing trenches, stacked folded layers or structured surfaces) or by using high dielectric constant materials. In addition, to limit the number of refresh operations, there is a minimum acceptable amount of charge loss by leakage (10^{-7}–10^{-8} A cm^{-2}).

In contrast to the DRAM technology, where the information is lost when the supply voltage is switched off, non-volatile memories maintain the information independent of such interruptions. In this case the cell consists of one single field effect transistor with two logical states corresponding to two threshold values. One of these threshold values is that for the charge-free gate insulator system, the second is that for the charged gate insulator system.

Two different approaches are being used for charge storage. In the first the charge is stored in the dielectric itself, which therefore should have a large trapping state density. The dielectric mostly used for storage is Si_3N_4, with a very thin barrier of SiO_2 on the channel side to improve the interfacial properties and increase the storage time. In the second approach an electrically floating poly-Si electrode is used for storage; it is insulated from the channel and the control gate by SiO_2 films. Charging and discharging take place by means of tunnel injection of carriers or by hot carrier injection. It should be noted that these are the very processes which one tries to avoid in the operation of standard MOSFETs since they lead to permanent changes in the device characteristics. Such degeneration phenomena limit the number of feasible charge-discharge operations to around 10^5 for floating gate structures (FLOTOX: floating gate tunnel oxide memory), to over 10^7 for storage in a nitride film with an additional SiO_2 layer on the gate electrode side to improve charge retention (SONOS: poly-Si gate/oxide/nitride/oxide/semiconductor memory) [4].

3. Dielectrics in the classical MOSFET technology

It has been known for many years that SiO_2 obtained by thermal oxidation of Si in an O_2 or H_2O atmosphere is a nearly ideal insulator and exhibits an excellent 'fit' to the semiconductor substrate. The Si–SiO_2 system provides high temperature diffusion masking, constitutes a passivated semiconductor surface and, above all, is the basis of the MOSFET technology. Since its inception in the early sixties this technology has developed rapidly. Originally the interest was mainly focussed on the macroscopic material properties of the insulator. The question of the atomic structure of electrically active defects in Si–SiO_2 became a major topic in the seventies. At the present time most of these developments are textbook material [5, 6].

The most striking features of the Si–SiO_2 system are the following: high temperature annealing in neutral ambients after oxidation suffices to lower the oxide charge to less than 10^{11} electron charges per cm^2. A low temperature post-metallization anneal in the presence of an Al gate electrode reduces the density of interface states below 10^{10} cm^{-2}. The combination of these annealing steps produces a well-defined threshold voltage and a high transconductance in MOSFETs. These features are both essential for the operation of integrated circuits.

The main reliability problems related to the gate dielectric in early MOSFETs were low field breakdown and electrical shorts, caused by extended defects in the film or by contaminants, particularly Na^+ ions. Na^+ ions also affect the threshold voltage. The introduction of clean processing and the insertion of a barrier layer on the gate side of the oxide effectively solved these problems. Low phosphorus concentration phosphosilicate glass (PSG), chemically vapor deposited (CVD) Si_3N_4 and CVD Al_2O_3 were proposed as barrier or trapping layers of Na^+. By keeping a SiO_2 layer adjacent to the silicon the favorable properties of the Si–SiO_2 interface were preserved in the gate structure. Only the SiO_2–PSG combination has been extensively used. Interestingly, SiO_2–Al_2O_3 has also been considered as a gate dielectric for enhancement n-channel MOSFETs because of the tendency of Al_2O_3 to charge up negatively due to its affinity for electrons [7]. Because of its technical interest the physics and technology of the Si–SiO_2 system dominated the programs of the different scientific conferences in the field of semiconductor–insulator technology.

Two of these have been held regularly for many years: the Semiconductor Interface Specialists Conference (SISC, in the USA, mostly annually since 1965); the Insulator Films on Semiconductors Conference (INFOS, in Europe, biennially since 1979). The published proceedings of the latter conference present an excellent overview of the development of the field over the past 15 years.

4. Newer developments

The development of the MOSFET technology to higher densities and smaller dimensions in the seventies and eighties had major consequences for the gate dielectric. Because of the higher fields in devices of reduced dimensions the problem of carrier heating, injection across the semiconductor–dielectric barrier and trapping in the dielectric became acute. This made the use of PSG, Si_3N_4 and Al_2O_3 with their high trap densities [7] problematic, so that gradually only single films of SiO_2 were employed. Consequently, attention shifted to the trapping behavior and the corresponding point defects of thermally grown SiO_2. Even though the defect densities in this dielectric (typically 10^{11}–10^{12} cm^{-2}) are lower by a few orders of magnitude (typically 10^{11}–10^{12} cm^{-2}) their control became of considerable importance.

Electrically active defects in SiO_2 may be introduced by foreign atoms, like Si dopants [8], but in most cases their concentrations are negligible. The so-called water-related defects [9] (Si–OH groups or H_2O dissolved in the SiO_2 network) are difficult to avoid and may be present in concentrations of 10^{11}–10^{12} cm^{-2}. They strongly affect the characteristics of the device when charge is injected. Electrically active intrinsic defects are known to occur in connection with oxygen deficiency [10] or strain in the oxide [11]. To this category also belongs the dangling bond ('trivalent silicon') interface state at the Si–SiO_2 interface [12].

Quantitatively more important than the defects which are present in the as-prepared MOS structure are those generated by injected carriers or by energetic radiation. The condition for the generation of these defects, which appear as bulk and as interface states, is the capture of the carriers by bulk defects [13]. Also, the presence of water-related defects and hydrogen transport appear to be conditions for the generation of interface states [14]. Since these states cause considerable changes in the characteristics of MOSFETs it is important to prevent them by minimizing the density of injected carriers and the fraction of these carriers that will interact with the oxide to form new defects.

5. Optimizing the Si–SiO_2 system

Notwithstanding attempts to reduce the exposure to high temperatures by using CVD-SiO_2 as a gate insulator, it appears that in order to match the quality of thermally grown SiO_2 films high temperature annealing is required. Thus, thermal oxidation remains the preferred method for preparing this gate insulator. However, considerable efforts have been made to maximize the level of control of the film properties and to move the limits of application of SiO_2 by reducing its sensitivity to carrier injection. In line with the development of the MOSFET technology to small dimensions this work focussed on SiO_2 films thinner than 10 nm.

In this thickness range the rate of generation of interface states and the density of injected charge necessary to cause breakdown of the film for a given average field in the oxide decrease with film thickness [15]. By itself, fabrication of functioning n- and p-channel MOSFET devices with gate oxides as thin as 3.5 nm does not appear to present special problems [16,17]. The requirement of a maximum tolerable leakage current puts the lower limit of SiO_2 thickness for a corresponding DRAM technology near 4 nm [18]. However, thickness and uniformity of the films in this thickness range are strongly dependent on the details of the growth technology. Developments in recent years were concerned with the following three aspects of film growth: preparation of the silicon surface for growth; minimizing the level of contamination; improving the properties of the $Si–SiO_2$ system by means of small concentrations of additives.

The goal of the substrate preparation technique is the removal of a thin (a few nm) layer of silicon by wet chemical oxidation and etching of the resulting oxide film in order to remove surface damage, particulate matter and contaminants, particularly metals. These factors, as well as rough surfaces, lead to films with reduced breakdown strength [19, 20]. Exposure to HF vapor or to an aqueous solution of HF as the final step in surface preparation will result in a hydrogen-terminated Si surface, which by heating in neutral ambients is turned into an extremely reactive 'naked' Si surface. In the presence of hydrocarbons this will lead to the formation of SiC, which affects the quality of the subsequently grown oxide [21].

Covering the substrate by a wet chemically prepared oxide film provides a well-defined starting point for the subsequent thermal oxidation and consequently for the growth of a film of uniform thickness and optimum properties.

High demands are being put on the purity of chemicals and gases used in this process. From the point of view of control the use of a closed system for surface preparation, oxidation and poly-silicon gate deposition, i.e. for the preparation of a sealed gate system, looks very attractive [19]. However, definite proof of the advantages of this cluster tool approach still has to be produced.

The region in the SiO_2 film close to the Si substrate, where the oxide network joins the crystalline semiconductors, is the site of strain and defects. It may be expected that incorporation of impurities in the Si–O ring structure may lead to strain relief and chemical saturation of the oxide structure. With this goal in mind the effect of addition of small amounts of nitrogen and fluorine on the oxide has been extensively studied in recent years.

Nitrogen-doped oxides are prepared by oxidation in N_2O/O_2, annealing in N_2O [22], annealing in NH_3 and O_2 [23], or N-implantation in the poly-Si gate followed by annealing [24]. Such low-N-doped oxides improve the resistance of the gate system to hot carrier degradation of the MOSFET characteristics and extend the number of write–erase cycles in FLOTOX memory devices [25]. Moreover, the outdiffusion of B from the poly-Si gate is markedly suppressed. N-doped oxides also slow down the diffusion of H, which plays a role in the hot carrier induced generation of interface states [14].

Whereas N-incorporation most likely takes place in the Si–O ring structure, providing additional flexibility to the network, the role of F is probably to chemically stabilize broken-up ring structures. Implantation into the poly-Si gate appears to be a practical way of introducing the F dopant into the oxide for thin oxide MOS-structures [26, 27]. Again charge trapping and the generation of interface states are suppressed. Only very low concentrations (approximately 10^{13} cm^{-2}) are necessary to reach these goals [28].

6. Insulators in other semiconductor technologies

Suitable materials for masking, capping, surface passivation and interconnection isolation have been found for most semiconductor technologies. However, for the most critical application, that of gate dielectric, this is not the case.

We first consider oxides obtained by thermal oxidation of the semiconductor. The thermally grown oxide of Ge has a tendency to be oxygen-deficient; this is also the case at the interface. Consequently, the Ge–Ge–oxide system has a large density of interface states and exhibits pronounced

carrier capture in the insulator [29]. When attempting to prepare a semiconductor insulator system on SiGe alloy, one is confronted with the same problems as encountered in Ge-technology. In the thermal oxidation process Ge tends to be rejected [29]. A study of Ge-implanted SiO_2 shows that Ge, if incorporated into the oxide, traps one electron per Ge-atom [30]. Oxidation of III–V or II–VI semiconductors presents basically the same problems as that of SiGe: one of the components is preferentially consumed or incompletely oxidized, with attendant electrically active oxide defects and high concentrations of interface states.

CVD insulator films (like SiO_2) in combination with annealing treatments have led in some cases to acceptable interface state densities but not to low bulk trapping levels. In recent years the idea of using an epitaxially grown wider gap semiconductor layer has been borrowed from HEMT (high electron mobility transistor) technology. This layer should be sufficiently thick to prevent tunneling of carriers. A conventional large gap insulator could be added on but the electrical stability of these configurations remains to be proven [31].

7. Features of the ideal semiconductor–insulator system

Next, we will attempt to define the characteristics of the ideal insulator for field effect gate and storage capacitor application. For the gate insulator the density of traps in the bulk of the material and at its interface with the semiconductor should be as low as possible. To reduce carrier injection the material should have a wide band gap. The requirement of low defect density would be ideally fulfilled in crystalline materials. To obtain also a perfect interface the insulator should be grown epitaxially on the substrate. In practice, it turns out that such an insulator–semiconductor combination is very rare occurrence. The results on the one system which has been studied fairly extensively, CaF_2 grown with 0.6% mismatch on (1 0 0) Si, have not been encouraging [32].

An alternative would be the growth of a vitreous insulator on the semiconductor. Vitreous materials are covalently bonded and exhibit considerable flexibility in their structure. For this reason they should be able to provide a low defect density interface. A prime example of this case is the Si–SiO_2 system. SiO_2 is a vitreous material which shows nearly perfect short range order determined by chemically saturated SiO_4 building blocks. Their flexible structure allows the formation of Si–O rings of different sizes [33, 34] which provides a good fit and minimizes the strain near the Si–SiO_2 interface. This explains why in the absence of hydrogen passivation defect densities as low as a few times 10^{11} cm^{-2} are obtained [35].

Covalent bonding as required for vitreous materials generally occurs between non-metals which do not differ too much in electronegativity. These conditions and that of a sufficient band gap are met by the elements on the upper right-hand side of the periodic table. In addition to SiO_2, typical vitreous materials are Si_3N_4 (which has a rather high electrically active defect density) and the chalcogenides like As_2S_3 (which has a relatively narrow band gap). Consideration of the vitreous insulators thus does not leave us with many additional choices. These considerations indicate that for MISFET gate applications an optimized SiO_2 film still provides the best option for control and reliability. For capacitor dielectrics the defect structure of the interface is of lesser importance. The prime requirements are high dielectric constant and low leakage, i.e. sufficiently large band gap. Since these two features generally do not go together, one will have to compromise on band gap. This compromise turns out to be unproblematic, since a high dielectric constant allows the use of reduced fields in the insulator. It turns out that oxides present a favorable compromise [36]. It should be pointed out that in using polycrystalline materials conduction along grain boundaries may present a problem and will require special attention. However, in contrast to the application for the gate system the use of alternative dielectrics for capacitors appears feasible and worth further consideration.

8. Alternative dielectrics for capacitors

Notwithstanding the use of trenches, stacked layers and structured surfaces Mbit DRAMs