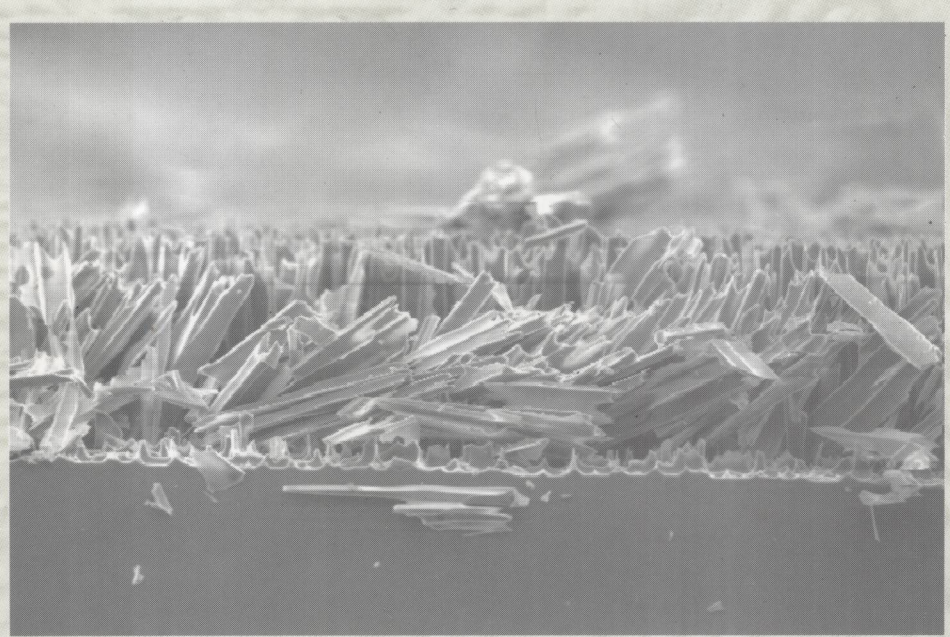
Thin Films and Porous Materials



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Thin Films and Porous Materials

Selected, peer reviewed papers from the first International Conference on Thin Films and Porous Materials, "ICTFPM'08", Organized in Algiers on May 19 to 22, 2008

Edited by:

N. Gabouze

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Preface

The first **I**nternational **C**onference on **T**hin **F**ilms and **P**orous **M**aterials (***ICTFPM'08***) was held in Algiers, Algeria, on 19-22 May 2008. The ***ICTFPM'08*** was organized by the Silicon Technology Development Unit, in close cooperation with the Algerian Ministry of higher Education and Scientific Research. The venue of this conference was ideally located in very nice town of "Zeralda" located at 25 Km from Algiers city.

This special series of ***Materials Science Forum*** contains a selection of the papers presented at the ICTFPM 2008 conference. The major goal of the conference was to give opportunity for professionals within academic research and companies to meet together and take part in recent scientific finding, current challenges and opportunities in the promising field of porous materials and thin films. We were delighted that 250 participants were present at the conference in "Zeralda". They were grouped mainly from Africa (Maghrebian) countries and European Union countries, but also from United States of America and Asia (especially from Japan). The scientific programme of the ICTFPM 08 was organized by a local committee with the assistance of Dr R. Boukherroub from the IEMN – Lille, France

The conference program consisted of 16 invited talks, 40 others oral contributions and 130 poster presentations. The conference programme was divided in twelve (12) sessions; the topics are listed as follows:

1. ***Advances in Deposition Techniques***
2. ***Characterization of Thin Films***
3. ***Functionalization and Surface Modification***
4. ***Magnetic Thin Films and Multilayers***
5. ***Nanotechnology and NanoStructured Materials***
6. ***New approach in Thin Films***
7. ***Organic Thin Films (polymers, biomolecules, alkyl…)***
8. ***Porous Materials and Applications***
9. ***Physics and Chemistry of Thin Films and Interfaces***
10. ***Single and Multilayer-based devices (Sensors, Photovoltaic, Optoelectronic)***
11. ***Technique Growth and Applications on Thin Films***
12. ***Thin Films and photonics application***
13. ***Thin Films Related Environment Devices***
14. ***New Materials: Modelling and Simulation***

We have selected a representative part of the papers based on the presentations given at the ICTFPM 2008 conference for this special issue of ***Material Science Forum***. As guest Editor I accepted opinions of the referees and selection took into account the scientific originality of the papers.

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Nanocrystal non-volatile memory devices

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Abstract. The physical background and present status of the application of metal-insulator-silicon structures with semiconductor nanocrystals embedded in the insulator layer for memory purposes is breafly summarized.

Introduction

Two kind of semiconductor nanocrystal structures are studied recently for non-volatile memory purposes. Ones of them are metal-insulator-semiconductor (MIS) structures containing semiconductor nanocrystals in the insulator layer, where nanocrystals serve as charge storage media replacing a floating gate in conventional memory field effect transistors (FETs) [1]. The other ones are the phase-change memory structures, where the channel layer itself is switched between nanocrystalline or amorphous state with high and low conductivity, respectively [2]. The goal of these studies is to overcome the difficulties of floating gate non-volatile memory devices (used e.g. in flash memories), which are connected with technology scale-down. MIS structures with embedded semiconductor nanocrystals are also studied for developing Si-based laser and light emitting diodes (LEDs) [1].

So - although related MIS structures can be prepared on any semiconductor substrate - silicon based structures are the most important ones for the technological development. In this paper the physical background, the preparation methods and the application of the MIS structures with semiconductor nanocrystals for non-volatile memory devices are briefly summarized.

Non-volatile MIS memory devices

Non-volatile memories are a group of memories, which hold the information without supplying power. Nowadays the most frequently used non-volatile memories are the Electrically Programmable Read Only Memories (EPROMs), the Electrically Erasable Programmable Read Only Memories (EEPROMs) and flash memories. The newest and most dinamically developing memories (used e.g. in mobile phones, pen drives, MP3 players, digital cameras, pocket computers, hybrid hard disks, etc.) are flash memories, which join the advantages of all other non-volatile memories, namely they are of high density, updateable, electrically erasable, relatively fast, and reliable [3]. The main difference between EEPROMS and flash memories is in the organization of memory arrays. In EEPROMs memory cells are erased one by one, while in flash memories by blocks using a "flash", i.e., a common erasing voltage pulse.

Information storage in non-volatile memories are based on changing the threshold voltage of FETs by appropriate voltage pulses. The actual mechanism is injection of charge by tunneling and its storage in a floating gate (see Fig. 1), or in traps in metal-nitride-oxide-semiconductor (MNOS) [4] (see Fig. 2) or silicon-oxide-nitride-oxide-silicon (SONOS) [5] devices located in the nitride layer close to the Si/Si_3N_4 interface.

The main characteristics of memory transistors are the amplitude and width (duration) of writing/erasing (W/E) voltage pulses, the width of the memory window (the difference between the threshold voltage for low and high state), the endurance (number of W/E cycles before degradation), and the retention (rate of threshold voltage change due to loss of the stored charge) properties. Requirements for fast writing and erasing with low pulse amplitudes are in contradiction with the requirements for high memory window widht and good retention behaviour.

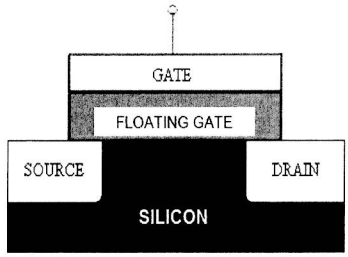

Fig. 1: The floating gate memory FET

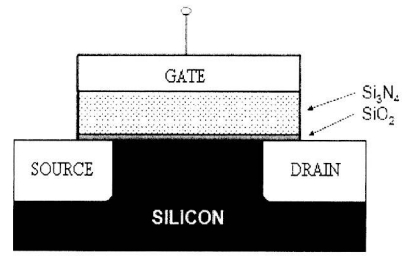

Fig. 2: The MNOS memory transistor

The reduction of dimensions is limited in these devices mainly due to reliabity problems connected with defects in the thin oxide layer below the floating gate (tunnel oxide). The main problem is that through defects or weak points in tunnel oxide with reduced thickness the whole amount of stored charge carrying the information can be lost.

The other problem of floating gate devices is the drain turn-on effect [6]. It is connected with strong capacitive coupling between the drain and floating gate and between the source and floating gate. So, if the drain voltage is increased, the potential of floating gate increases as well, and the drain current does not saturate.

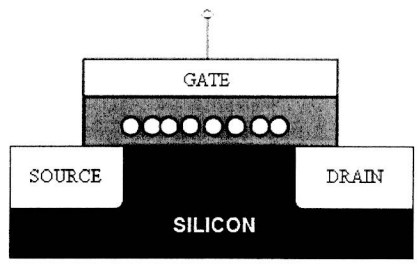

Fig. 3: The nanocrystal memory transistor

One of the possible solutions is to replace floating gate with separated semiconductor nanocrystals (NCs) [7], which are electrically isolated, as shown schematically in Fig. 3. In this case the loss of information via local defects can be avoided, and the drain turn-on effect is strongly reduced as well [6].

Another possible way to avoid the above difficulties is the application of SONOS or MNOS devices. In these structures the charge holding the information is stored in the traps of nitride layer, which are electrically isolated by their nature. So, both the effect of local defects and strong capacitive coupling are reduced significantly [6,8]. Further on, if using Si_3N_4, as an upper insulator layer (control layer), due to its higher dielectric constant, higher electric field will be developed in the tunnel oxide for the same layer thicknesses and voltage pulses, than for a SiO_2 control layer [9]. The higher electric field enhances the charge injection. This is another advantage of using Si_3N_4, as a control layer. However, this is partly compensated or even overcompensated - depending on the tunnel oxide thickness - by the higher conductivity of Si_3N_4 due to traps yielding Poole-Frenkel current [4]. So, SONOS structures are prepared with thin tunnel oxide layers [8]. Another disadvantage of nitride based memories is that the energy level of traps is shallower (1-2 eV), than the energy levels in nanocrystals (about 3 eV), which yields faster retention behaviour of nitride based structures [8].

A third altenative way to solve the above difficulties is the application of phase change memories mentioned above, which are scalable and fast, and require low writing/erasing (W/E) pulse amplitudes [10].

In addition to non-volatile memories, nanocrystal memory structures are also studied for dinamic random access memory (DRAM) purposes. The goal of this research is to decrease the lateral dimensions and the refresh frequency [8].

Preparation of MIS structures with embedded semiconductor nanocrystals

The most common MIS structure used for both memory and LED purpuses is the metal or poly-$Si/SiO_x/Si$ structure with Si nanocrystals embedded in the SiO_x layer. As dielectric matrix, Al_2O_3 or stacked dielectrics are also used. Ge and SiGe nanocrystals are also often formed. For LED purpuses the effect of different compound semiconductor (GaSb, CdS, CdSe, CdTe, SiC, PbS) nanocrystals is widely studied as well, but in polymer structures mainly. Metal crystallites have also been applied in some cases [11].

MIS structures with embedded semiconductor nanocrystals are prepared by four main methods. The most frequently used method is the ion beam synthesis, which means implantation of Si or Ge into SiO_x layer and subsequent annealing (or oxidation) at high temperatures [12-14]. Another method is a layer by layer growth, i. e., the deposition of a thin amorphous or polycrystalline Si or Ge layer onto a lower dielectric layer. This Si or Ge layer is either covered by another dielectric layer, or the Si grains themselves are oxidized. The nanocrystals are formed by annealing either during evaporation or after the deposition of the Si or Ge layer, or after the deposition of the second dielectric layer [15-17]. The third method is the deposition of a Si-rich or Ge-containing SiO_x layer, and formation of nanocrystals within the SiO_x layer by high temperature annealing [18-20]. The fourth, most recent method is the deposition of Si nanocrystals themselves or of a SiN_x layer containing Si nanocrystals by different chemical vapour depositon (CVD) methods without postdeposition annealing [8,9,21].

Non-volatile memory devices with embedded Si nanocrystals

Recent results published on memory devices with Si nanocrystals prepared by ultra-low-energy ion-beam synthesis are very promising [12,13]. This method involves an ion implantation at low energies and one or two subsequent annealing steps at high temperatures. Normand et al. performed implantation in the range of 0.5-2 keV [12]. Optimazing the preparation conditions, memory transistors with the following characteristics were achieved. About 2 V memory window width was obtained for W/E pulses of ±9 V, 10 ms. No change of the memory window was detected after 1.5 million W/E cycles. The estimated memory window of unstressed devices kept at 85 °C is 0.4 V after 10 years, the stressed devices also store the information for several years [12,22].

Ng and coworkers [13] performed implantation at energy of 2 keV. The tunneling oxide thickness was 3 nm or 7 nm for realization of direct or Fowler-Nordheim tunneling during the charging process. For direct tunneling they obtained a memory window width of about 1 V using charging pulses of ±12 V, 1 μs, while for Fowler-Nordheim tunneling the memory window width was about 0.5 V using charging pulses of ±12 V, 1 ms. So, devices with the thicker tunnel layer required much longer charging pulses, and they degraded faster as well. However, the extrapolated for 10 years memory window width was about 0.3 V at 85 °C for both type of structures.

Schmidt and co-workers performed Si implantation at 50 keV yielding ion mixing at the Si/SiO_2 interfaces. Memory window of about 0.5 V for W/E voltage pulses of ±7 V, 10 ms was obtained for implanted fluence of $(5–7)\cdot10^{15}$ Si^+ cm^{-2} and annealing at 1050 °C for 30 s [23,24]. The memory window increased by annealing at higher temperatures (1100 °C) and/or for longer duration (over 120 s) up to about 3 V. No degradation in memory windows was observed for devices after 10^7 W/E cycles with programming conditions ±7V, 1 ms. However. retention time was 100 days at room temperature and 8 h at 85 °C, which is too low for non-volatile purposes, but is good for DRAM applications.

Lu et al. prepared different memory structures containing one-three Si NC layers using evaporation of SiO powder by layer by layer growth [25-27]. They studied the charging behaviour of the structures by C-V measurements. In structures with two or three NC layers two or three different saturation levels of flat-band voltage shift were obtained with increasing bias, which correspond to charge injection to and capture at the first, second, or third NC layer [26]. Charge captured in the first layer yielded a flat-band voltage shift of about 2.5 V, charge captured in the second NC layer yielded an additional flat-band voltage shift of about 2.5 V, while charge captured in the third layer yielded an additional shift of about 1.5 V, according to different depth of NC layers from the Si surface. A good correlation was also obtained between NC density and the density of stored charge (flat-band voltage shift) [25,27]. The multilayer storage yielded very good retention as well [26].

Another successful method for creating nanocrystals for memory applications is the chemical vapour deposition. Rao and co-workers used low pressure CVD (LPCVD) for device preparation for non-volatile purposes using tunnel oxides with thickness 3.8-5.0 nm, respectively [8]. They obtained about 1.5 V of threshold voltage shift by voltage pulses of 14 V, 100 μs or 12V, 1ms. Retention characteristics were also very good, but the memory window shifted slightly with increasing number of W/E cycles.

They also studied the effect of NC density and size on the charging and retention behaviour [28]. It was obtained that writing as well as erasing characteristics were influenced by both the NC density and size due to the effective capture cross section and Coulomb blockade, respectively. Nevertheless, statistical studies performed on 4 Mbit NC memory arrays showed that these effects do not disturb the memory characteristics significantly over a wide range.

It is worth mentioning that on the basis of these experiments a 4 Mbit nanocrystal flash memory array was introduced in production in 2003, and a 24 Mbit array in 2005 [29].

Non-volatile memory devices with embedded Ge nanocrystals

Duguay and co-workers studied memory structures containing Ge NCs prepared by implantation with doses of $1 \cdot 10^{16}$ cm^{-2} and $2 \cdot 10^{16}$ cm^{-2} and energies 13-17 keV into 30 nm thick SiO_2 [30]. They obtained the best performance for the dose $2 \cdot 10^{16}$ cm^{-2} and energy 13 keV [30]. A memory window width of about 1.5 V was obtained for charging pulses of ±6 V, 6 ms. However, the retention time was estimated at about 28 hours [31].

Hong et al. deposited self-assembled Ge NCs on the top of 3 nm tunneling SiO_2 by sputtering in Ar^+ plasma at room temperature, which were covered by a 20 nm control SiO_2 layer [32]. The effect of Ge amount was studied on the memory behaviour from 18 to 54 momolayers. As a general picture, both charging and retention behaviour became better with increasing amount of Ge in the studied range. The NC size increased, but NC density decreased with increasing Ge amount: NC densities of $(2\text{-}5) \cdot 10^{12}$ cm^{-2} and NC sizes of 2-6 nm were obtained. So, as the NC size was small, the dependence of memory behaviour on Ge amount was connected with quantum confiment. A memory window width of about 3.5 V was obtained for writing pulse of +7 V, 1 ms and erasing pulse of -9 V, 1 ms.

Wang and co-workers embedded Ge NCs between a 5 nm thick HfAlO tunnel oxide deposited on the nitrided Si surface and a 8 nm thick HfAlO control oxide [33]. They obtained a memory window width of 2.2 V for charging pulses ±12 V, 100 ms.

Choi and co-workers prepared Ge NCs on a stacked tunnel layer of $LaAlO_3$ and SiO_2 [34]. The structure consisted of a 3.7 nm thick thermal SiO_2 layer, a 1 nm thick $LaAlO_3$ layer, a sheet of Ge NCs prepared by evaporation and annealing, and a control $LaAlO_3$ layer with a thickness of 13 nm. A reference structure without the lower $LaAlO_3$ layer was also studied. The memory window width was about 2 V and 1.8 V, respectively, for the charging pulse of ±5 V, 100 ms. The structure with stacked tunnel layer exhibited negligible degradation up to 10^4 W/E cycles, while the memory window of the reference structure shifted with increasing number of W/E cycles. There was a significant difference in retention behaviour as well. While in the structure with the stacked

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tunnel layer 60% of the stored charge is expected to be retained after 10 years, the reference structure lost it within 15 min.

Li and co-workers prepared memory FETs with Ge/Si NCs by LPCVD [35]. The tunnel oxide was 5 nm thick, the control oxide 25 nm. The obtained NC density was about $5 \cdot 10^{11}$ cm^{-2}. They compared the memory properties of Ge/Si NC devices with those of reference Si NC FETs. Writing and retention behaviour for Ge/Si NC devices were better, than for Si NC devices. The obtained memory window width for Ge/Si NC devices was about 1 V for charging pulses ±15 V, 2 ms. The endurance behaviour was similar: both structures begin degrade over 10^5 W/E cycles.

Silicon nitride based memory structures with embedded Si or Ge nanocrystals

Our group realized that formation of NCs in nitride based memory structures can enhance both the charging and retention behaviour due to making direct tunneling possible to NCs and creating deep energy states, respectively [9,36]. So, our idea was to create MNOS structures with semiconductor NCs at the Si_3N_4/SiO_2 interface.

First MNS (metal-nitride-semiconductor) structures were studied with embedded Si NCs [36]. The structures were prepared by LPCVD at 810-830 °C in three steps. First a 15 nm thick stochiometric Si_3N_4 tunnel layer was deposited using NH_3 and SiH_2Cl_2, followed with a Si NC layer grown from SiH_2Cl_2 only, then another stochiometric Si_3N_4 layer was prepared with a thickness of 32 nm [36]. The effect of duration of Si NC deposition was studied on their size and on the memory behaviour in the range of 0-120 s (samples NI000-NI120, respectively - see Table 1).

Table 1: The Si nanocrystal deposition duration, the initial memory window width, its extrapolated values for 1 and 10 years, and the retention time for the studied MNS and MNOS structures for writing/erasing voltage pulses of ±15 V, 10 ms [37].

Sample No.	NC deposition duration (s)	Initial memory window width (V)	Memory window width after 1 year (V)	Memory window width after 10 years (V)	Retention time (years)
NI000	0	5.80	0	0	0.564
NI030	30	4.59	0	0	0.091
NI045	45	4.16	0	0	0.050
NI060	60	2.06	0	0	0.075
COA00	0	5.34	0.87	0.46	128.290
COA30	30	6.61	0.85	0.32	41.190
COA60	60	6.68	0.47	0	7.370

The obtained thickness of NC layer depended on the deposition duration and changed from 2 nm to 13 nm. Deposition up to 60 s yielded well separated Si NCs with the size up to 7-8 nm, while deposition for 120 s resulted in a continious network of NCs [36].

The effect of NCs on memory properties was just opposite, than it was expected: the memory window shrinked with increasing duration of NC deposition, as presented in Table 1 [36,37]. This can be explained as follows. A part of injected charge is stored in nitride traps and the other part in NCs. Let us consider that the centroid of charge trapped in nitride is closer to the Si/Si_3N_4 interface, than NCs, which are at a depth of 15 nm in our case. For the same amount of stored charge, the higher part trapped in NCs, the lower is the flat-band voltage shift. On the other hand, the development of the same electric field for injecting charge of opposite sign also requires higher pulse amplitude, if higher part of the trapped charge is stored in NCs [37].

The retention depended on the charging pulse amplitude and width, which also indicates charge storage in both nitride traps and NCs. For high pulse ampitudes and widths (±20 V, 400 ms) no significant difference was found between retention behaviour of samples for deposition duration

0-60 s. But the sample with deposition duration of 120 s exhibited much higher retention rate due to the continous layer of NCs [36]. For short charging pulses (±15 V, 10 ms) the retention time (the extrapolated time corresponding to the disapparence of memory window) was much shorter for structures with NCs (0.05-0.09 year), than for the reference sample without NCs (0.56 year), as presented in Table 1 [37].

A systematic study of MNOS structures with embedded Si NCs was carried out as well [9]. The effects of tunnel oxide deposition method and of NC depositon duration were studied. For the tunnel layer two chemical and a thermal SiO_2 layers were prepared. Chemical SiO_2 layers were grown using HNO_3 treatments at different conditions yielding 2.5 nm and 4.5-5.0 nm thick films [9, 38]. The third oxide layer was grown thermally with a thickness of 4.2 nm [9]. The Si NCs and Si_3N_4 control layers (the latter with a thickness of 40 nm) were grown by a similar way, as in MNS structures described above. The duration of Si NC deposition was in the range 0-60 s (samples COA00-COA60, respectively). The best memory behaviour was obtained for the thinner chemical tunnel layer [9]. The injection properties enhanced with longer NC deposition duration, as it is presented in Table 1. This is connected with the increasing tunneling probability of charge carriers via Si NCs.

However, the retention behaviour became worse with increasing NC deposition duration, as presented in Table 1 for charging pulses of ±15 V, 10 ms [37,39]. It is striking that MNOS structures exhibited much longer retention time for short charging pulses, than MNS structures (see Table 1), while for long pulses (400 ms) their retention behaviour was similar [9]. This indicates that during short pulses NCs and nitride traps close to the Si/SiO_2 interface are filled by carriers, while during longer pulses the charge is escaped also by traps located deeper in the nitride layer.

Table 2: Ge nanocrystal deposition duration, memory window width of the studied MNOS structures with Ge nanocrystals for different charging pulse amplitude with duration of 100 ms, and its value in 1 and 10 years after applying voltage pulses of ±25 V, 100 ms.

Treatment	Deposition duration (s)	Applied voltage pulse amplitude (V)				Memory window width (V) after	
		10	15	20	25	1 year	10 years
HNO_3	–	0.6	1.9	4.7	10.9	1.18	0.13
	25	1.3	3.5	7.5	14.5	0.96	0
	50	0.8	2.1	5.5	11.8	1.43	0.33
$H_2SO_4 + H_2O_2$	–	0.7	1.7	4.3	10.5	0.92	0
	25	0.8	2.1	4.9	11.2	1.17	0.07
	50	0.9	2.0	4.8	11.1	1.2	0.14

In addition to structures with Si NCs, MNOS structures with embedded Ge NCs were also examined. The effects of tunnel oxide preparation (HNO_3 [9,37] versus H_2SO_4+H_2O_2 [40] treatment) and of duration of Ge NC deposition were studied as well. The thickness of the tunnel and control layers was about 2.5 nm and 75 nm, respectively. Ge nanocrystals were deposited between the two layers by electron beam evaporation at 350 °C [16]. Reference devices without any Ge nanocrystal layers were also prepared.

Good charging behaviour was obtained, as presented in Table 2 for devices with different parameters. The retention behaviour was also acceptable for some devices, as presented in Table 2 as well. It is seen that the HNO_3 treatment yielded better injection as well as retention behaviours, than H_2SO_4+H_2O_2 treatment. On the other hand, in the case of HNO_3 treatment both injection and retention performances of the sample with deposition duration of 50 s is better, than that for reference sample without NCs. This is the case for both NC structures with H_2SO_4+H_2O_2 treatment.

Summary

For solving problems connected with technology scale-down in MIS non-volatile memories three alternative ways seem to be prespective, namely the application of nanocrystal or silicon nitride based MIS structures as well, as phase change memory structures.

MIS nanocrystal memory structures are prepared by four main methods, namely, by ion beam synthesis, by layer by layer growth, from a dielectric layer with excess Si or Ge, and by direct chemical vapour deposition. Except the last method, the nanocrystals are formed by annealing either during or after the deposition.

Silicon nitride based memory structures with embedded semiconductor nanocrystals can merge the advantages of nitride based and nanocrystal memory structures.

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