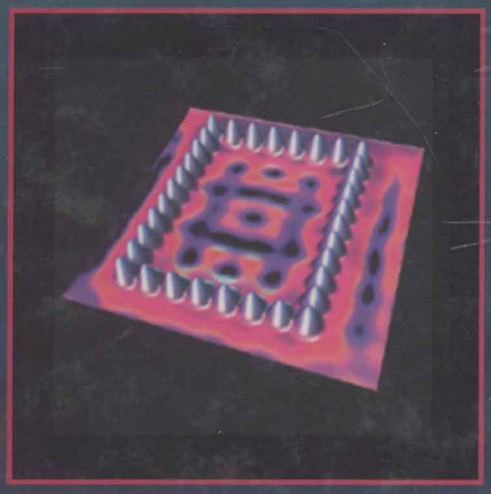
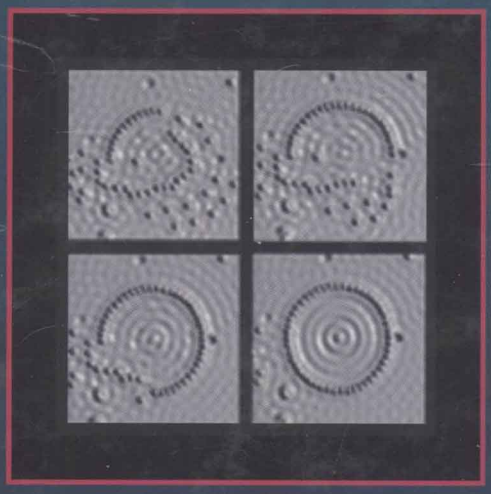
Microfabrication AND Nanomanufacturing





Edited by Mark J. Jackson

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Preface

Currently, the development of products at the nano- and microscale is being driven by economic necessity in highly developed countries in order to improve the quality of life, and in recent years to prevent the spread of global terrorism. Nanotechnology is seen as the next step in the industrial revolution and, as such, requires manufacturing processes that will revolutionize the way small products are made. The promises offered by nanotechnology will change the way we exist. The challenges for engineers and scientists are manifest in the construction of products at such small scales, which has been the preserve of Mother Nature since the creation of the universe.

This book is concerned with the technology of fabrication and manufacturing of engineering materials at the micro- and nanoscale. Chapter 1 sets the scene for these challenges and gives a brief overview of techniques used in the semiconductor industry for constructing electronic circuits and provides clues for scaling manufacturing processes to operate at the nanoscale for nonsemiconductor applications. The construction of microscale components using established lithographic techniques is described in Chapter 2. In this chapter, the x-ray lithographic technique for forming microscale components is described, including examples of using LiGA and deep x-ray lithography to fabricate master molds that are subsequently used to manufacture microscale and nanoscale products.

Chapter 3 focuses on bulk and surface micromachining techniques that are used for producing features such as trenches using etching, machining, and molding procedures. Manufacturing techniques such as injection molding and hot embossing, in which polymeric materials are shaped to economically produce masses of micro- and nanoscale products are also described. The fabrication of master molds for subsequent operations such as molding can also be made from engineering materials and not just silicon. These processes are described in Chapters 4 through 6. Here, the effects of machining at the microscale are introduced for products such as dies and molds and for biomedical products such as micro- and nanofluidic devices made from stainless steels and biocompatible alloys. Substrates of these materials are flat and require grinding techniques to produce the required flatness tolerances. Small-scale features are then created from the bulk material by removing small portions of the material from the surface using micromilling processes. These require specially developed cutting tools that are produced using physical and chemical vapor deposition techniques. Chapter 7 introduces the reader to the deposition of thin solid films to the surfaces of such tools.

Nontraditional micro- and nanoscale processing procedures are described in Chapters 8 and 9, including a newly developed technique called pulsed water jet machining. This technique uses the power of water to machine materials at the microscale and has been shown to work on silicon-based materials. The efficient removal of materials using optical energy is shown in Chapter 9, which provides an understanding on how lasers are being developed and used to machine materials at the micro- and nanoscales.

The latter chapters lead to an interesting conclusion. The development of nanoscale processes for producing products other than semiconductors is explored in Chapters 10 through 12. The use of abrasive particles embedded in a porous tool is discussed in Chapter 10. The bonding of the embedded tool to a piezoelectric oscillator is shown to improve the machining of materials at the nanoscale. The process of nanometric machining and the development of machine tools are provided in Chapter 11. The deposition and application of nanocrystalline diamond are explained in Chapter 12.

Chapter 13 is devoted to the promotion and commercialization of micro- and nanoscale products and explains how product-market issues will affect how micro- and nanoscale technologies are developed to meet demand and focuses on the infrastructure required to market these products. The final chapter, Chapter 14, provides an outlook on the future perspective of micro- and nanofabrication technologies and how they can be developed into nanomanufacturing processes.

The diversity of such a subject as micro- and nanomanufacturing requires specialists from a wide field of multidisciplinary expertise. I am grateful to all the contributors of this edited professional textbook.

M. J. Jackson
Editor
West Lafayette, Indiana

The Editor

Mark J. Jackson, Ph.D., is Associate Professor of Mechanical Engineering at Purdue University. He began his engineering career in 1983 when he studied for his O.N.C. part I examinations and his first-year apprenticeship-training course in mechanical engineering. After gaining his Ordinary National Diploma in Engineering with distinctions and I.C.I. prize for achievement, he read for a degree in mechanical and manufacturing engineering at Liverpool Polytechnic and spent periods in industry working for I.C.I. Pharmaceuticals, Unilever Industries, and Anglo Blackwells. After graduating with a Master of Engineering (M.Eng.) degree with Distinction under the supervision of Professor Jack Schofield, M.B.E., Dr. Jackson subsequently read for a Doctor of Philosophy (Ph.D.) degree at Liverpool in the field of materials engineering, focusing primarily on microstructure-property relationships in vitreous-bonded abrasive materials under the supervision of Professor Benjamin Mills.

He was subsequently employed by Unicorn Abrasives' Central Research & Development Laboratory (Saint-Gobain Abrasives' Group) as materials technologist and then as technical manager, responsible for product and new business development in Europe and university liaison projects concerned with abrasive process development. Dr. Jackson then became a research fellow at the Cavendish Laboratory, University of Cambridge, working with Professor John Field, O.B.E., F.R.S., on impact fracture and friction of diamond before becoming a lecturer in engineering at the University of Liverpool in 1998.

At Liverpool, Dr. Jackson established research in the field of micromachining using mechanical tools, laser beams, and abrasive particles. At Liverpool, he attracted a number of research grants concerned with developing innovative manufacturing processes for which he was jointly awarded an Innovative Manufacturing Technology Center from the Engineering and Physical Sciences Research Council in November 2001. In 2002, he became associate professor of mechanical engineering and faculty associate in the Center for Manufacturing Research and Center for Electric Power at Tennessee Technological University (an associated university of Oak Ridge National Laboratory) and a faculty associate at Oak Ridge National Laboratory. Dr. Jackson was the academic adviser to the Formula SAE Team at Tennessee Technological University.

In 2004, he moved to Purdue University as Associate Professor of Mechanical Engineering in the Department of Mechanical Engineering Technology. Dr. Jackson is active in research work concerned with understanding the properties of materials in the field of microscale metal cutting, micro- and nano-abrasive machining, and laser micromachining. He is also involved in developing next-generation manufacturing processes and biomedical engineering.

Dr. Jackson has directed, co-directed, and managed research grants funded by the Engineering and Physical Sciences Research Council, The Royal Society of London, The Royal Academy of Engineering (London), European Union, Ministry of Defense (London), Atomic Weapons Research Establishment, National Science Foundation, NASA, U.S. Department of Energy (through Oak Ridge National Laboratory), Y12 National Security Complex at Oak Ridge, Tennessee, and Industrial Companies, which has generated research income in excess of $10 million. Dr. Jackson has organized many conferences and currently serves as General Chair of the International Surface Engineering Congress. He has authored and co-authored over 150 publications in archived journals and refereed conference proceedings and is guest editor to a number of refereed journals. He is the editor of the newly established *International Journal of Nanomanufacturing*.

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INTRODUCTION

The semiconductor industry has grown rapidly in the past few decades, driven by the microelectronics revolution. The desire to place many transistors onto a silicon wafer has demanded innovative ways to fabricate electronic circuits and to fit more and more electronic devices into a smaller workable area. Early transistors were made from germanium but are now predominantly silicon, with the remainder being made from gallium arsenide. Although gallium arsenide has high electron mobility compared with silicon, it has low hole mobility, a poor thermal oxide, less stability during thermal processing, and a much higher defect density than silicon. Silicon has become the material of choice for most electronic applications, but gallium arsenide is useful for circuits that operate at high speeds with low to moderate levels of integration. This type of material is used for analog circuits operating at speeds in excess of 10^9 Hz. Increasing the performance of integrated circuits can be accomplished by placing transistors closer together and by depositing transistors in a precise way. The minimum feature size has been reduced at an astonishing rate over the past 30 years. Figure 1.1 shows the reduction in feature size from 10 μm to less than 350 nm using conventional lithographic techniques. Figure 1.2 shows a single strand of human hair and an array of transistors on a single piece of silicon, revealing the relative size of transistors that can be accommodated on a piece of silicon.

Microfabrication begins when a set of photomasks are provided to the integrated circuit fabricator. The photomasks are physical representations of the design of the circuits to be manufactured in accordance with the rules of layout. A silicon wafer provides the basis of the integrated circuit. Wafers are processed using a grinding process that produces a flat surface that is still conductive at this stage. The wafer is insulated by growing a thermal oxide layer to prevent

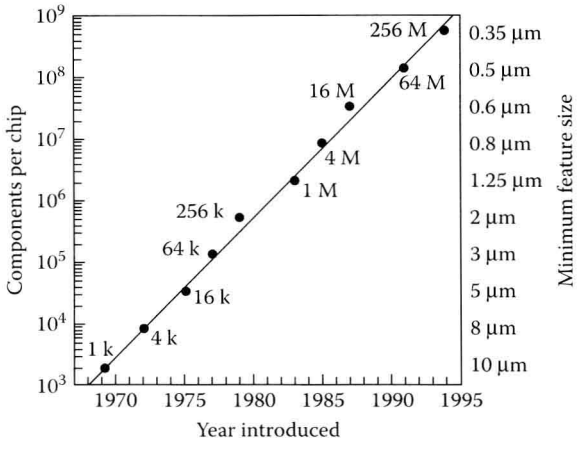

FIGURE 1.1 Memory and minimum feature sizes for dynamic random access memories as a function of time.[1]

leakage of current between transistors. A conducting layer is deposited that is used for producing transistors. Several techniques have been developed for depositing insulating and conducting layers, such as sputtering, physical vapor deposition using a magnetron, chemical vapor deposition (CVD), and epitaxial growth of layers using techniques such as metal oxide CVD, molecular beam epitaxy, and chemical beam epitaxy. The conducting layer is divided up into individual resistors. Individual resistors are deposited to the wafer by use of photolithographic techniques. Further processing is required to form the integrated circuit; this processing uses techniques such as pattern transfer, etching, deposition, and growth. These same techniques have also been used to create a plethora of microscale products in silicon-based materials for applications other than integrated circuits.

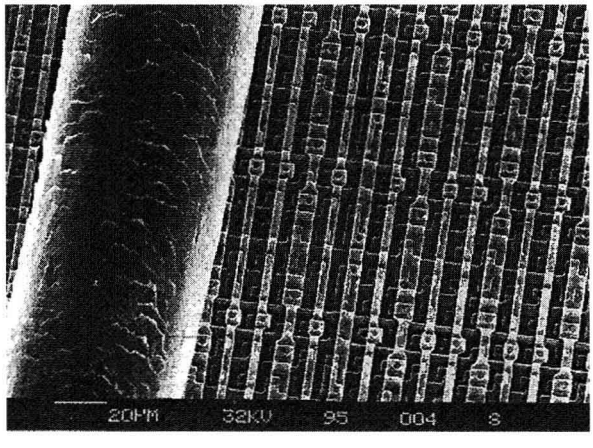

FIGURE 1.2 Scanning electron micrograph of an integrated circuit chip in the mid-1980s. The human hair to the left of the image provides an indication of the relative size of the transistor wires.[1]

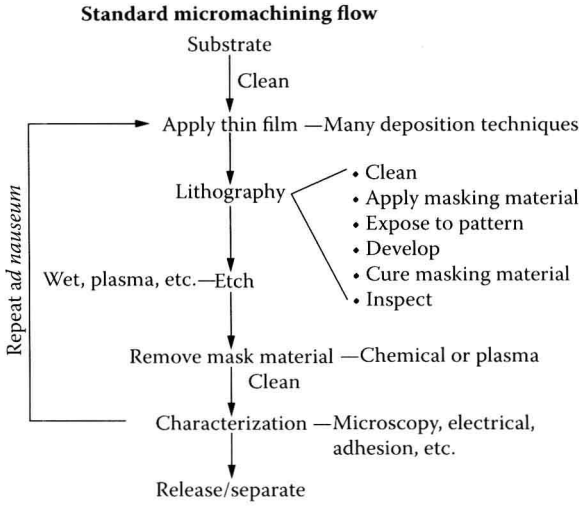

FIGURE 1.3 Standard micromachining flow chart. (Courtesy of ASME.)

MICROFABRICATION

Traditionally, integrated circuits have been manufactured by use of microfabrication techniques that have been classified as machining processes. Figure 1.3 shows the standard route followed to produce an integrated circuit. The same flowchart can be used for producing any microscale product made with silicon-based materials. The chart shows the basic functions of initially cleaning the substrate, applying a thin film using many deposition techniques, applying lithographic techniques to apply mask material, etching to form the required shape of the microscale features, removing the mask material using chemical or plasma etching, and finally characterizing the nature of the created structure.

The basics of microfabrication are shown in Figure 1.4, Figure 1.5, and Figure 1.6; fabrication at the microscale is made up of three basic regimes: addition, multiplication, and subtraction. The addition phase involves adding a thin film coating to the substrate material. This can take the form

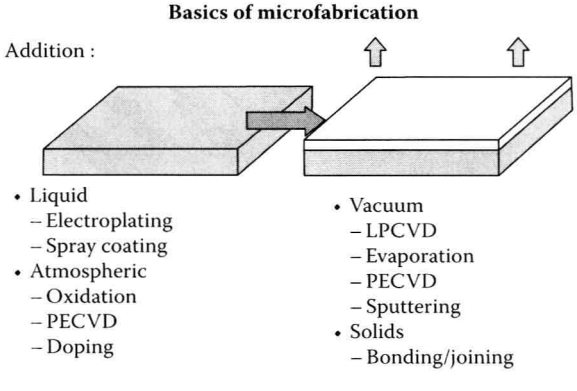

FIGURE 1.4 Microfabrication by the addition of a thin solid film. (Courtesy of ASME.)

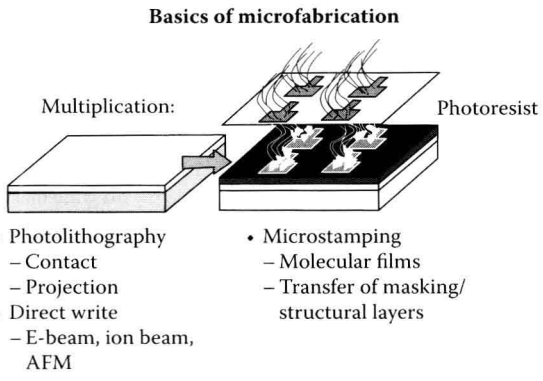

FIGURE 1.5 Microfabrication by the multiplication of a thin solid film. (Courtesy of ASME.)

of electroplating or spray coating a liquid film to the substrate and allowing it to dry; a thin film can also be created by oxidation or doping in an atmospheric chamber. Other methods include fusion bonding a solid to the substrate or using low- and high-pressure vacuum techniques to bond a thin coating to the substrate. The process of feature multiplication also takes many forms and is a process step necessary to create microscale features, particularly channeled features that are used in micro- and nanofluidic devices.

Multiplication of features can be performed with a number of processes such as direct writing of features using electron beam, ion beam, and atomic force microscopic techniques. Contact lithography is another popular technique for depositing features in addition to new methods of micro/nanoscale feature generation using microstamping processes. Subtraction of materials to create features can be accomplished with a variety of techniques, as shown in Figure 1.6. In materials other than silicon, subtraction processes can include mechanical micromilling, laser ablation, water micromachining, and a great number of other processes. These processes can remove materials at much higher material removal rates and are discussed further in subsequent chapters in this book.

Combinations of all of these techniques can be used to produce features of different size, shape, and scale. The standard way of creating features on single pieces of silicon is being

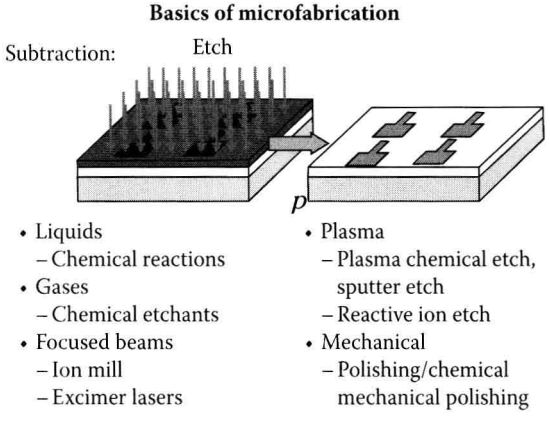

FIGURE 1.6 Microfabrication by the subtraction of parts of a thin solid film. (Courtesy of ASME.)

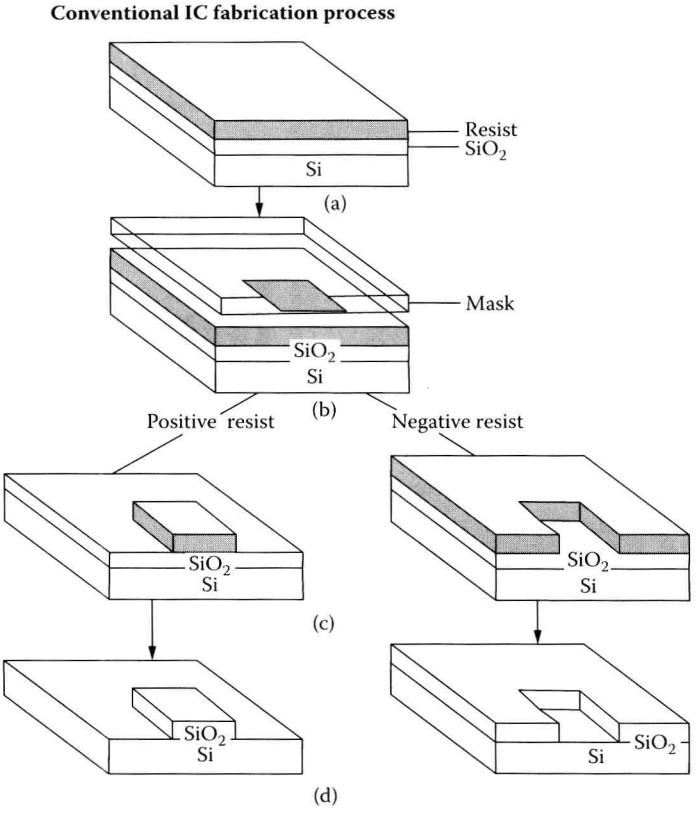

FIGURE 1.7 Typical fabrication process for an integrated circuit (IC). (Yeager, R.C., *Introduction to Microelectronic Fabrication, Modular Series on Solid State Devices*, Neudeck and Pierret, Eds., Vol. V, Addison Wesley Press, 1988.)

surpassed by new microfabrication processes that achieve improved performance of individual devices. The standard way of producing integrated circuits is shown in Figure 1.7. Figure 1.7 shows the process of depositing a thin film on the surface of silicon, which is selectively removed by etching processes that produce wells or channels with known geometry owing to the texture of the silicon crystal. The removal of silicon in certain directions of crystal planes is known as bulk micromachining.[2] Figure 1.8 shows the characteristic planes of silicon etched by using KOH etchant. The shape of the channel, or trench, produced is fixed by the way atoms are arranged in known directions.

The process of bulk micromachining to produce electronic devices such as capacitors is shown in Figure 1.9. Here, (a) the feature is cleaned to prepare the substrate for deposition of the mask, (b) the mask is etched using KOH etchant, and (c) the substrate is etched to produce a deep trench. Trenches for microfluidic devices made from silicon can be produced in this way, but the shape of the trench is controlled by the way atoms are arranged in crystallographic planes.

Another method used for bonding thin films to silicon substrates is fusion bonding. Figure 1.10 shows the basic principle used for bonding silicon on an insulator material to create a voltage-tunable, piezoelectrically transduced SCS resonator (Figure 1.11). Figure 1.11 shows the basic construction of the resonator and also shows how etching a thin ZnO film can create a Q-enhanced

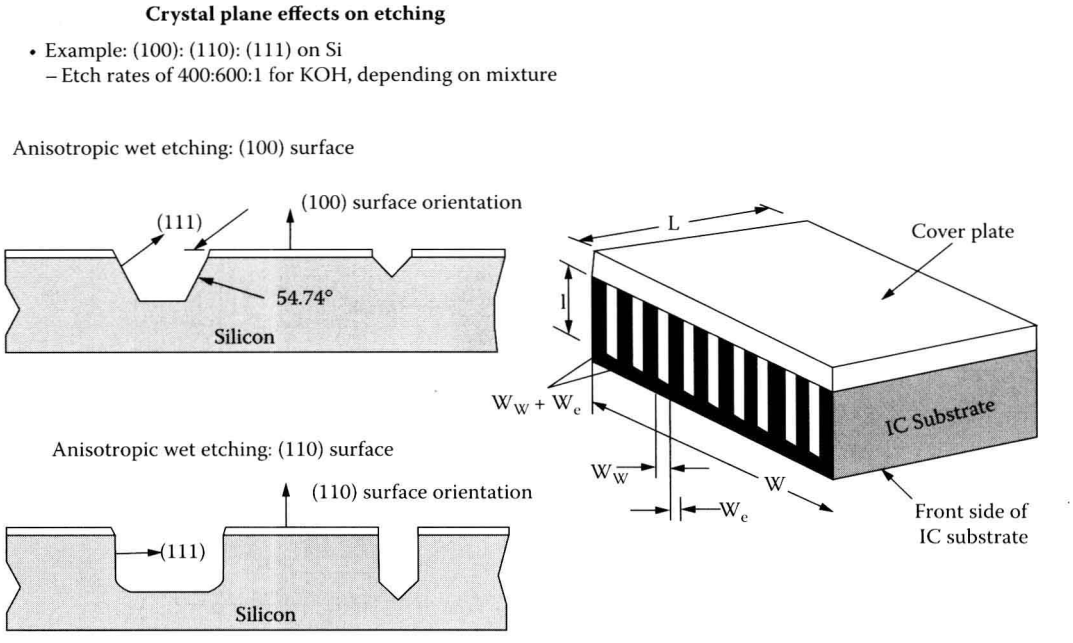

FIGURE 1.8 Crystal plane etching on (100), (110), and (111) planes of silicon using KOH etchant. The shape of the channel produced in silicon by bulk micromachining is shown. (Yeager, R.C., *Introduction to Microelectronic Fabrication, Modular Series on Solid State Devices*, Neudeck and Pierret, Eds., Vol. V, Addison Wesley Press, 1988.)

resonating device. This process can also be used for creating stepped features in microfluidic devices and other micromachined products.

The formation of the trench in the previous application can take a long time to produce when using wet etchants. One way of increasing the aspect ratio of a trench to make it deeper is to reactively ion etch the substrate to produce a deeper feature. The principle of this process is shown in Figure 1.12. The etching speed is typically 1 to 2 μm per minute, which is slow compared with micromilling and laser-based micromachining processes.

Deep reactive ion etching is a way of producing masters for manufacturing products on the mass scale. When coupled with micromolding techniques, a wide variety of microproducts can be produced. Deep reactive ion etching of deep trenches is used to produce tunable capacitors. Figure 1.13 shows such an application. This type of process is discussed in detail in Chapter 3.

In the field of nanofabrication, microfabrication processes can be used to make cantilever probes for atomic force microscopes that can be used for multiplying features on silicon and other materials by direct writing. This book explains how microfabrication techniques have been developed to produce single products through fabrication and also explains how multiple microproducts can be produced through manufacturing. An example of how microfabrication can produce nanofabrication tools is shown in Figure 1.14. A cantilever made from silicon and glass is etched to produce the features required to produce a probe for directly writing to the surface of the substrate (Figure 1.15). This type of cantilever can be used to produce nanofabricated features that are discussed at length in the next section.

During cantilever production, anisotropic etching is used to form the pit into the (100) surface of the silicon wafer. A silicon nitride film is deposited to the surface and fills the pit created by etching. The beam of the tip is prepared by using a glass plate from which the silicon is etched away to leave a silicon nitride cantilever beam that is connected to a metal block.

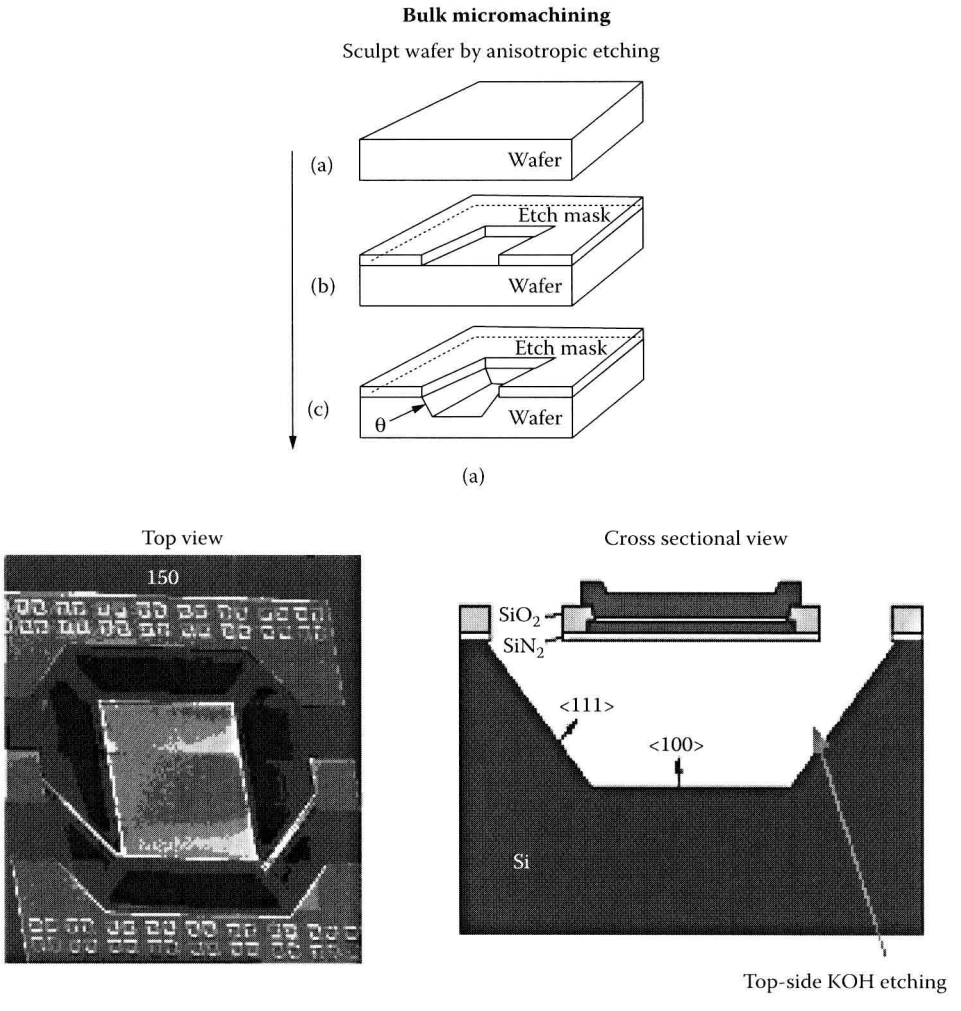

FIGURE 1.9 Bulk micromachining by anisotropic etching to produce features such as a capacitor. (Sun, Y., H. von Zeigl, J.L. Tauritz, and R. Baets, *Suspended Membrane Inductors and Capacitors for Application in Silicon MMCs,* Microwave and Monolithic Circuits Symposium Digest of Papers, IEEE, 1996, p. 99–102.)

In addition to producing nanofabrication tools for the manipulation of single atoms or clusters of atoms and molecules, in 2000, the semiconductor industry began producing field effect transistors with nanoscale features. The Pentium 4 microprocessor contains some 42 million transistors connected to each other on a single piece of silicon. In order to do this, silicon grown by the Czochralski process no longer produces a defect-free substrate for the deposition of nanoscale transistors. Producers of silicon wafers routinely deposit a defect-free single crystal silicon layer using a gaseous deposition technique. Engineers also deposit an oxide layer with low capacitance prior to the deposition of the thin silicon layer. This is known as silicon-on-insulator technology. This technology increases the speed with which transistors can be switched on and off. Another novel way of increasing the speed further still is to slightly strain the silicon lattice by forming a silicon-germanium blend that increases the mobility of electrons. To insulate the gate of the

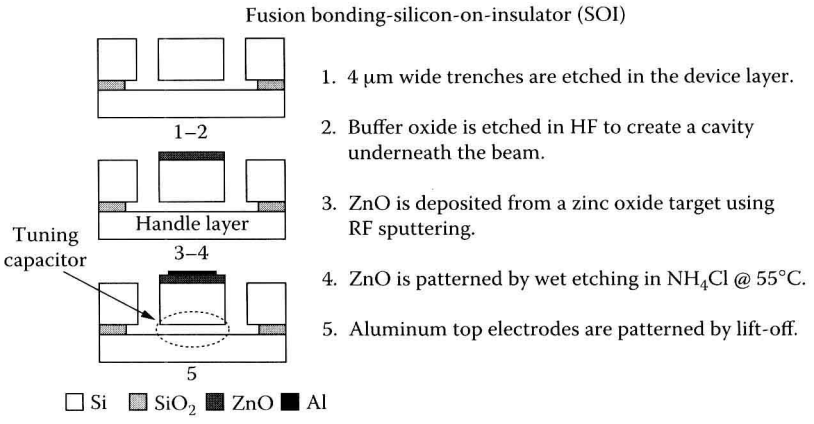

FIGURE 1.10 Fusion bonding of silicon on an insulator showing the various steps of the process. (Piazza, G.R., R. Abdolvand, and F. Ayazi, *Voltage-Tunable, Piezoelectrically-Transduced Single Crystal Silicon Resonators on SOI Substrates,* 2003 IEEE MEMS Conference, Kyoto, Japan, 2003, p. 149–152.)

transistor, a thin layer of silicon dioxide has traditionally been deposited to conventional substrates. A material with a high dielectric constant is being developed to replace the use of silicon dioxide. Hafnium oxide and strontium titanate are likely contenders that will allow the gate oxide layer to be slightly thicker, without compromising the switching ability of the transistor. This is achieved

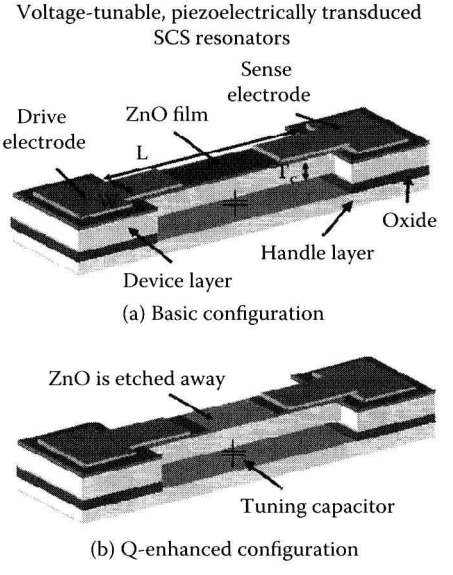

FIGURE 1.11 Voltage-tunable, piezoelectrically transduced SCS resonantor showing the manufacturing process used to produce the Q-enhanced configuration. (Piazza, G.R., R. Abdolvand, and F. Ayazi, *Voltage-Tunable, Piezoelectrically-Transduced Single Crystal Silicon Resonators on SOI Substrates,* 2003 IEEE MEMS Conference, Kyoto, Japan, 2003, p. 149–152.)