# Embedded Processor-Based Self-Test

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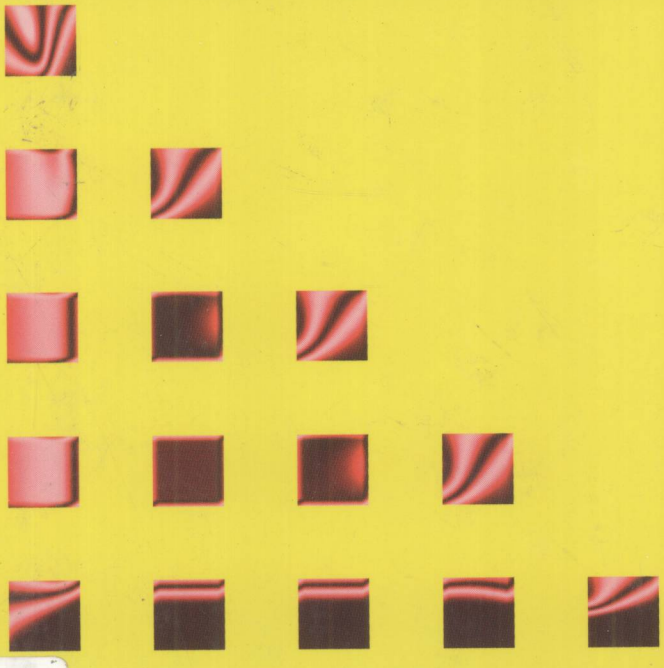

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# EMBEDDED PROCESSOR-BASED SELF-TEST

by

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to Georgia, Dora and Rita

# Preface

This book discusses self-testing techniques in embedded processors. These techniques are based on the execution of test programs aiming to lower the cost of testing for processors and surrounding blocks.

Manufacturing test cost is already a dominant factor in the overall development cost of Integrated Circuits (IC). Consequently, cost effective methodologies are continuously seeked for test cost reduction. Self-test, the ability of a circuit to test itself is a widely adopted Design for Test (DfT) methodology. It does not only contribute to the test cost reduction but also improves the quality of test because it allows a test to be performed at the actual speed of the device, to detect defect mechanisms that manifest themselves as delay malfunctions. Furthermore, self-test is a re-usable test solution. It can be activated several times throughout the device's life-cycle. The self-testing infrastructure of a chip can be used to detect latent defects that do not exist at manufacturing phases, but they appear during the chip's operating life

The application of self-testing, as well as, other testing methods, face serious challenges when the circuit under test is a processor. This is due to the fact that processor architectures are particularly sensitive to performance degradation due to extensive design changes for testability improvement. DfT modifications of a circuit, including those that implement self-testing, usually lead to area, performance and power consumption overheads that may not be affordable in a processor design. Processor testing and self-testing is a particularly challenging problem due to sophisticated complex processor structure, but it is also a very important problem that needs special attention because of the central role that processors play in every electronic system.

In this book, an emerging self-test methodology that recently captured the interest of test technologists is studied. *Software-based self-testing*, also called *processor-based self-testing*, takes advantage of the programmability of processors and allows them to test themselves with the effective execution of embedded self-test programs. Moreover, software-based self-testing takes advantage of the accessibility that processors have to all other surrounding

blocks of complex designs to test these blocks as well with such self-test programs. The already established System-on-Chip design paradigm that is based on pre-designed and pre-verified embedded cores employs one or more embedded processors of different architectures. Software-based self-testing is a very suitable methodology for manufacturing and in-field testing of embedded processors and surrounding blocks.

In this book, software-based self-testing is described, as a practical, low-cost, easy-to-apply self-testing solution for processors and SoC designs. It relaxes the tight relation of manufacturing testing with high-performance, expensive IC test equipment and hence results in test cost reduction. If appropriately applied, software-based self-testing can reach a very high test quality (high fault coverage) with reasonable test engineering effort, small test development cost and short test application time.

Also, this book sets a basis for comparisons among different software-based self-testing techniques. This is achieved by: describing the basic requirements of this test methodology; focusing on the basic parameters that have to be optimized; and applying it to a set of publicly available benchmark processors with different architectures and instruction sets.

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# *Introduction*

## 1.1 Book Motivation and Objectives

Electronic products are used today in the majority of our daily activities. Thus, they enabled efficiency, productivity, enjoyment and safety.

The Integrated Circuits (ICs) realized today consist of multiple millions of logic gates and even more memory cells. They are implemented in, very deep sub-micron (VDSM) process technologies and often consist of multiple, pre-designed entities called Intellectual Property (IP) cores. This design methodology that allowed the integration of embedded IP cores is known as Embedded Core-Based System-on-Chip (SoC) design methodology. SoC design flow supported by appropriate Computer Aided Design (CAD) tools has dramatically improved design productivity and has opened up new horizons for successful implementation of sophisticated chips.

An important role in the architecture of complex SoC is played by embedded processors. Embedded processors and other cores built around them constitute the basic functional elements of today's SoCs in embedded systems. Embedded processors have optimized design (in terms of silicon area, performance, power consumption, etc), and provide the means for the integration of sophisticated, flexible, upgradeable and re-configurable functionality of a complex SoC. In many cases, more than one embedded

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processors exist in a SoC, each of which takes over different tasks of the system and sharing the processing workload.

Issues such as the quality of the final SoC, the reliability of the manufactured ICs, and the reduced possibility of delivering malfunctioning chips to the end users, are rapidly getting more importance today with the increasing criticality of most of electronic systems applications.

In the context of these quality and reliability requirements, complex SoC designs, realized in dense manufacturing technologies face serious problems that need special consideration. Manufacturing test of complex chips based on external Automatic Test Equipment (ATE), as a method to guarantee that the delivered chips are correctly operating, is becoming less feasible and more expensive than ever. The volume of test data that must be applied to each manufactured chip is becoming very large, the test application time is increasing and the overall manufacturing test cost is becoming the dominant part of the total chip development cost.

Under these circumstances, which are expected to get worse as circuits size shrinks and density increases, the effective migration of the manufacturing test resources from outside of the chip (ATE) to on-chip, built-in resources and thus the effective replacement of external based testing with internally executed *self-testing* is, today the test technology of choice for all SoCs in practice. Self-testing allows at-speed testing, i.e. test execution at the actual operating speed of the chip. Thus all physical faults that cause either timing miss-behavior or an incorrect binary value can be detected. Also, self-testing drastically reduces test data storage requirements and test application time, both of which explode when external, ATE-based testing is used. Therefore, the extensive use of self-testing has a direct impact on the reduction of the overall chip test cost.

Testing of processors or microprocessors, even when they are not deeply embedded in a complex system, is known to be a challenging task itself. Classical testing approaches used in other digital circuits are not adequate to the carefully optimized processor designs, because they can't reach the same efficiency as in other types of digital circuits. Also, self-test approaches, successfully used to improve the testability of digital circuits, are not very suitable for processor testing because such techniques usually add overheads in the processor's performance, silicon area, pin count and power consumption. These overheads are often not acceptable for processors which have been specifically optimized to satisfy very strict area, speed and power consumption requirements.

This book primarily discusses the special problem of testing and self-testing of embedded processors in SoC architectures, as well as the problem of testing and self-testing other cores of the SoC using the embedded processor as test infrastructure.