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Edited by *R. K. WILLARDSON*

ALBERT C. BEER

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Semi-Insulating GaAs

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Preface

The advent of monolithic GaAs integrated circuits is having a broad impact on microwave signal processing and power amplification. Impressive improvements are being made in the performance and cost effectiveness of advanced systems for military radar and telecommunication as well as in digital integrated circuits for ultra-high-speed or fifth generation computers. A multibillion dollar market for GaAs analog, digital, and optoelectronic integrated circuits is predicted for the 1990s, with estimates as high as eight billion dollars in 1993 being made.

In the 1950s, semi-insulating GaAs was made by float-zone refining and by bombardment with electrons, neutrons, and protons. In the 1960s, the standard preparation technique involved the addition of chromium or the use of native defects (the EL2 center) and Fe, Zn, or Cd impurities—either natural or preferentially added. High-purity aluminum oxide, aluminum nitride, or boron nitride crucibles were used. The purity of the gallium and the arsenic was comparable with that available today, as was the GaAs produced.

In the 1970s, the group at the Naval Research Laboratory, as well as others, revived much of the dormant technology of the 1960s and added further improvements. High-purity undoped semi-insulating GaAs was prepared. High-pressure liquid-encapsulated Czochralski (LEC) pullers, developed at the Royal Radar and Signals Establishment and manufactured by Cambridge Instruments, provided an in situ method of reacting gallium and arsenic plus a technique for growing low-cost, large-diameter, stable, high-resistivity GaAs single crystals. A low-pressure technique for meeting the same objectives was developed at Hewlett-Packard. In this volume, these methods of crystal growth, including means for determining crystal quality, electrical and optical properties related to impurities and point defects, as well as use of direct ion implantation for the preparation of integrated circuits, are explained by experts working in this field.

The group at the Westinghouse Research and Development Center used the Melbourn (Cambridge Instruments) puller to grow high-quality GaAs crystals, with diameters ranging from 2 to 4 in. In Chapter 1, details of this process are described, including dislocation distributions and the effect of water in the boric oxide on twinning. Thermal gradients, asymmetries, and

fluctuations can be influenced by pressure and boric oxide thickness, and these are related to dislocation densities and impurity stria. Advances are proceeding very rapidly in this area and after these chapters were set in type a procedure was reported, involving the use of indium, which gave a reduction in dislocation densities by as much as a factor of 25. Also, Terashima and co-workers at the Optoelectronics Joint Research Laboratory in Kawasaki have shown that the application of a magnetic field can reduce both the number of EL2 defects and the dislocation density in crystals grown with a Melbourn puller.

In Chapter 2, materials and ion implantation procedures, which are used at Hewlett-Packard for the fabrication of GaAs integrated circuits, are discused. Emphasis is given to a low-pressure LEC technique, which has been used for in situ synthesis of the GaAs to produce high-quality 65-mm-diameter single crystals, having dislocation densities as low as $200/cm^2$. Interestingly, similar results have been reported by Zou and co-workers in China. Spectrographic analyses and Hall mobilities of electrons in implanted semi-insulating GaAs produced by high- and low-pressure LEC, Bridgman, and liquid-phase-epitaxial growth are used to evaluate these growth methods and their suitability for producing device quality substrates.

Extensive studies of Melbourn LEC growth of GaAs, including dislocations, twins, surface gallium inclusions, microdefects, and stoichiometry by the group at Rockwell Microelectronics Research and Development Center are presented in Chapter 3. The key to reproducible growth of undoped semi-insulating GaAs is control over melt stoichiometry and impurity content — the balance between EL2 deep donors and shallow acceptors. The incorporation of EL2 centers increases as the atom fraction of arsenic increases. An acceptor lattice defect, which increases in concentration as the gallium atom fraction is increased above the stoichiometric proportion, is also described. Fine structure in dislocation distributions shows both cellular structure and lineages, with relatively high densities being measured along ⟨100⟩ compared to ⟨110⟩ directions. More recently, it has been reported that similar distributions or inhomogeneities in the EL2 center are revealed by infrared imaging.

Chapter 4 focuses on models for deep levels in semiconductors such as semi-insulating GaAs. It extends the discussions of deep levels in III–V compounds which were treated in Volume 19 of our treatise and provides a guide for experimentalists to extensive and detailed theoretical treatments of localized states in the central part of the intrinsic gap. A classification scheme for the principal varieties of localized flaws in semiconductors is presented. Approaches that have been made theoretically to describe deep-lying states derived from nonextended flaw situations are explained. The features responsible for a flaw's signature are examined, including the form

of the potential, site symmetry, and any distortion or relaxation of the lattice.

The editors are indebted to the many contributors and their employers who made this treatise possible. They wish to express their appreciation to Willardson Consulting and Battelle Memorial Institute for providing the facilities and the environment necessary for such an endeavor. Special thanks are also due to the editors' wives for their patience and understanding.

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Contents

CHAPTER 1

High-Purity LEC Growth and Direct Implantation of GaAs for Monolithic Microwave Circuits†

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List of Symbols

ASES	Arc source emission spectroscopy
$C-V$	Capacitance–voltage
D	Diffusion constant ($cm^2\ sec^{-1}$)
DLTS	Deep-level transient spectroscopy
EL2	Main deep-donor level in undoped GaAs
DWS	Differential weight gain signal
f	Fraction melt solidified
FET	Field effect transistor
g	Ground-state degeneracy factor
I_{fc}	Full channel current ($A\ cm^{-1}$)
k_0	Effective segregation coefficient
K	Mass action constant governing the donor/acceptor role of implanted silicon via interaction with $n(T_a)$
k_1	Mass action constant describing the contribution of arsenic-vacancies V_{As} on the electron density measured at T_a
LEC	Liquid-encapsulated Czochralski
LPE	Liquid-phase epitaxy
LVM	Localized vibrational mode far-infrared spectroscopy
MESFET	Metal–semiconductor field effect transistor
N_D^+	Ionized donor concentration (cm^{-3})
N_{Do}^+	Residual ionized donor concentration (cm^{-3})
N_A^-	Ionized acceptor concentration (cm^{-3})
N_{Ao}^-	Residual ionized acceptor concentration (cm^{-3})
n_i	Intrinsic free-electron concentration (cm^{-3})
N_{SC}	Net donor concentration in the implanted layer (cm^{-2})
N_{SM}	Free-electron concentration in the implanted layer including surface depletion effects (cm^{-2})
N_{SMH}	Free-electron concentration in the implanted layer as determined by surface Hall-effect measurement (cm^{-2})
N_{SMO}	Concentration that can be depleted at breakdown in an idealized parallel plate geometry (cm^{-2})
[OH]	Water content in the encapsulant
PBN	Pyrolytic boron nitride
PR	Photoresist
PSG	Phosphosilicate glass
V	Electronic charge
R_M	Depth of maximum implanted concentration
R_P	Projected range of the implanted ion concentration
R_{PA}	Projected range of the ionized net donor concentration
sccm	Standard cubic centimeter per minute
SIMS	Secondary ion mass spectrometry
SSMS	Spark source mass spectrometry
{Si}	Implanted silicon concentration (cm^{-3})
T_a	Annealing temperature
Tang end	Tail section of an ingot
V_p	Pinch-off voltage
VPE	Vapor-phase epitaxy
V_B	Breakdown voltage
v_{sat}	Electron saturation velocity

Δ	Net donor concentration ($N_D^+ - N_A^-$)
ϵ	Permittivity of GaAs
λ_d	Surface-depletion depth
λ_0	Effective channel thickness ($R_M + \sqrt{\pi/2} \cdot \sigma_d$)
μ_D	Electron drift mobility
μ_{SH}	Average electron mobility as determined by surface Hall-effect measurement
η	Differential net donor activation efficiency determined with respect to the implanted-ion concentration
η_Δ	Differential net donor activation efficiency determined with respect to Σ
η_Σ	Differential total ionized center activation efficiency determined with respect to implanted-ion concentration
ρ	Resistivity
$\sigma_{s,d}$	Standard deviations of a single energy implant based on joined half-gaussian modeling for the surface and deep sides of R_M, respectively
θ	Compensation ratio defined as the concentration of implanted ions acting as acceptors divided by the concentration of implanted ions acting as donors [e.g., $(Si^-)/(Si^+)$]
Σ	Total equivalent ionized center concentration ($N_D^+ + N_A^-$)

I. Introduction

GaAs metal–semiconductor field effect transistors (MESFETs) have received increasing attention over the past decade for applications beyond the 1–2-GHz operating range of silicon devices because of the higher electron mobility and saturated velocity in GaAs, and because of its availability as a semi-insulating substrate. This technology has now progressed to where monolithic integration in GaAs of many high-frequency circuit functions is being pursued vigorously in several laboratories throughout the world. The advent of monolithic GaAs integrated circuits (ICs) is expected to have a broad impact on the way in which microwave detection, signal processing, and power amplification will be carried out in the future. Military radar and microwave telecommunication systems, in particular, are expected to reap dramatic benefits of improved performance and availability at significantly reduced costs from this emerging technology. Significant advances have already been demonstrated in the fabrication of monolithic GaAs amplifiers for low-noise/high-gain or high rf power outputs at X-band frequencies and beyond, as well as in very high-speed GaAs digital logic ICs for "front-end" data processing.

Historically, GaAs MESFET technology has been strongly influenced by the quality of the underlying semi-insulating substrate and, over the years, an epitaxial processing technology has been developed to circumvent the unpredictable and often undesirable effects of the substrate. High-purity, epitaxial buffer layers are often utilized to decouple the active device region from the substrate, and the commercial availability of high-performance, epitaxial field effect transistors (FETs) capable of very low-noise figures (as

low as 2.8 dB at 18 GHz) or with high output powers (exceeding 5 W at 12 GHz) attests to the effectiveness of these techniques.

In contrast to discrete FETs, the present trend in monolithic GaAs circuit fabrication strongly favors the use of direct-into-substrate implantation techniques. This follows from the much greater flexibility of direct ion implantation over epitaxial techniques for device processing. In particular, selective implantation enables active device regions to be confined to selected areas on a semi-insulating substrate without resorting to the mesa-etch isolation techniques of epitaxial structures. Relatively simple planar processing can therefore be used to combine diode and FET structures with passive circuit elements on the same semi-insulating substrate. This planar and selective nature of implantation is a significant advantage and holds considerable promise of evolving as a high-yield manufacturing technology.

Significant progress (Welch *et al.*, 1974; Thomas *et al.*, 1980) is currently being made toward developing a viable planar ion-implantation technology, but it is widely recognized that direct implantation imposes severe demands on the quality of the semi-insulating GaAs substrate. In the past, the inferior properties of commercially available semi-insulating substrates, usually prepared by horizontal Bridgman or gradient freeze techniques, have been major limitations to attaining uniform and predictable device characteristics by implantation. These problems of substrate reproducibility are now well recognized in a symptomatic sense and are probably associated with excessive and variable concentrations of impurities — particularly, silicon, chromium, oxygen, and carbon — present in typical Cr-doped semi-insulating GaAs substrates, which contribute to the difficulties in achieving uniform implant profiles. A common manifestation of the problem is the formation of a conductive *p*-type surface layer following a thermal annealing process. These anomalous conversion and compensation phenomena, which have been observed following post-implantation annealing, adversely affect the implant profile and activation and can result in poor control of full-channel current and pinch-off voltage in directly implanted FET structures. Chromium redistribution has been graphically demonstrated in the case of directly implanted Cr-doped substrates by Huber *et al.* (1979a) and Evans *et al.* (1979). In addition, typical Cr-doped GaAs substrates contain at least 1×10^{17} cm^{-3} ionized impurities that severely reduce the electron mobility in directly implanted FET channels and degrade the FET performance and frequency limitations. Monolithic GaAs circuits require substrates that

(a) exhibit stable, high resistivities after thermal processing to maintain both good electrical isolation and low parasitic capacitances associated with active elements;

(b) contain very low total concentrations of ionized impurities so that the implanted FET channel mobility is not degraded; and

(c) permit fabrication of devices of predictable characteristics so that active and passive elements can be matched in monolithic circuit designs.

Another important consideration is the need for uniformly round, large-area substrates. Broad acceptance of GaAs ICs by the user and systems communities will occur only if a reliable GaAs IC manufacturing technology capable of yielding high-performance monolithic circuits at reasonable costs is realized. Unfortunately, the characteristic D-shaped slices of boat-grown GaAs material have been a serious deterrent to the achievement of this goal, since much of the standard semiconductor processing equipment developed for the silicon IC industry relies on uniformly round substrate slices. To address these needs for a reliable "siliconlike" technology base in semi-insulating GaAs materials processing, liquid-encapsulated Czochralski (LEC) growth was selected over other growth technologies because of its current capability for producing large-diameter, ⟨100⟩ and ⟨111⟩ crystals of semi-insulating GaAs. The 50- and 100-mm-diam wafers cut from ⟨100⟩-oriented LEC GaAs crystals are shown in Fig. 1 to illustrate the significant economic benefits of large-area processing. The monolithic power amplifiers shown on the 50-mm slice are approximately 5×2 mm. Device

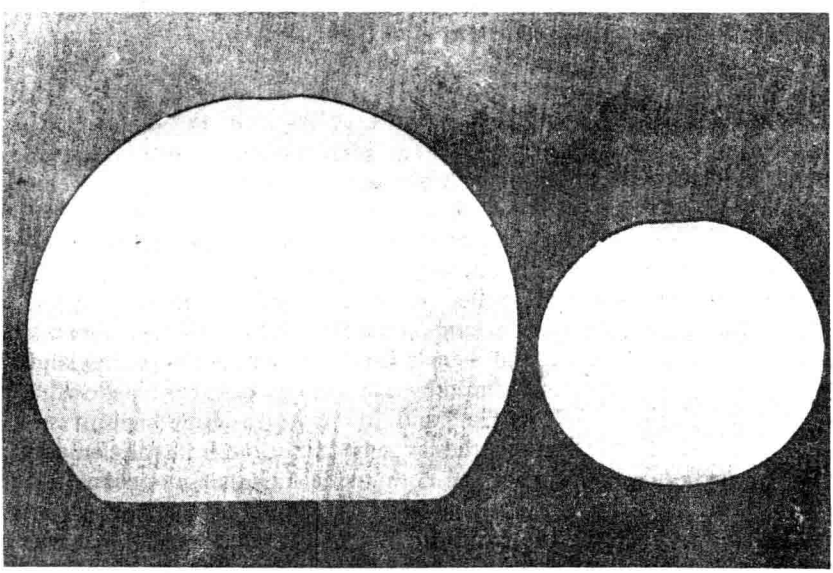

FIG. 1. Comparison of available wafer area for monolithic power amplifier fabrication on 50- and 100-mm-diam GaAs slices cut from ⟨100⟩ crystals grown in high-pressure Melbourn LEC puller.

processing on 100-mm wafers would increase the die count from 75 to 300 per wafer, although the handling and processing costs in manufacturing are approximately independent of wafer size.

In the following sections, we report on the growth of high-purity, large-diameter ⟨100⟩ GaAs crystals; on assessments of the structural perfection, compositional purity, and electrical properties of these crystals; and upon evaluation of their suitability and compatibility for direct ion-implantation device processing. Finally, the application of many of the wafer fabrication techniques now confined to the silicon industry to produce uniform, large-area substrates in GaAs is discussed briefly.

The underlying aim is to establish a reproducible GaAs materials base in order to realize the full potential of direct ion implantation as a reliable, cost-effective fabrication technology of high-performance GaAs MESFET devices and integrated circuits.

II. Large-Diameter GaAs Crystal Growth

1. High-Pressure LEC Technology

Liquid encapsulation was first demonstrated experimentally by Metz *et al.* (1962) for the growth of volatile PbTe crystals and has since been applied to the Czochralski process by Mullin *et al.* (1968) and others (Swiggard *et al.*, 1977; Henry and Swiggard, 1977; AuCoin *et al.*, 1979; Ware and Rumsby, 1979) for the growth of several III–V crystals. In liquid-encapsulated Czochralski, the dissociation of the volatile As from the GaAs melt is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a nonreactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure.

The LEC technique has been developed intensively in recent years, and high-pressure pullers are now available commercially. One is the "Melbourn" high-pressure LEC puller (manufactured by Cambridge Instruments, Ltd., in Cambridge, England, and is the outcome of developmental efforts at the Royal Radar and Signals Establishment, Malvern, England), which is currently being introduced by many laboratories for the growth of large bulk GaAs as well as GaP and InP crystals. With high-pressure capability, in situ compound synthesis can be carried out from the elemental Ga and As components, since the boric oxide melts before excessive As sublimation starts to take place ($\leq 460°C$). Compound synthesis occurs rapidly and exothermally at about 820°C under a sufficient inert gas pressure (~ 60 atm) to minimize significant sublimation of the arsenic component. To maintain a nearly stoichiometric or slightly arsenic-rich melt, a slight excess of As is utilized to compensate for inadvertent loss of As during the heat-up cycle. After compound synthesis, the chamber pressure can be

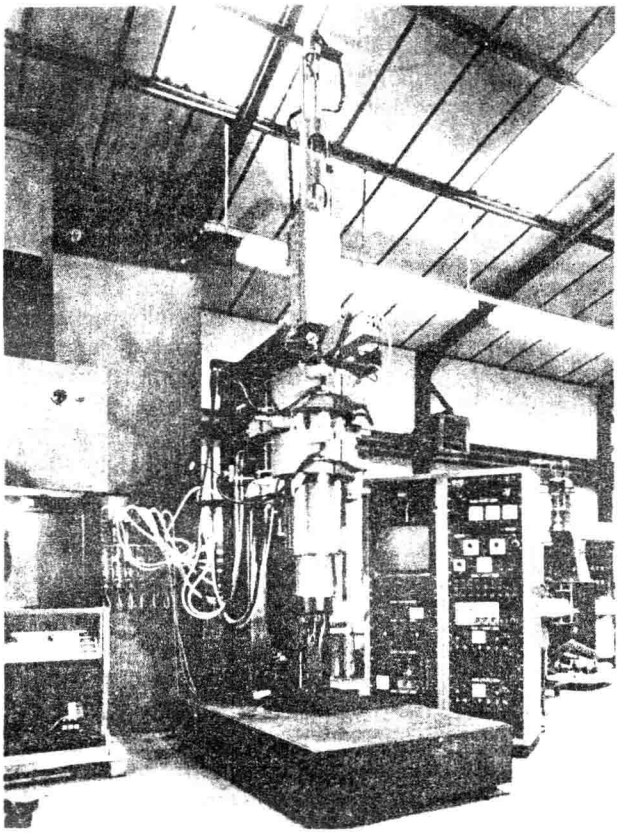

FIG. 2. Melbourn high-pressure, liquid-encapsulated Czochralski puller. (Courtesy of Cambridge Instruments Ltd., England.)

decreased to ~20 atm and crystal growth initiated from the 1238°C GaAs melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.

Large-diameter GaAs crystals are typically pulled at speeds less than 10 mm hr^{-1}, and counter- and corotation of seed and crucible at rates between 6 and 18 rpm have been investigated. The Melbourn LEC puller shown in Fig. 2 consists of a resistance-heated 150-mm-diam crucible system capable of charges up to about 10 kg and can be operated at pressures up to 150 atm. The GaAs melt within the pressure vessel can be viewed by means of a closed-circuit TV system. A high-sensitivity weight cell continuously weighs the crystal during growth and provides a differential weight signal for manual diameter control. In addition, a unique diameter control

technique, which involves growing the crystal through a diameter-defining aperture, has been developed for ⟨111⟩-oriented growth (Ware, 1977). In this "coracle" technique, the defining aperture is fabricated from pressed silicon nitride, which conveniently floats at the GaAs melt–B_2O_3 encapsulant interface.

2. Growth from Large GaAs Melts

a. Manual Diameter Control

At our laboratories, the high-pressure Melbourn LEC puller has been employed to develop a reproducible growth technology for preparing large-diameter (up to nominally 100 mm), ⟨100⟩-oriented GaAs crystals. Techniques for producing crystals which are free of major structural defects (such as twin planes, lineage, inclusions, and precipitates), and which yield stable, semi-insulating properties without resorting to conventional Cr doping, have been successfully developed over the course of about 70 experimental growths. The work expands upon earlier LEC studies of Swiggard *et al.* (1977) and AuCoin *et al.* (1979), who showed independently that improved purity, semi-insulating GaAs crystals could be grown from undoped LEC melts when contained in high-purity, pyrolytic boron nitride (PBN) crucibles. The present effort is directed at the growth of much larger crystals required for commercial GaAs IC processing, and exploits the recent availability of 150-mm-diam PBN crucibles in conjunction with an advanced high-pressure LEC technology as embodied in the Melbourn puller. For comparison purposes, GaAs crystals grown from Cr-doped melts and using conventional fused silica crucibles have also been investigated. Two semi-insulating ⟨100⟩ GaAs crystals pulled from pyrolytic boron nitride crucibles and grown using the differential weight signal for diameter control are shown in Fig. 3. The crystal in Fig. 3a is nominally 50 mm in diameter and weighs 3 kg; Fig. 3b shows a nominally 100-mm-diam crystal weighing 6 kg. Such a crystal will yield approximately 200 semi-insulating substrates.

The growth of crystals in the ⟨100⟩ orientation has relied upon the ability to control the crystal diameter by continuously monitoring the crystal weight and the instantaneous derivative of the weight gain signal (DWS). On the basis of these measured quantities and visual monitoring through the TV system, adjustments to the power level are made to correct for undesirable changes in crystal diameter. However, owing to reliance upon operator judgment and the inability to see clearly at all times the growth meniscus through the boric oxide layer, as well as systematic errors in the differential weight gain signal due to capillary forces (Jordan, 1981), this growth method results in crystals with diameters which vary (usually within ±5 mm) along the boule length, as demonstrated by the crystals in Figs. 3a and 3b and the