

**Second International Conference  
on Indium Phosphide and Related Materials**

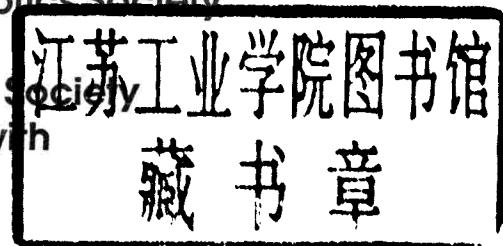
**Second International  
Conference**

**Indium Phosphide and Related Materials**

**April 23 - 25, 1990**

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Denver, Colorado**

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Chair: Y. Yoshikuni, NTT Optoelectronics Lab, Kanagawa, Japan

- WA.1 Monolithic Mode Locked GaInAsP Lasers**, P. A. Morton, A. Mar, and J.E. Bowers, University of California, Santa Barbara, CA; L.A. Koszi, M. Soler, J. Lopata, and D.P. Wilt, AT&T Bell Laboratories, Murray Hill, NJ

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- WA.2 Optimization of Etched Mesa Profiles During Planarized Mesaembedding Layer Growth and Fabrication of Etched-mesa Buried Heterostructure (InGaAsP/InP) Distributed Feedback Laser**, U.K. Chakrabarti, J. L. Zilko, N. K. Dutta, R. L. Brown, Y. Twu, J. W. Lee and A. B. Piccirilli, AT&T Bell Laboratories, Murray Hill, NJ

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- WA.3 Performance Characteristics of Buried Facet Optical Amplifiers**, M.S. Lin, A. B. Piccirilli and N. K. Dutta, AT&T Bell Laboratories, Murray Hill, NJ

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- WA.4 Design of High Speed GaInAs/InP p-i-n Photodetectors**, Y.G. Wey, D.L. Crawford, J.E. Bowers, University of California, Santa Barbara; M.J. Hafich, G.Y. Robinson, Colorado State University, Ft. Collins, CO; F. Storz, AT&T Bell Laboratories, Holmdel, NJ

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### **WB: OPTOELECTRONIC DEVICES II**

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- WB.2 A High-Speed Broad-Wavelength InAlAs/InGaAs Schottky Barrier Photodiode for 0.4 to 1.6  $\mu$ m Detection**, K.C. Hwang, and S. S. Li, University of Florida, Gainesville, FL; Y.C. Kao, Texas Instruments, Inc., Dallas, TX

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- WC.1 Ion Beam Processing and Rapid Thermal Annealing of InP and Related Compounds**, S. J. Pearton, AT&T Bell Laboratories, Murray Hill, NJ

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- WC.2 Improved Thermal Processing of MOS Diodes on n-InP**, Z.Q. Shi, Y.S. Lee, and W. A. Anderson, State University of NY at Buffalo, Amherst, NY

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- WC.3 A Native Oxide Mask for In-Situ Patterning of InP**, Y.L. Wang, H. Temkin and Lloyd R. Harriott, AT&T Bell Laboratories, Murray Hill, NJ

N/A

- WC.4 Remote Plasma Etching of InP in Cl<sub>2</sub> and HCl**, D. G. Lishan and E. L. Hu, University of California, Santa Barbara, CA

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- WC.5 Dislocation Density After S-Diffusion Into p-Type InP Substrates**, M. Faur, M. Faur, C. Goradia and R. Clark, Cleveland State University, Cleveland, OH; I. Weinberg, NASA Lewis Research Center, Cleveland, OH

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- WC.6 Etching of InP in Methane-Based Plasmas**, I. Adesida, C. Jones, and N. Finnegan, Materials Research Laboratory, University of Illinois, Urbana, IL; E. Andideh, Department of Electrical & Computer Engineering, University of Illinois, Urbana, IL

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- WC.7 Variations in Surface Morphology of Ion Implanted InP after Rapid Thermal Annealing**, D.V. Stevanovic, P.L. Ferret and D.A. Thompson, McMaster University, Hamilton, Ont., Canada

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**MONDAY, APRIL 23**

## InP-based Heterojunction Bipolar Transistors: Performance Status and Circuit Applications

P.M. Asbeck, C.W. Farley, M.F. Chang, K.C. Wang and W.J. Ho  
Rockwell International Science Center  
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### Abstract

Present status and prospects of heterojunction bipolar transistors configured with InP, InGaAs and/or InAlAs on InP substrates are reviewed. Importance of ultrahigh electron velocity is highlighted. Self-aligned fabrication techniques are described, and devices with wide bandgap collectors for microwave power applications and with low turn-on voltage  $V_{be}$  for digital applications are presented. Frequency dividers configured with these devices have operated to 17GHz.

### Introduction

The recent achievement of ultrashort (sub-picosecond) transit times in InP-based HBTs has been the source of considerable excitement [1]. At present, InP-based HBTs are being vigorously developed for microwave, digital and optoelectronic applications. This paper reviews the present status of device technology, and describes future prospects for InP-based HBTs.

The HBT structure has inherent advantages for a variety of applications.

- 1) Ultrahigh  $f_t$  and  $f_{max}$  can be obtained as a result of short transit times for carriers. The relevant dimensions are controlled by epitaxial growth and can be made very short even with simple processing with conventional lithography.
- 2) HBTs provide very high transconductance and high current handling capability per unit chip area.
- 3) Device turn-on ("threshold") voltage is very well controlled and uniform.
- 4) HBTs do not suffer from backgating or trapping effects, and leakage currents through substrates are absent. These issues are of significant concern in FET technologies.
- 5) Breakdown voltage is directly controllable by transistor design (collector structure).

InP-based materials provide a significant number of advantages over competing materials for HBT implementation:

- 1) Electron mobility is very high on a steady-state basis at low electric fields and velocity can be high under nonequilibrium conditions at high fields (velocity overshoot).
- 2) Material combinations are available which offer large bandgap differences (for the convenient implementation of wide bandgap emitters and collectors) and can be doped controllably over a wide range (above  $10^{20} \text{ cm}^{-3}$ ).
- 3) Surface recombination velocity is lower than for GaAs.
- 4) Low bandgap materials are available for use in the base region (InGaAs), which can provide low  $V_{be}$  value for digital circuit operation.
- 5) Substrate thermal conductivity is high (0.7 W/cmC for InP compared with 0.46W/cmC for GaAs).
- 6) Devices utilize the same substrate as sources and detectors of 1.3-1.55 $\mu\text{m}$  radiation, simplifying the fabrication of optoelectronic integrated circuits.

### HBT Structure

Highest speed performance has been obtained from Npn HBT structures whose band diagram in the direction of electron travel is shown in fig. 1. Emitters of InP or AlInAs have been employed. Base regions and typically collector regions consist of InGaAs. Upon traversing the base-emitter junction, electrons are given high kinetic energy as a result of the conduction band step

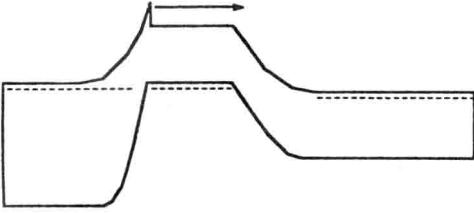


Fig. 1. Schematic band diagram of InP HBT with hot electron injection into base

(which amounts to  $dEc=0.23\text{eV}$  for InP/InGaAs junctions, and  $dEc=0.55\text{eV}$  for AlInAs/InGaAs junctions). For sufficiently thin base regions ( $<500\text{\AA}$ ) most of the electron forward momentum is retained as the electrons cross the base. In the base-collector depletion region, electrons are driven to very high velocity by the electric field. This velocity can be maintained if the voltage drop is kept sufficiently small that the electrons do not scatter from the gamma minimum to satellite valleys, which requires small values of applied voltage (since the separation of gamma and X minima is  $0.55\text{eV}$  in GaInAs).

HBTs utilize high acceptor doping level in the base. For solid or gas-source MBE, concentrations up to  $1-5 \times 10^{20} \text{ cm}^{-3}$  have been obtained using Be doping. Dopant redistribution has been retarded by growth at low temperatures (down to  $350^\circ\text{C}$ ). MOCVD growth has been used with Zn or Be doping. For both materials, hole mobility is relatively low ( $50-75 \text{ cm}^2/\text{Vsec}$ ) at the highest concentrations. The subcollector region and emitter contact regions make use of heavily doped n-type material. Concentrations of  $6-8 \times 10^{19} \text{ cm}^{-3}$  have been used, with Si doping. The associated contact resistances are extremely low ( $<1-2 \times 10^{-7} \text{ ohm cm}^2$ ).

For a variety of applications, it is desirable to establish a graded composition between wide band gap and narrow bandgap device regions. For InP-based materials, continuous grading requires quaternary intermediate compositions which must be precisely controlled in order to maintain lattice match. An alternative method is to employ short period superlattices composed of the ternary materials, whose composition is accurately controlled. In the work at Rockwell the superlattice period is kept constant at  $12\text{\AA}$  and the duty factor of the materials is varied across a number of intermediate ratios as illustrated in fig. 2. For highest speed performance, device layout and processing must succeed in minimizing the separation between emitter and base contacts, and minimizing the area of the base-collector junction. Self-aligned approaches have been developed for this purpose [3]. Isolation is typically accomplished by mesa etching down to the semi-insulating InP substrate. Planarization is subsequently needed in order to facilitate interconnects. Fig. 3 illustrates the structure used at Rockwell for InP-based ICs. The structure is a derivative of the "dual-liftoff" technique described for GaAs HBT circuits [4]. Planarization based on SiO<sub>x</sub> and polyimide is utilized. The top view of a fabricated HBT is shown in fig. 4.

InP HBTs typically feature current gain on the order of 50-100, relatively independent of bias current (since base and collector current ideality factors are both near unity) and independent of emitter size (since the emitter edge recombination component of base current is typically low). The  $f_t$  obtained for the devices is typically higher than for comparable GaAs HBTs, and has reached the value of  $165\text{GHz}$  at room temperature, and  $244\text{ GHz}$  at  $77\text{K}$  [1]. The associated value of  $f_{max}$  was  $100\text{ GHz}$ . The estimated average velocity of electrons traversing the base and collector depletion regions was  $3.5 \times 10^7 \text{ cm/S}$ .

The high velocity is of particular significance. With bipolar structures, it is relatively convenient to minimize the distance over which electrons travel, and as a result high  $f_t$  can be obtained in numerous material systems. In SiGe/Si HBTs,  $f_t$  of  $75\text{ GHz}$  has recently been reported [5].

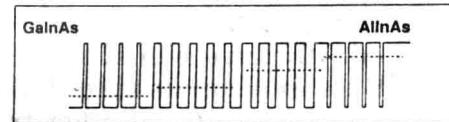


Fig. 2. Short period superlattice technique for grading effective composition.

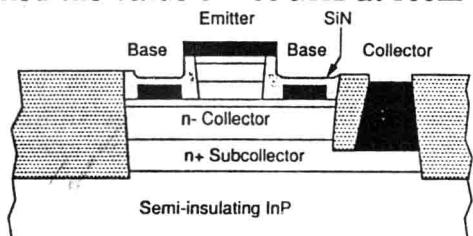


Fig. 3. Schematic cross-section of self-aligned HBTs fabricated at Rockwell.