SUPERCONDUCTIVITY ELECTRONICS

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Preface

This volume summarizes and makes available to overseas as well as domestic researchers in the field of superconductive electronics the outcomes of research and development in this field in Japan. It covers the last five years, i.e., since the Committee on Superconductive Electronics of the Japan Society for the Promotion of Science was established.

Before the committee was established, the Special Research Project on Superconductive Quantum Electronics started a three–year project in 1979 to financially support individual research workers in universities and also discussion and information exchange among researchers in universities, government, and related research institutions as well as industrial organizations. The results of R and D of the Special Project have been summarized in the Proceedings of the Symposium on Superconductive Quantum Electronics (issued March 1983). The key fabrication technology in those days was, roughly speaking, limited to the framework of lead alloy technology following the IBM developments. Nonetheless, Nb and NbN fabrication technology was developed and investigated with great effort during this period. Basic research expanded also during this time in such fields as integration of logic and memory circuit, single flux quantum logic, variety of SQUID applications (NMR, MCG, geophysics, solid state physics etc.), metrology applications ($h/2e$ determination, noise, and temperature measurement), radio frequency applications (Josephson junction oscillator, detection, and mixing of microwave and laser), and weak link fabrication technology of good quality.

Fortunately, following the Special Research Project period, researches as well as population growth in this field in Japan expanded steadily despite world wide deceleration due to the stumbling of IBM's project on the high performance Josephson computer. Integrated circuit technology based on NbN and Nb–Aloxide–Nb junctions has nearly reached its peak, though practical applications must be considered. Fluxoid logic has been intensively studied together with the Josephson sampler to monitor the performance of logic transition. Measurement technology such as Josephson potentiometer and $h/2e$ determination together with quantum Hall resistance are now opening new areas of low temperature quantum metrology. Josephson mixers of various kinds are reaching their ultimate performances. SQUID applications are becoming more and more practical

with combinations of planar signal coupling and Nb related fabrication technology. Improvements in weak link performance are accomplished by a variety of fabrication methods that will find numerous of applications in the future. Of importance are the exploratory trials in Chapter 5 of this volume, among which three terminal devices are of interest, where much more physics is necessitated.

As mentioned above, research and development in this field in Japan have made great progress during the JSPS period. However, effective demonstration and practical applications of this progress proved difficult to achieve. Superconductive electronics must some aspect inevitably compete with semiconductor electronics that is powerful in every aspect of technological, historical, and social viewpoints. Continuous efforts are being made by the superconductive electronics researchers.

Finally, discussion on the recent rapid progress in the high T_c oxide superconductor have not been included in this volume except for a few contributions. This has, no doubt, a big impact not only as a zero resistance conducting material, but also as a material for superconductivity on R&D electronics. Physics and technology of the thin film of this material (necessarily single crystal) with physically well defined surface for superconductive electronics should be the goal pursued with great effort to gain popularity in the general world.

Ko Hara

June 1987

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I JOSEPHSON INTEGRATED CIRCUIT

I·1·1 JOSEPHSON IC TECHNOLOGY

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ABSTRACT

A Josephson integrated circuit(IC) technology developed at ETL for high speed digital applications is reviewed. Logic circuit technology using a 4JL(four junction logic) gate family is presented. Various circuits such as 2-bit ALU(arithmetic logic unit) and 4-bit shift-register have been developed using an Nb/Al-oxide/Nb junction technology. A new approach for realizing Josephson RAM(random access memory) in which the variable threshold memory cells are integrated is described. A more advanced technology of all-refractory planarization process has been developed and adapted to fabricate a 4x4-bit multiplier chip, in which more than 2800 Josephson junctions are integrated. The 4-bit multiplication was achieved in 1ns. A new fabrication process of CLIP(cross line pattern) method for integrating sub-micron NbN junctions in LSI chips has been developed, that shows small spreads in Josephson critical currents.

INTRODUCTION

Josephson digital LSIs have been expected to have high performance in both circuit speed and power dissipation. The superconducting digital system based on Josephson IC technology has also great advantages for realizing ultra-high speed computers because of extremely low loss and distortion for high speed signal transmission made by superconducting strip lines. Josephson integrated circuit technology has been evolved with the lead-alloy technology developed by IBM groups[1]. A number of circuits were demonstrated using this technology. More recently, Josephson IC technology has been accelerated by refractory junction technology such as NbN/ NbN[2] and Nb/ Nb[3]. Material research, integration process and circuit design have also been developed extensively. The circuits fabricated using refractory materials show higher performance than that of conventional devices.

In this paper, a new approach for Josephson IC technology developed at ETL is reviewed. First, the logic circuit technology based on a 4JL-gate family shows a feasibility to realize digital systems. Both combination logic circuits(2-bit ALU and 4-bit multiplexer) and sequential logic circuits(4-bit shift-register and 4-bit counter) have been developed. Second, the principle of a new Josephson memory cell named variable threshold memory is described. The cell has been extended to integrate a 1k-bit cell plane. Third, the all-refractory planarization process including spin-on glass process has been successfully demonstrated to develop a 4x4-bit multiplier circuit, which has a complexity at LSI level. Finally, a sub-micron tunnel junction process which is adaptable to integrate junctions with precise dimensions is discussed.

LOGIC CIRCUIT TECHNOLOGY USING 4JL-GATE

The 4JL-gate[4][5] consists of four Josephson junctions which are directly coupled in a closed loop. In this 4JL-gate, operating characteristics are essentially determined by the phase relations of the individual junctions, which gives us a wide fabrication tolerance in integrated circuits. The elimination of the inductances in the closed loop makes it possible to reduce the device size, resulting in faster switching speed. In fact, the delay time of 7ps at a power dissipation of 4μW has been achieved in a ten-stage chain of the 4JL-gates with 2.5μm square junctions[6].

A 4JL-gate family is designed for making integrated logic circuit. Figure 1 shows schematic configurations of the 4JL-family gates; (a) two-input OR-, (b) two-input AND-, (c) AMP- and (d) timed

INVERT-gates, and their threshold curves, respectively[7]. Wide operating margin of more than ±35% is obtained in each gate. In this gate family, the current-isolation function between input and output is performed by the OR-gate. OR-AND gate-cell[8] is useful to construct the circuits systematically. The AMP-gate is used to obtain a fan-out of 4.

A data-latch function is quite important in logic circuits, especially in sequential logics. A directly-coupled data-latch[9] which consists of five 4JL-gates and two single junctions is developed. The circuit configuration is shown in Fig. 2. The latch can generate dual outputs of true(T) and complement(C), driving by a two-phase power supply P1 and P2 as is described in the figure. Single junctions Jp and Jn prevent the input signal from free-running for overlap-interval of P1 and P2.

A flip-flop function is achieved to make a feedback loop by using two data-latch circuits. This data-latch do not need any inductances for the data storage, so that the sequential circuit size can be reduced, resulting high speed operations.

Nb/Al-oxide/Nb junctions were used to make Josephson integrated logic circuits. In order to integrate small junctions with high Vm, an Nb underlayer[10] was introduced. Figure 3 shows a cross section of the circuit. A junction sandwich with a 2-inch Si wafer size was first made on the Nb underlayer which was defined by the base-electrode pattern. The tunnel barrier was made by thermal oxidation of the Al film surface with a pure oxygen gas of 1 torr at ambient temperature. Each junction was defined by an RIE(reactive ion etching) process with CF4 gas. MgO thin

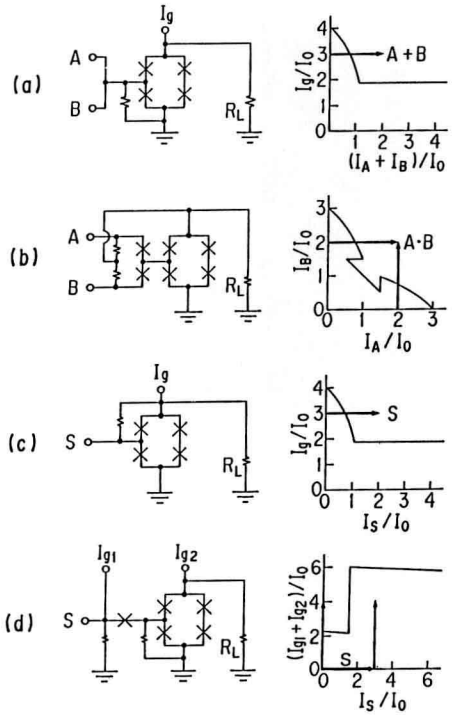

Fig.1. 4JL-family gates and their threshold curves.

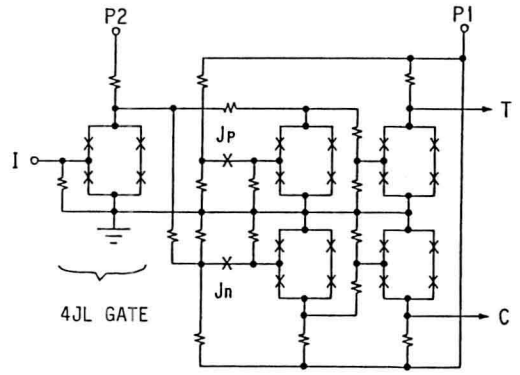

Fig.2. Direct-coupled data-latch.

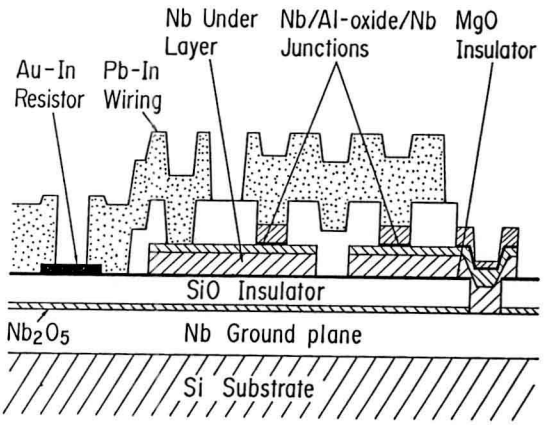

Fig.3. Schematic cross section of the circuit.

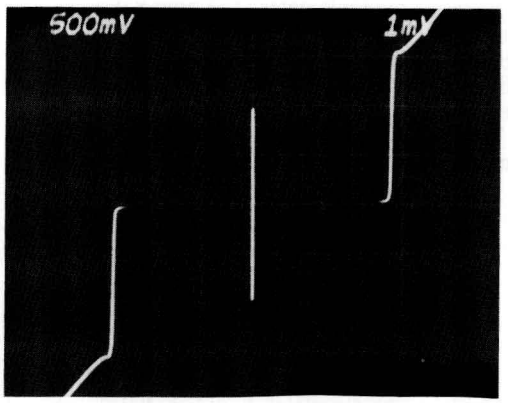

Fig.4. I-V curve of the Nb/Al-oxide/Nb junction. Vertical:0.5mA/div, horizontal:1mV/div.

film[11] protects a SiO layer on a ground plane during the RIE process. Insulations between each junction were performed with a self-aligned SiO evaporated film[12]. Interconnections of the junctions and Au-In resistors were done by Pb-In alloy wiring. An example of current-voltage characteristics of the Nb/Al-oxide/Nb junction fabricated is shown in Fig.4. A gap-voltage of 2.8mV and a Vm of up to 50mV are shown.

Josephson 2-bit ALU circuit[13] was designed using the 4JL-family gates. In order to obtain a high speed logic operations, a carry-look ahead logic is introduced instead of ripple carry one.

The circuit was designed based on the 3μm Nb/Al-oxide/Nb junction (Vg=2.8mV, Vm= 50mV) and an impedance(Zo =14ohm) of the 3μm-superconducting strip line. The 3μm OR-gate has a maximum gate current Im=0.2mA . The OR-gate can be operated at a nominal bias current of 0.75·Im with a power dissipation of 1.7μW.

The Josephson 2-bit ALU circuit was fabricated using the 3μm Nb/Al-oxide/Nb junction process. A photograph of the circuit fabricated is shown in Fig.5. 178 4JL-family gates are integrated in the circuit. The circuit size is about 0.8mm x 2mm.

The ALU was tested at 4.2K supplying monopolar pulse current to a power line with a Josephson regulator. Every ALU operation of 32 kinds of arithmetic/logic functions was confirmed completely. Delay time measurements of the ALU were also performed in the power current range between 50mA and 93mA. A constant delay time of 225ps was measured in the power current range between 50mA and 70mA at the operation of $\overline{A}$·B function. This constant delay time is due to a regulated power voltage which is delivered to each 4JL-gate. Figure 6 shows the output waveforms obtained for delay time measurement at the power current of 93mA, which gave the fastest operation. Time interval of two waveforms shows the delay time of 157ps which corresponds 12 stages of the logic gates. The power dissipation of the ALU is 580μW. By computer simulations, operating time of the ALU was estimated to be 180ps with a power dissipation of 261μW at the nominal bias condition.

The ALU was designed based on a bit-slice configuration which extends bit-length easily. 16-

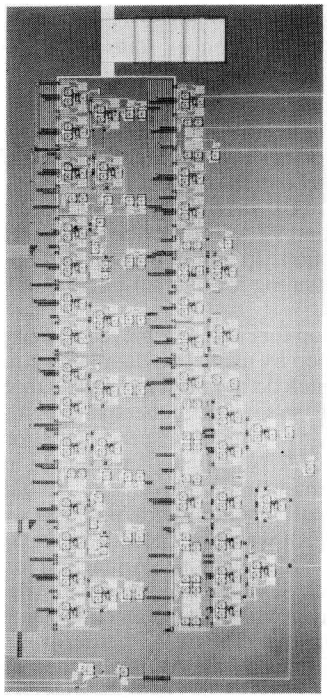

Fig.5. 2-bit ALU circuit fabricated with 3μm Nb/Al-oxide/Nb junction technology.

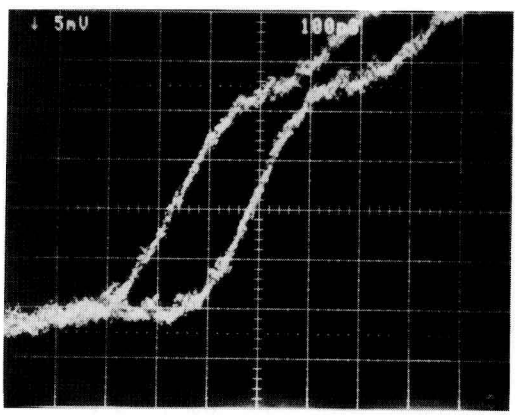

Fig.6. Output waveforms of the ALU for delay time measurement.

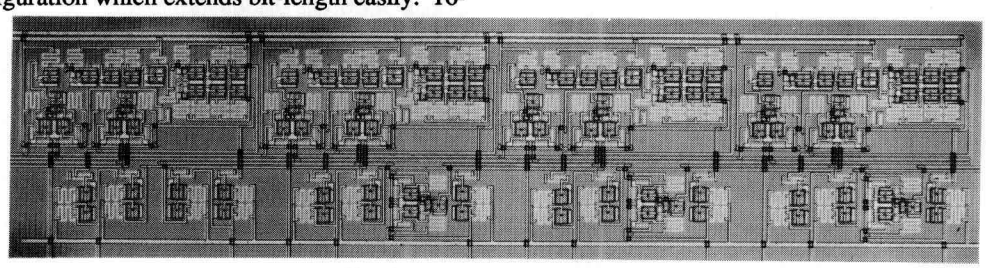

Fig.7. 4-bit digital counter.

bit ALU can be composed by connecting eight 2-bit ALU in parallel. Additional circuits which generate both generation and propagation signals are required for carry bits. In this configuration, the operating speed of the 16-bit ALU is estimated to be about 405ps.

A 4-bit digital counter[11] was designed using the 4JL-gate family and the directly-coupled data-latchs. Figure 7 shows a photograph of the 4-bit counter circuit which was fabricated with the 3μm Nb/Al-oxide/Nb junction technology described previously. The counter has three operating functions of counting, data-loading and clearing, adaptable for a program counter. The circuit size is 0.33mm x 1.4mm in which 103 4JL-gates are integrated. The counter was tested at 4.2K with the two-phase power supply, and the operations of every functions were confirmed. Operating speed of the 4-bit counter is estimated to be up to 3GHz with a power dissipation of 161μW.

A 4-bit shift-register[14] was also designed and fabricated. Figure 8 shows a photograph of the 4-bit shift-register circuit. The circuit size is about 0.3mm x 0.8mm. The register has four functions of shifting, data-loading, data-holding and clearing. Every functions were confirmed by supplying the two-phase power supply at 4.2K. The operating time is 195ps with a power dissipation of 116μW by computer simulations.

High speed multiplexer[15] was designed based on the 4JL OR-AND gate cell. Figure 9 shows the 4-bit multiplexer circuit fabricated using the 3μm Nb/Al-oxide/Nb junction technology. Four input signals are first stored in the latch to generate 4-bit dual outputs. In the second stage, the multiplexer circuit selects the one bit dual outputs from the 4-bits. The circuit tests were successfully carried out with the two-phase power supply. Every latch and multiplexer operation was confirmed. Operating delays were estimated to be 150ps and 60ps for the latch and the multiplexer, respectively.

These results show that the very complicated logic circuits such as CPU can be constructed by combining and extending these 4JL circuits developed here.

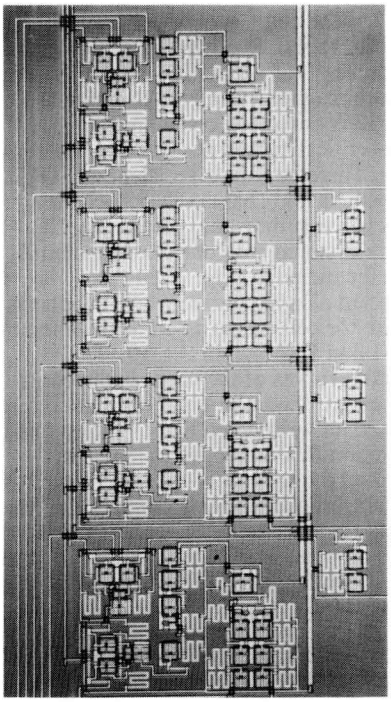

Fig.8. 4-bit shift-register.

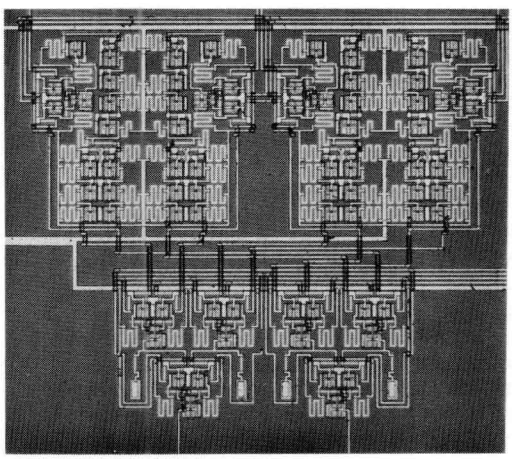

Fig.9. 4-bit multiplexer.

VARIABLE THRESHOLD MEMORY TECHNOLOGY

It is very important to realize memory devices for constructing Josephson digital systems. Considerable efforts have been done to achieve full operations of memory chips. A complete operation of Josephson memories, however, has not yet been achieved in LSI levels. A main reason is that the tolerance required for fabrication of Josephson memory circuits is smaller than that current technology can offer. Therefore, new approaches are needed in both the fabrication process and the memory circuit design. A refractory junction process has been recently developed which gives a good uniformity of the critical current in circuits. The variable threshold memory cell has been proposed and developed, which has a large operating margin[16].

The variable threshold memory cell has a very simple structure, i.e., an equivalent asymmetrical dc SQUID structure without a sense gate in it. Figure 10 shows a schematic configuration of the cell, in which one of two junctions of the dc SQUID is a three-junction SQUID gate J1 functioning as a write gate