PROCEEDINGS
SPIE—The International Society for Optical Engineering

Electro-Optic Computer Peripherals Technology

Eric G. Lean
Min-Shyong Lin
Chairs/Editors

16 December 1992
National Chiao Tung University
Hsinchu, Taiwan China

Co-Organized by
National Chiao Tung University
SPIE—The International Society for Optical Engineering

Cooperating Organizations
Asia-Pacific Optics Federation
Chinese Optical Engineering Society (Taiwan China)
Ministry of Education (Taiwan China)
Ministry of Transportation and Communications (Taiwan China)
National Science Council (Taiwan China)
Photonics Society of Chinese-Americans
SPIE Japan Chapter
SPIE Korea Chapter
SPIE Taiwan Chapter

Volume 1816

PROCEEDINGS
SPIE—The International Society for Optical Engineering

Electro-Optic Computer Peripherals Technology

Eric G. Lean
Min-Shyong Lin
Chairs/Editors

16 December 1992
National Chiao Tung University
Hsinchu, Taiwan China

Co-Organized by
National Chiao Tung University
SPIE—The International Society for Optical Engineering

Cooperating Organizations
Asia-Pacific Optics Federation
Chinese Optical Engineering Society (Taiwan China)
Ministry of Education (Taiwan China)
Ministry of Transportation and Communications (Taiwan China)
National Science Council (Taiwan China)
Photonics Society of Chinese-Americans
SPIE Japan Chapter
SPIE Korea Chapter
SPIE Taiwan Chapter

Published by
SPIE—The International Society for Optical Engineering

Volume 1816

Please use the following format to cite material from this book:
Author(s), "Title of paper," in *Electro-Optic Computer Peripherals Technology*, Eric G. Lean, Min-Shyong Lin, Editors, Proc. SPIE 1816, page numbers (1992).

Library of Congress Catalog Card No. 92-61853
ISBN 0-8194-1016-0

Published by
SPIE—The International Society for Optical Engineering
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone 206/676-3290 (Pacific Time) • Fax 206/647-1445

Printed in the United States of America.

Conference Committee

Conference Chairs

Eric G. Lean, Industrial Technology Research Institute (Taiwan China)
Min-Shyong Lin, Industrial Technology Research Institute (Taiwan China)

Program Committee

Soo-Jin Chua, National University of Singapore (Singapore)
Golden Diau, Industrial Technology Research Institute (Taiwan China)
Eberhard P. Hofer, Universität Ulm (Germany)
Steve Lai, IBM Korea, Inc. (Korea)
Shu Chien Liang, Sampo Ltd. (Taiwan China)
C. Lin, Bell Communications Research (USA)
Wei-Yuan Lin, Photon Imaging International, Inc. (Taiwan China)
Kohki Noda, IBM Japan Ltd. (Japan)
Frank E. Talke, University of California/San Diego (USA)
Chung Y. Ting, Trace Storage Technology Corporation (Taiwan China)
Chia-yu Yen, National Taiwan University (Taiwan China)

Session Chairs

Session 1—Plenary Session

Session 2—Hard Disk Drive Technology
Eric G. Lean, Industrial Technology Research Institute (Taiwan China)

Session 3—Optical Disk Drive Technology
Frank E. Talke, University of California/San Diego (USA)

Session 4—Other Peripherals Technology
Min-Shyong Lin, Industrial Technology Research Institute (Taiwan China)

Session 5—Poster Presentation

OCCC '92 Symposium Committee

Symposium Chairs

Sien Chi, National Chiao Tung University (Taiwan China)
Pochi Yeh, University of California/Santa Barbara (USA)

Technical Program Chairs

S. T. Peng, National Chiao Tung University (Taiwan China)
Bor-Uei Chen, Optical Communications Products, Inc. (USA)

Local Advisory Committee

Ming-Wen Chang, National Central University (Taiwan China)
Louis S. Chou, Ministry of Transportation and Communications (Taiwan China)
Ching-Piao Hu, National Science Council (Taiwan China)
Peter S. C. Shih, National Science Council (Taiwan China)
Ching-shen Su, National Tsing Hua University (Taiwan China)
T. K. Wang, National Science Council (Taiwan China)

Intersociety Liaison

T. Russell Hsing, Bell Communications Research (USA)

Introduction

Computer peripherals, which include input devices, storage, output devices and communication, are the essential parts of a computer system. The ever-increasing power of computer processing demands rapid advances in the performance of peripherals to avoid the bottleneck of information processing. The technological progress in electro-optical computer peripherals has been very rapid. The technical innovations and competitive market have accelerated cost reductions and user acceptance of many electro-optic computer peripherals. Computer peripherals have grown to be a hundred-billion-dollar industry.

This year's SPIE conference has devoted a whole day to discussion of the recent advances in computer peripherals technology. Papers that will be presented include invited talks on optoelectronic high-speed and high-power devices, optical fiber communication, and magnetic and optical storage technologies from well-known scientists and engineers from Japan, the USA, mainland China, and Taiwan China. Many interesting contributed papers will also be presented.

Eric G. Lean
Min-Shyong Lin
Industrial Technology Research Institute (Taiwan China)

Contents

SESSION 1

Plenary Session

Invited Paper

Optoelectronics high power control devices

Jun-ichi Nishizawa*,** and Kazushi Dezaki**

* Tohoku University
Katahira Aoba Sendai, 980 Japan
** Semiconductor Research Institute
of Semiconductor Research Foundation
Kawauchi Aoba Sendai, 980 Japan

ABSTRACT

Light Trigger and Light Quench Static Induction Thyristor (LTLQ-SIThy) is described on the optical triggering and quenching mechanism. The Static Induction gate structure provides the high turn-on gain. Static Induction Photo Transistor (SIPT) is used for the quenching device. The SIPT gives the high gain of the LTLQ-SIThy at turn-off. This functionally integrated power device propose the high efficiency to switch the large energy. The new LTLQ-SIThy which utilizes the LQ-SIThy for the quenching device is reported. This LTLQ-SIThy is improved the switching ability in the large current, the dependency of temperature and the controllability by the trigger/quench light.

1. INTRODUCTION

It is possible that the Static Induction Photo Transistor (SIPT), the Light Trigger SI Thyristor (LT-SIThy), Light Trigger Light Quench SIThy (LTLQ-SIThy) and Double Gates type of LTLQ-SIThy designate to the Optoelectronic High Power Devices. Among these devices, the LTLQ-SIThy is evolved to the high power device that the several item to scale up to the large current device have been solved by utilizing the advantage of SIThy. The device structure of the LTLQ-SIThy[1] was invented by J.Nishizawa et.al. in 1979. The SIThy is the main switch of LTLQ-SIThy, which was invented by author (J.N.) in 1972 (fig.1)[2]. The SIThy with the step gate structure has been developed up to the data rate of 4000V 400A[3,4]. The SIThy with planer gate structure[5,6] has reached the very high speed operation of 2MHz switching. SIThy obtained the expectant characteristics which are high speed, high gain and high efficiency.

A regulation of the power should be controlled by the least energy and should be isolated from main current flowing. It had been desired that the LTLQ-SIThy which has the SIPT[7] as the quenching device was produced as HVIC (High Voltage Integrated Circuit) on the monolithic silicon chip. In 1984, this LTLQ-SIThy which was controlled by the irradiation of LEDs (Light Emitting Diodes) showed the high gain $10^4/10^6$ at turn-on / turn-off in the switching operation at 400V 1A[8]. The DG (Double Gates)-SIThy[9] with the 1'st planer gate and the 2'nd buried gate was presented in 1985. This sophisticated device showed high performance in switching operation[10]. In 100V 1A operation, the turn-on time is 0.2 μsec and the turn-off time is 0.3 μsec with a few tail current. Also the DG-SIThy could been driven by LED's light irradiation for turn-on / turn-off. This LTLQ-DG-SIThy should be the light control power device with very high speed. In 1989, the LTLQ-SIThy progressed to the capability of 1200V 40A. This device demonstrated the high ability that the rise times of current was 1.8 μsec and the fall time was 1.7 μsec[11].

In the recent development, the new functional integrated LTLQ-SIThy which is

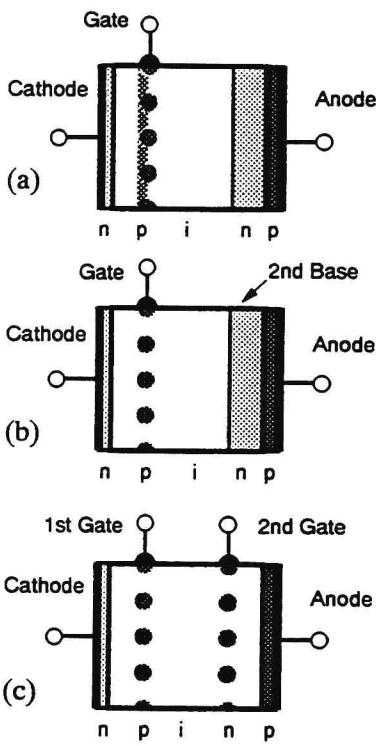

Fig.1 The ideas of (a) beam base thyristor, (b) Single Gate SIThy, (c) DG-SIThy.

0-8194-1016-0/92/$4.00

enhanced from the previous LTLQ-SIThy has a LT-SIThy as the quenching device[12]. This new integration improves the dependency that the switching time relates to the main current, the working temperature and the light intensity to trigger/quench. To switch high voltage and large current, the new quench device of LT-SIThy assists to stabilize switching operation. Because the LTLQ-SIThy utilize the SIThy for the switch of the main current, the LTLQ-SIThy is possible to switch as large current and high voltage as a SIThy. Therefore, all property of the SIThy is succeeded to this functional device.

In this paper, SIThy's characters of high speed switching, high gate gain and low dissipation are introduced. The basic analysis of SIPT and LT-SIThy lead the study of turn-on mechanism and the reason of a high gate gain. The turn-off procedure of LTLQ-SIThy is described. The turn-off time is diminutive, because all of the holes of main current in the channels are able to pull out effectively by the function of the SI gate structure. In the recent time, several functional integrated devices which are called MCT (MOS Controlled Thyristor) and IGT (Insulated Gate Transistor) are developed. In the former, a *pnpn*-thyristor combines with a MOSFET as a cascoded connection. In the latter, bipolar transistor is integrated with MOSFET. It is different from these devices that a on-state current of the LTLQ-SIThy flows only in its *pin* structure. It is significant that the LTLQ-SIThy maintains the character of low forward voltage drop.

2. PRINCIPLE OF THE HIGH SPEED, HIGH GAIN, AND LOW LOSS SITHY

The SIThy is the main switch of the LTLQ-SIThy. The basic investigation of the SIThy induces the study of the LTLQ-SIThy.

2.1 Operation of SIThy

The buried gate structure of the SG-SIThy is shown in fig.2. The SIThy consists of a *pin* rectifier structure in which a gate junction has been introduced to control the current flow from the anode to cathode. In the presence of a gate bias, the depleted region around the gates connect to together. When forward voltage is added to the anode against the cathode, $p+$ base of the gate and $n-$ 2nd base are biased inversely. Fig.3 shows the potential of diagram such an off-state condition. In fig.3, the dotted line indicates the potential diagram from cathode to anode which passes through intrinsic gate G* (in fig.2) and the solid line indicates the potential diagram from cathode to anode which passes through the center of the gate. In order to turn to the on-state, a positive bias is added to the gate. This is the start of latch-up process as follows. That is, electrons are injected from cathode to 2nd base. Electron injection decreases 2nd base potential. Hole defuses to 2nd base area from the anode. Holes which reach to the gate attain the gate to more positive potential. This results in that the amount of electron and hole increase. As mentioned above, the positive feedback establishes on-state in latch up condition. In order to turn to the off-state, the negative gate voltage depletes the holes which pull up the potential of the gate. The gate which has a low resistivity can pull out the holes in the channel competently. This gate potential stops the flow of electrons and holes. But in the 2nd base, electrons are burnished by the recombination of the holes which are injected from the anode.

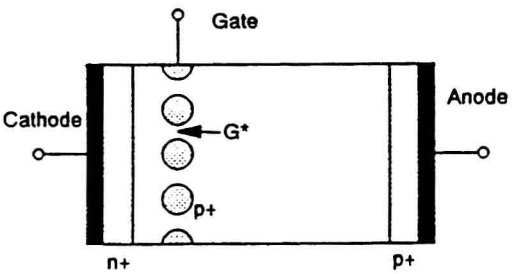

Fig.2 Cross sectional view of the simple SIThy's model.

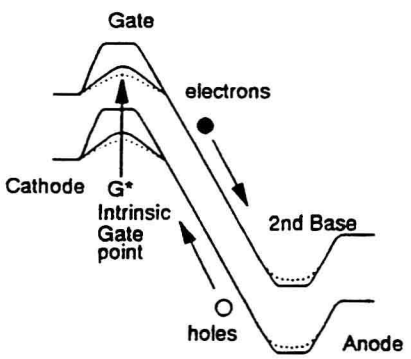

Fig.3 Energy potential diagram of the Single Gate SIThy.

2.2 High speed switching

The gate energy to turn on is very small. To trigger on, few of holes which injected from the gate are required to

pull down the center of the potential barrier between the gates. As mentioned in previous part, only this electricity of holes induces to inject the hole which rise up from the 2nd base. The delay time of turn-on depends how fast pull out all the electrons which build the depletion areas around the gates. The capacitance between the gate and the cathode and resistance of the gate fingers are the parameter of the turn-on time[13]. In the case of the SIThy, the small electricity of gate is neutralized by holes which is delivered from the low resistivity of the gate finger.

To turn off, all the holes in the channel must be extracted from the gate electrode. Under the condition that the gate have a sufficient voltage, the gate blocks the leak current from cathode to gate. The change of the electricity in the channel can describe as the Equ.(1).

$$-\frac{dQ}{dt} = I_{gp} + \frac{Q}{\tau_{eff}} \qquad \text{--- (1)}$$

Q: The electric charge of the hole in the channel.

I_{gp}: The maximum of the gate current.

τ_{eff}: The effective life time considering the auger's recombination.

The time of $Q = Q_{on}$ (a value of on-state) to $Q = 0$ is the turn-off time (t_{off}). t_{off} is shown by integration of Equ.(1).

$$t_{off} = \tau_{eff} \ln (1 + \frac{I_a}{I_{gp}}) \qquad \text{--- (2)}$$

I_a: Anode current.

The turn-off time depends τ_{eff} and I_{gp}. When $I_a = I_{gp}$, t_{off} takes the minimum value of ($\tau_{eff} \cdot \ln 2$). The Fig.4 shows the result of calculation of Equ.(2). When turn-off anode current is increased, the electron density in *n*- layer is increased. The effective life time depends on density of electrons[14].

2.3 Current gain at turn-off

From the description of Equ.(2), when the maximum gate current (I_{gp}) is equal to the anode current (I_a), the turn-off time can takes the least value. The relation of the gate voltage and the gate resistance is Equ.(3).

$$I_{gp} = \frac{V_{gk}}{R_g} \qquad \text{--- (3)}$$

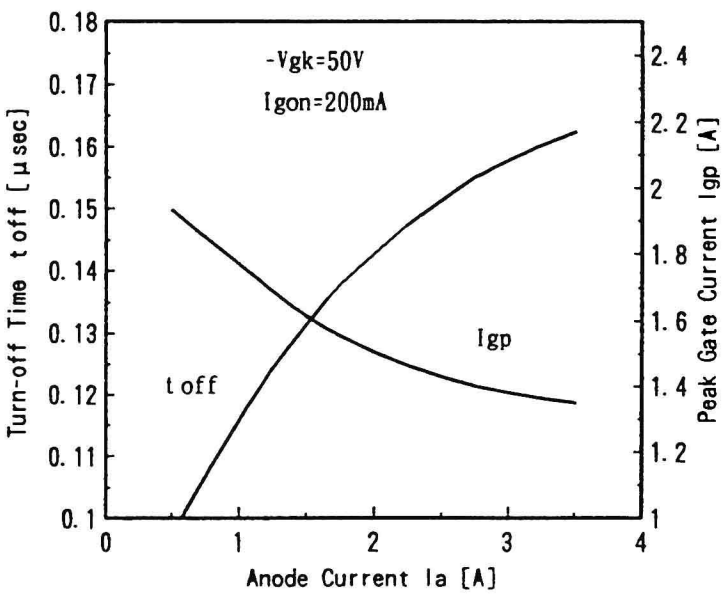

Fig.4 Calculated result of equ.(1). The relations of the turn-off time and the peak gate current with the anode current.

The low resistance of gate of SIThy is suitable for realizing of $I_a = I_{gp}$. In the case of SIThy, the real power of gate driving is small in spite of gate gain which is equal to 1, because the time of turn-off process is a short. However, the gate current can be flowed to the main current by a gating method. In this way, the gate gain of I_a / I_{gp} is very high. This method is taken in the later chapter of the LTLQ-SIThy.

2.4 Forward voltage drop at on-state

The high efficiency of SIThy is consisted by not only the fast switching but also the high conductivity in on state. As the model of the forward voltage drop, a *pin* diode which has the same area of main current channel is able to be suggested. In this model, the voltage at on state (V_f) is described the summation of tree terms as follow.

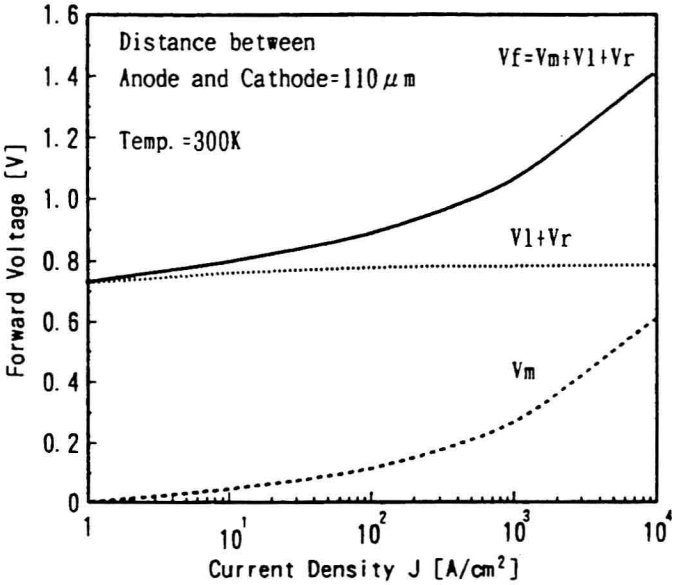

Fig.5 Calculated result of the forward voltage drop for the anode current density.

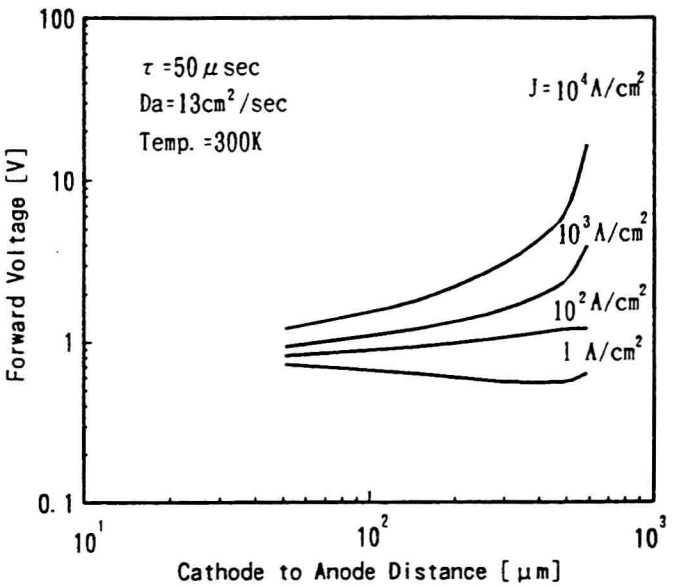

Fig.6 The characteristics between the distance of the cathode to anode and the forward voltage drop.

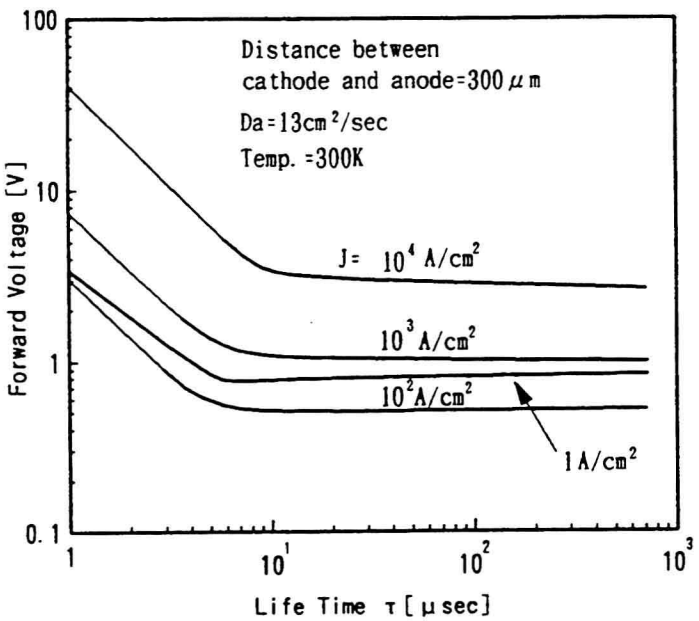

Fig.7 The contribution of the life time of the channel to the forward voltage drop.

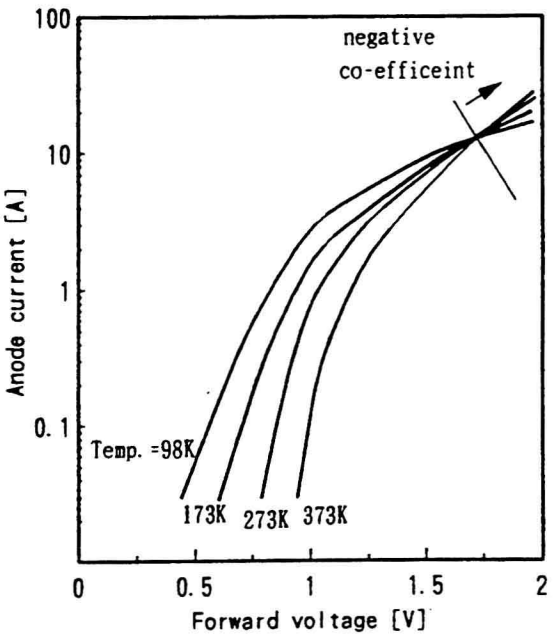

Fig.8 Characteristics of the anode current and the forward voltage drop under the latch-up condition. The negative co-efficiency is indicated.

$$V = V_m + V_l + V_r \qquad \text{--- (4)}$$

V_m: The resistance of $n-$ layer.
V_l: The built-in potential of $p+n-$ junction.
V_r: The built-in potential of $n+n-$ junction.

The results of this model[14] shows Fig.5 ~ Fig.7. As shown Fig.5, in the higher region of the current density, the resistance of $n-$ layer is major.

The forward blocking voltage and the forward voltage drop depend on the thickness of the $n-$ layer. The relation between the thickness of $n-$layer and forward voltage are shown in several current density as Fig.6. Fig.7 indicates that in the case of fat $n-$ layer, the effective life time (τ_{eff}) effects to the voltage at on-state. The characteristics of I_f and V_f is measured at several temperature. The Fig.8 shows that the SITHy has a negative co-efficiency to the temperature in the high density current region. In this region, the voltage drop by $n-$ layer is major. Therefore, the SIThy operates with a high conductivity and a negative coefficient of temperature in the high current density region.

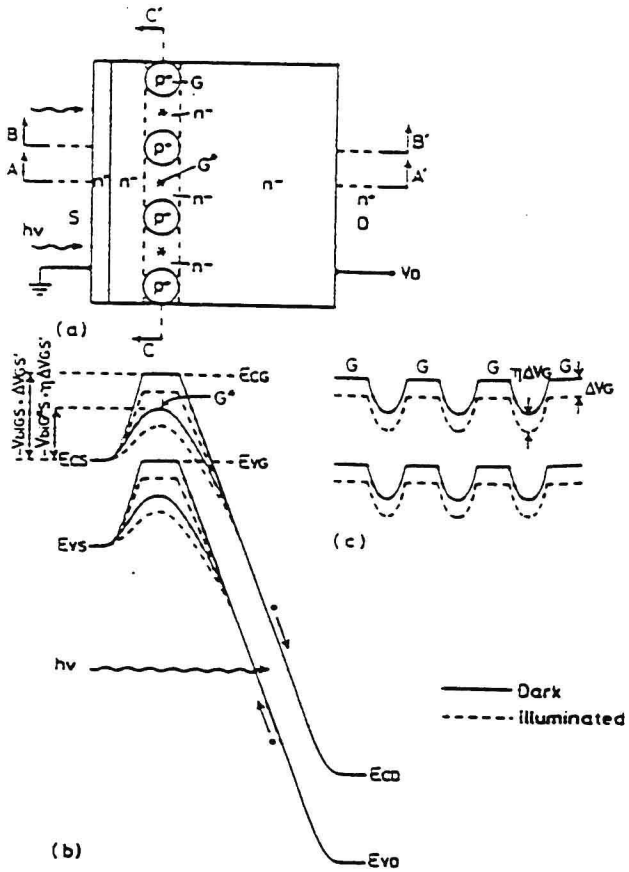

Fig.9 Operational principle of SIPT. (a) Schematic device cross section. (b) Energy potential diagram at the cross section surface in A-A' and B-B' line.(c) Energy potential diagram at the cross section surface in C-C'.

3. SIPT

In this chapter, the operation of SIPT is introduced. The SIPT is the quench device of LTLQ-SIThy. The high optical gain of the SIPT devote to the turn-off gain of the SIThy.

3.1 Structure and energy potential

A schematic cross section of the buried gate type SIPT is shown in fig.9(a), where the $p+$ region G, $n+$ region S, $n+$ region D, and $n-$ region C indicate gate, source, drain and channel regions, respectively. Fig.9 shows the energy potential diagram at the cross section surface of the B-B' line of the $p+n-n+$ region and the A-A' line of the $n+n-n+$ region in fig.9(a) on the same plane. Fig.9(c) shows the potential diagram at the cross sectional view of the C-C' line of the $p+$ gate region in fig.9(a). Fig.9(b) and fig.9(c) are dimensionally scaled in fig.9(a). When the SIPT is irradiated from the $n+$ source surface to the deeper portion of the $n-$ channel region, electron-hole pair are generated in the depleted channel region, and photo-generated holes accumulate at the $p+$ gate region surface, because the $p+$ gate region of the SIPT is the minimum region of the potential for the holes, as shown in fig.9(b) and fig.9(c). Even in the dark condition, the height of the potential barrier for electrons at the intrinsic gate point G* is lowered by the value of $\eta \Delta V'_{GS}$, because generated holes in the dark condition can accumulate in the $p+$ gate region by the value of the ΔV_{GS}. In the illuminated condition, the height of the potential barrier for electrons at the G* point is lowered by the value of $\eta \Delta V_G$. A comparison of the dark condition is shown in fig.9(b) and (c). In these figures, the solid line is the

schematic potential diagram in the dark condition, and the dotted line is the potential diagram in the illuminated condition. The value η indicates the effectiveness of the gate potential variation on the intrinsic gate point G* potential variation. Therefore, the height of the potential barrier for electrons in the source region becomes $-V_{biG^*S} + \eta V'_{GS}$ for the dark condition and $-V_{biG^*S} + \eta(V'_{GS} + \Delta V'_{GS})$ for the illuminated condition. On the other hand, The height of the potential barrier for holes stored in the gate region becomes $-V_{biGS} + V'_{GS}$ for the dark condition and $-V_{biGS} + \Delta V'_{GS} + \Delta V_G$ for the illuminated condition. Because the potential barrier height for holes is very controllable by the incident photon, high current gain can be expected in SIPT. A large current gain capability and very high efficient optical triggering and quenching mechanism of the SIThy occurs due to the same mechanism. This device can be used as a solid state image sensor[7].

3.2 Operation

A schematic diagram of the cross sectional view of the experimental normally-off type SIPT is shown in fig.10(a). Fig.10(b) shows the calculated optical absorption rate $\exp(-\alpha x/2)$ values versus penetration depth x[μm] in the direction from the $n+$ source surface to the drain, using the absorption coefficient α data of reference[15]. The position of the source region depth (x = 0.5μm), the position of the gate region depth (x = 2.6μm) and the thickness of the $n-$ layer (x = 5μm) are indicated in this figure. It is obvious that the depth of the $p+$ gate region and the thickness of the $n-$ layer are important device parameter. In fig.10(c), photo-generated holes are indicated by open circles which are mostly crowed near the $p+$ gate region, resulting from the fact that photo-generated holes drift to and are stored at $p+$ gate region surface according to the energy potential for the holes as shown in fig.10(c). The length of the allow indicators shows the intensity of the electric field according to the energy potential for the holes schematically.

The experimental circuit diagram and a schematic relationship between current-voltage characteristics of the normally-off type SIPT as a function of the incident optical power (P_i) and the output load line are illustrated in fig.11[16]. The gate terminal of the SIPT is opened and the gate is only biased by the photo-generated and stored holes in the $p+$ region, because the normally-off type SIPT can be operated in the forward direction of the gate potential from the dark condition to the illuminated condition by increasing the intensity of the incident light P_i as shown in fig.12. The drain terminal of the SIPT is biased to the V_D by the drain voltage source V_{DD} through the load resistance R_L.

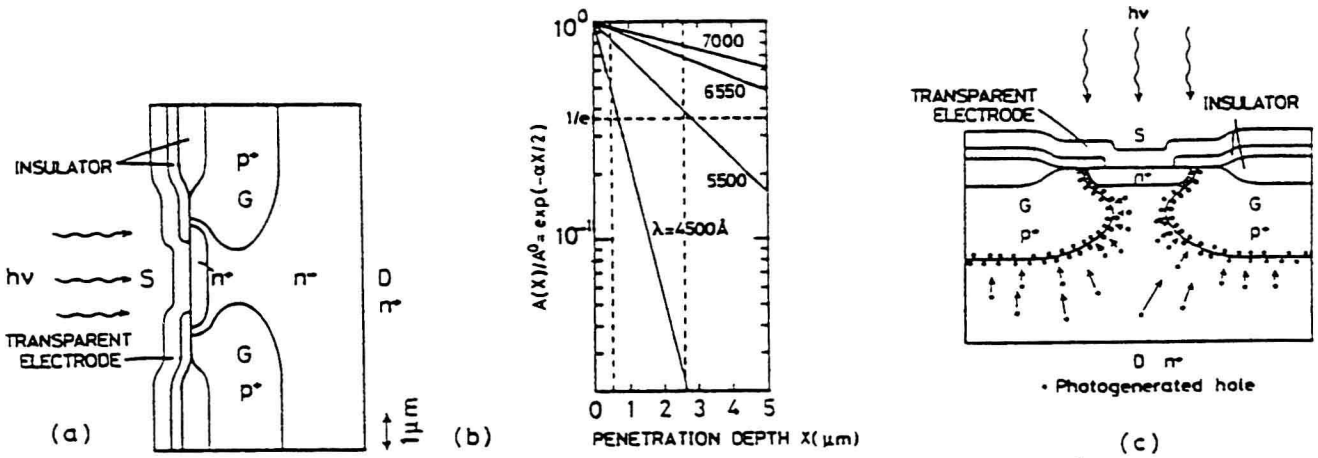

Fig.10 Experimental normally-off type SIPT. (a)Schematical cross sectional view of the measured SIPT. (b)Calculated optical absorption rate $\exp(-\alpha x/2)$ vs penetration depth x for four difficult wave length λ corresponding to the device vertical dimension shown in (a). (c)Schematic of accumulation process of photo generated holes.

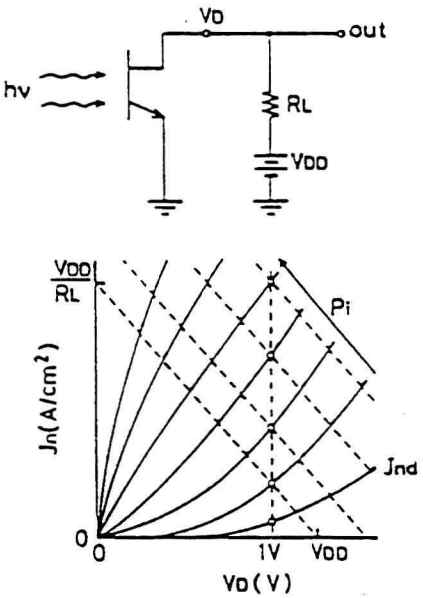

Fig.11 Optical circuit diagram and current–voltage characteristics (solid lines) of normally–off SIPT and output load line (dotted lines), open circles indicate bias point (Jn, VD).

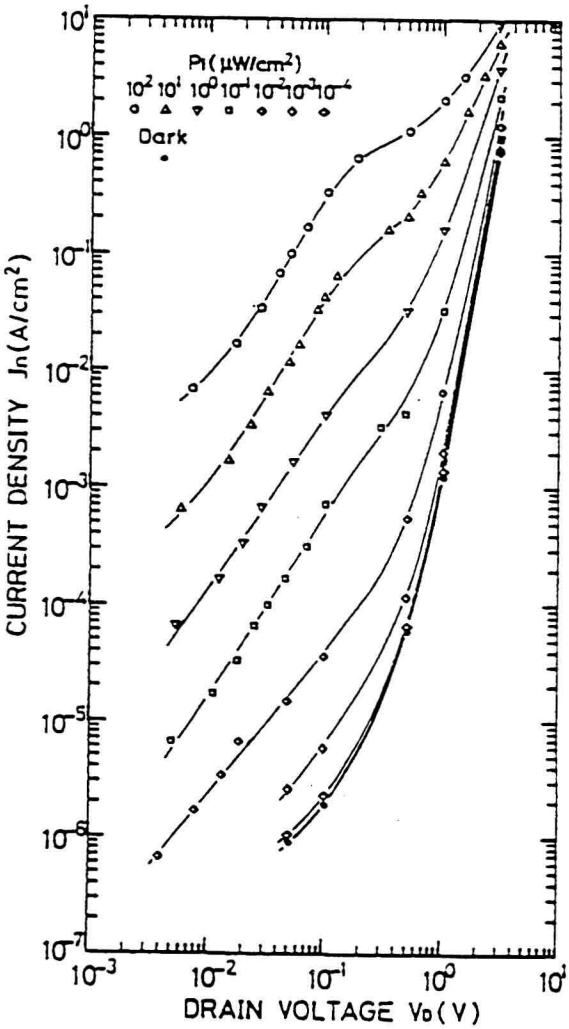

Fig.12 Electron current density Jn vs drain voltage VD characteristics of the normally off SIPT for several intensity of the incident power Pi.

4. LT-SITHY

4.1 Principle of Operation

Fig.13 shows the schematic device cross section of the buried gate SIThy having a quenching p channel SIPT. The incident light directly irradiated on the surface of the SIThy is refracted through the beveled surface between the gate and cathode electrodes and can penetrate into the $n-$ layer so as to generate electron-hole pairs in the depletion layer. Fig.14 shows the energy potential diagram and the equivalent circuit at the cathode side of the SIThy in the forward blocking state. Photo-generated holes are stored at the $p+$ gate region, because this region is the minimum position of the energy potential for the holes. Photo-generated electrons are stopped at the $n-$ base near the $p+$ anode region. When the gate potential is positive biased ΔV_G by the excessive stored holes, the potential barrier height for the electrons in the $n+$ cathode region is lowered to $V_{biG*K} - \eta \Delta V_G$, although the stored holes in the $p+$ region have a large barrier height of $V_{biGK} - \Delta V_G$. When the gate terminal of the SIThy is opened, the maximum directional current optical gain of the static induction gate structure at the cathode side is approximately given by equ.(5) as low as the incident optical power.

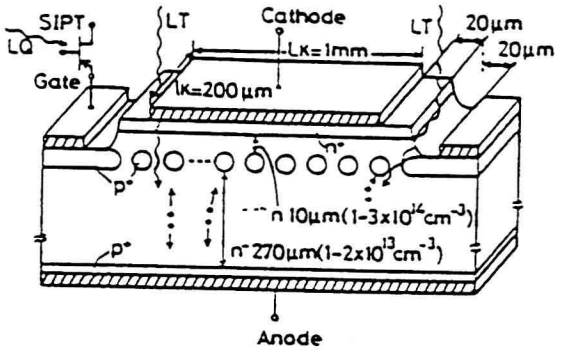

Fig.13 Schematic device structure of the single gate SIThy with p channel SIPT.

$$G_{Kmax} = \frac{n_K}{p_G} \cdot \frac{D_n/W_G}{D_p/L_p} \cdot \exp\left[\frac{q}{kT}(V_{biGK} - V_{biG*K})\right] \quad \text{--- (5)}$$

n_K: The electron concentration of the cathode region.
p_G: The hole concentration of the gate region.
D_p: The diffusion constant of holes.
W_G: The effective potential width.
L_p: The diffusion length of holes.
q: The unit charge.
k: Boltzmann's constant.
T: The absolute temperature.
V_{biG*K}: The built-in potential between the gate and cathode at G*.

The term $(D_n / W_G) / (D_p / L_p)$ shows the ratio of the electron injecting velocity to the hole diffusion velocity. Because the exponential term has a very large value, the current gain of the SIThy at the cathode side is much larger than those value of the *conventional* Light Trigger Thyristor.

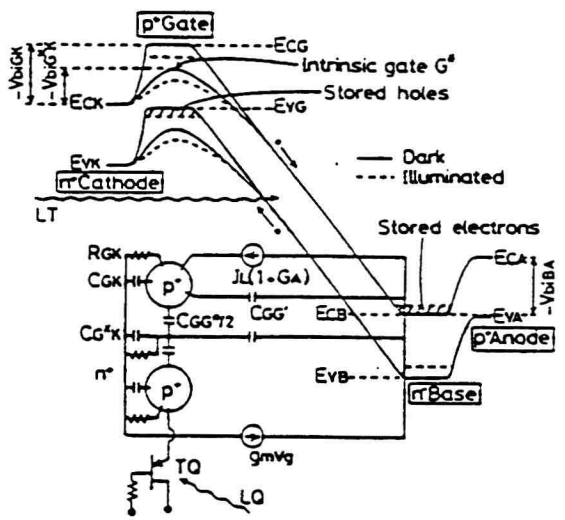

Fig.14 Energy potential diagram of the single gate SIThy and an equivalent circuit at the cathode side.

5. LTLQ-SITHY USING SIPT FOR QUENCHING DEVICE

Several types of the LTLQ-SIThy are proposed by J.N. as shown in fig.15[17]. In this chapter, the LTLQ-SIThy of type (a) which was fabricated to prove the performance of the SIThy is featured. This type of the SIThy was fabricated the rating of the 1200V 40A in 1988.