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PAPER NOT RECEIVED IN TIME FOR PUBLICATION*

PC-Based X-ray Micro-Fluorescence Analyzer
for Plating Thickness and Composition Analysis

William Silverman, Veeco Instruments, Inc., Syosset, NY

Since introduction in 1981 of X-ray micro-fluorescence instrumentation dedicated to measurement of plating thickness and composition, major advances have been made in the analytical capabilities of these systems. Through use of the personal computer, computational power and data storage of the analyzer section have been dramatically increased. The PC greatly simplifies implementation of enhanced software features that support new application capabilities and provide an entirely new user interface. Recent advances relating to precision, accuracy, smaller X-ray beam size and new plating thickness/composition applications will be discussed. A description will be presented of the ergonomic improvements that afford immensely simplified instrument usage without sacrificing power and performance.

* For copies of this paper, please contact the author directly.

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PAPER NOT RECEIVED IN TIME FOR PUBLICATION*

The "Total Control" Concept for the CVS Analysis of the PWB Plating Systems

Dr. Peter Bratin, ECI Technology, Plainview, NY

The progress made in the PWB industry over the past decade, combined with new environmental laws, have placed additional demands on the control and analysis of plating solutions and waste water. Quality demands are increasing, down-time must be minimized, and it has become impractical and expensive to simply dump the plating baths when they get out of control.

During the past decade, few analytical methods usable in plating industry have seen the upsurge comparable to the Cyclic Voltammetric Stripping (CVS). The technique has achieved wide acceptance in the industry for control of organic additives in various plating solutions.

This presentation will discuss new improvements of the technique to satisfy some of the most demanding applications. This includes topic of "total control", including control of additives and their components in copper, solder, and nickel additives and their components in copper, solder, and nickel solutions; keeping contamination under control, checking activity and contamination in cleaners, predips, and etchants; incoming inspection of raw materials; and carbon treatment process. Other topics to be discussed in this presentation will be on-line control and statistical process control, and their role in the "total control" concept.

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Chemical Vapor Deposition of Metals for VLSI Applications

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Metal films play vital roles in the operation of a VLSI circuit. Gate, contact, diffusion barrier, interconnect and via fill metallization applications bring various requirements to bear on these films and the way in which they are deposited. These films can be deposited using a variety of deposition techniques such as sputtering, evaporation or chemical vapor deposition. Each technique has its own merits and drawbacks, which have been discussed in detail.[1] This paper focusses on the chemical vapor deposition (CVD) of metals for VLSI applications, a field which is currently of great interest and whose applications are in their infancy compared to evaporation or sputtering. CVD metals processing offers solutions to VLSI metallization problems arising from the small ($\lesssim$1 μm design rules) dimensions typical of such devices.

CVD is the deposition of a solid film on a substrate, brought about by the reaction of one or more vapor phase species. Typical deposition reactions include pyrolysis, reduction, oxidation, hydrolysis, disproportionation, or combinations of these, and are usually catalyzed by the substrate. The ability to deposit a particular film depends only on favorable thermodynamics and kinetics for the chosen reaction, and the availability of vapor sources for the reactants.

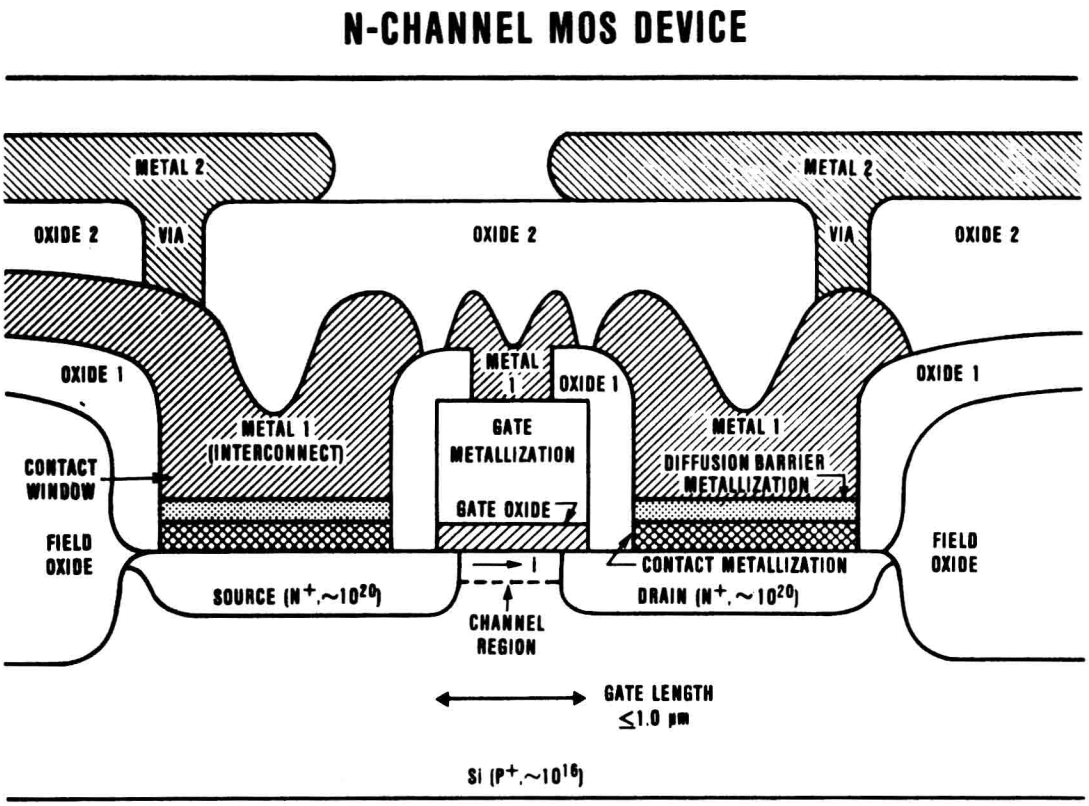
The advantages of CVD processing are best discussed in the context of metallization applications on a VLSI circuit device. Figure 1 is a schematic diagram of an N-channel MOS device which features a multilevel metallization scheme. Each of the five metallization applications on this device, i.e., gate, contact, diffusion barrier, interconnect and via fill, represents a challenge in thin film processing that can be addressed by CVD. The materials and processing requirements for the various metallizations will now be summarized.

Gate Metallization. The gate is deposited early in the VLSI processing scheme, and will be exposed to subsequent high temperature processing steps ($\lesssim$950°C), sometimes in oxidizing atmospheres. Therefore, high melting temperature and oxidation resistance are important for this application. CVD films of the refractory metals Mo,[2,3] Ru[4] and W[5] have been studied as gates, but their oxidation has to be prevented (not necessary for the case of Ru, whose oxide, RuO_2, is itself a good conductor[4]).

Contact Metallization. The contact between the metallization and the silicon substrate may be rectifying (i.e. a Schottky contact), or ohmic. Usually, the function of the contact metallization is to provide low resistance, ohmic contact between it and the Si and it and the interconnect metallization. However, CVD processing has been used to create both kinds of contacts. Schottky contacts have been formed with Cr[6], Mo[7,8], V[9] and W[10]. Low resistance ohmic contacts have been formed by CVD of Ag[11], Mo[12,13], Pt[14] and W[15-17]. Many CVD reactions automatically result in intimate contact between the deposited metal and the substrate due to the consumption of a thin layer of the substrate during deposition.

Interconnect Metallization. The primary requirements for interconnects are low resistivity and good electromigration resistance. Al has low resistivity (2.7 μΩ-cm), but poor electromigration

resistance due to its low melting point. However, alloying improves this greatly.[18] Higher melting point metals such as W have excellent electromigration resistance, but higher resistivity than Al. Al,[19-22] Mo[23,24] and W[25-29] have all been evaluated as CVD interconnect metallizations, their major advantage being conformal coverage.



1) Schematic diagram of a multilevel (two) metallized N-channel MOS device. Dopant concentrations in the various Si regions are expressed in atoms/cm^3.

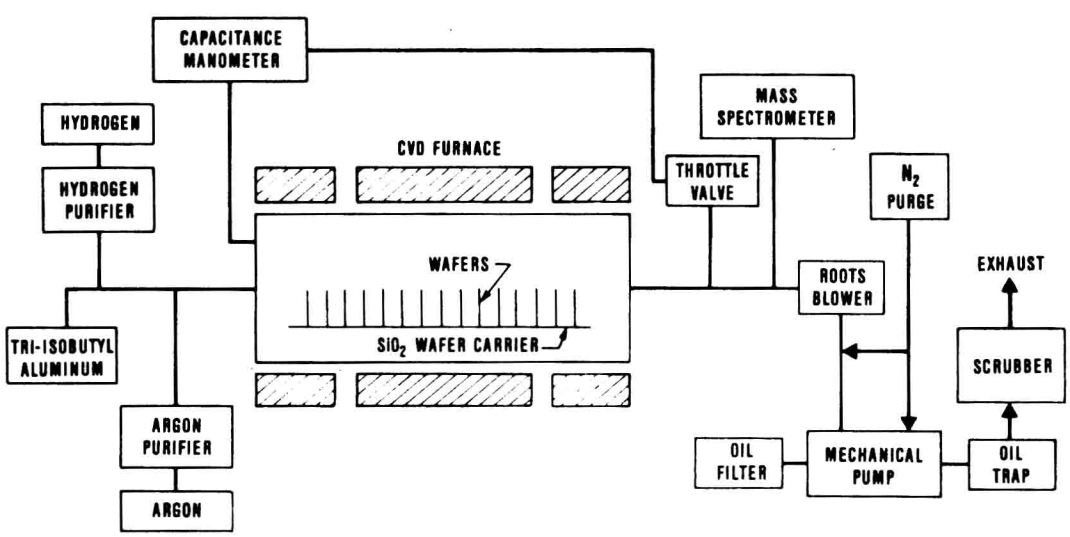
Via Fill or Planarization Metallization. Multilevel metallization gives rise to the need to fill vias that connect one level of interconnect metallization to another. CVD processing is well suited for this due to the conformal coverage that its films exhibit. Blanket deposition of CVD W followed by etchback[30-32] is one scheme for forming plugs in vias. Another technique involves the deposition of highly selective CVD W in the vias,[33-38] after which no etchback is required.

Table I compares the salient features of CVD processing with those of the physical vapor deposition techniques, sputtering and evaporation. Film characteristics such as conformal coverage and high purity, and processing benefits such as low temperature and radiation-damage free deposition and deposition selectivity allow one to make high quality films by CVD processing. At the same time, the high throughput and correspondingly low cost per wafer associated with traditional CVD processing make it an economically attractive process.

Figure 2 is a schematic illustration of a typical hot-wall, horizontal LPCVD (low pressure) reactor. The reactants are pumped through the furnace, at which point they react to deposit a film on the substrates. The gaseous by-products are then pumped out of the system. Source materials, which are either gases, or liquids or solids with high vapor pressures, can be obtained in very pure form.

TABLE I. Comparison Between Chemical Vapor Deposition and Physical Vapor Deposition (Sputtering and Evaporation)

	CVD	Sputtering	Evaporation
Step Coverage	Conformal	Nonconformal (line-of-sight)	Nonconformal (line-of-sight)
Low Temperature Deposition	Yes	Yes	Yes
Radiation Damage	No	Yes	Yes (Electron-beam evaporation)
Selectivity	Possible	No	No
Film Purity	Good-Excellent (Process Dependent)	Good-Excellent (Gas Incorporation)	Excellent
Wafer Throughput	~100/hr	~60/hr	~30/hr
Relative Processing Cost per Wafer	Low	Medium	High

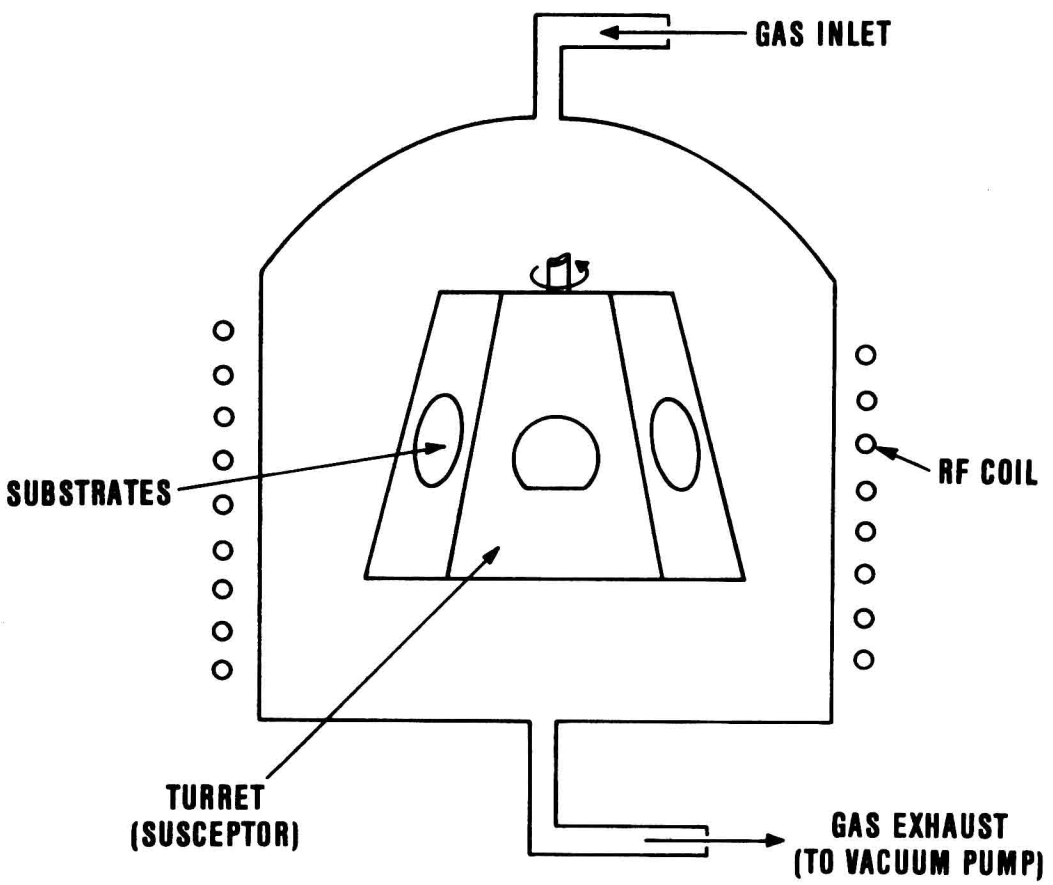


2) Schematic diagram of a hot-wall low pressure CVD system, such as might be used for the deposition of Al from tri-isobutylaluminum.

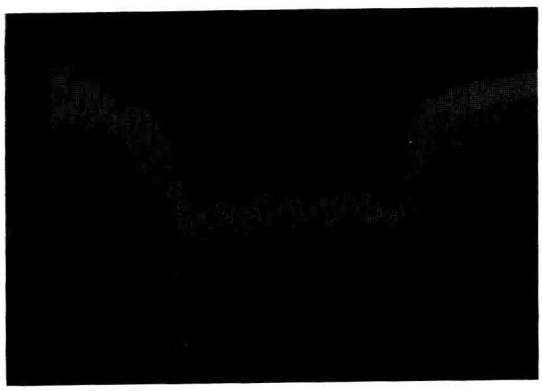
The reactor depicted in Fig. 2 can be used, for example, to deposit Al or W films. However, two current trends in CVD processing are the use of cold-wall reactors, Fig. 3, and the use of single-wafer reactors. Cold-wall reactors keep film contamination due to gas phase nucleation of particles to a minimum because only the wafers and the heater block on which they sit get hot. Cold-wall reactors have been found necessary to achieve the high degree of selectivity of CVD W that has recently been observed.[36] Single-wafer reactors are a variant of cold-wall reactors in which only one wafer at a time is processed. This is desirable mainly to exercise great deposition control over expensive, large size (≥6") wafers. The theory of reactor design has been discussed in great detail.[39]

The advantages of CVD processing will now be considered further.

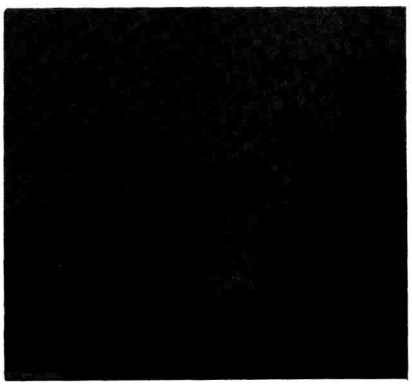
Conformal Coverage. Narrow, straight-walled windows and vias, re-entrant angles and overhangs are device features that can lead to poor conformal coverage with sputtered or evaporated films. Figure 4a illustrates the poor conformal coverage typical of physical deposition processing. During such line-of-sight deposition processes, shadowing effects due to device features leads to local film thickness nonuniformities. On the other hand, Fig. 4b illustrates the ideal conformal coverage that is typical of CVD processing. Because the growth of CVD films is usually surface catalyzed, nucleation and growth occurs on all surfaces, regardless of their orientation to the gas source. Therefore, by definition, uniform coverage is achieved. Uniform coverage can lead to "plugging" of windows and vias if the films are allowed to become thick enough, as is shown in Fig. 4c.



3) Schematic diagram of a cold-wall low pressure CVD system.



a



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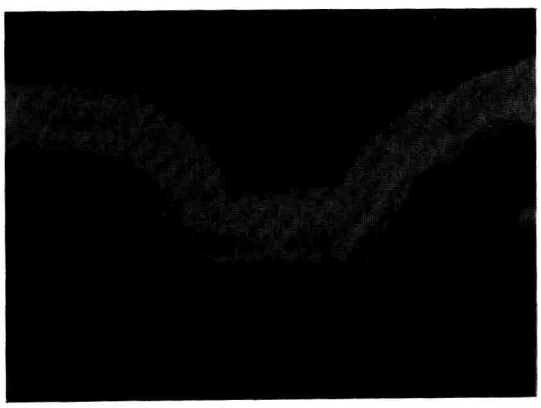


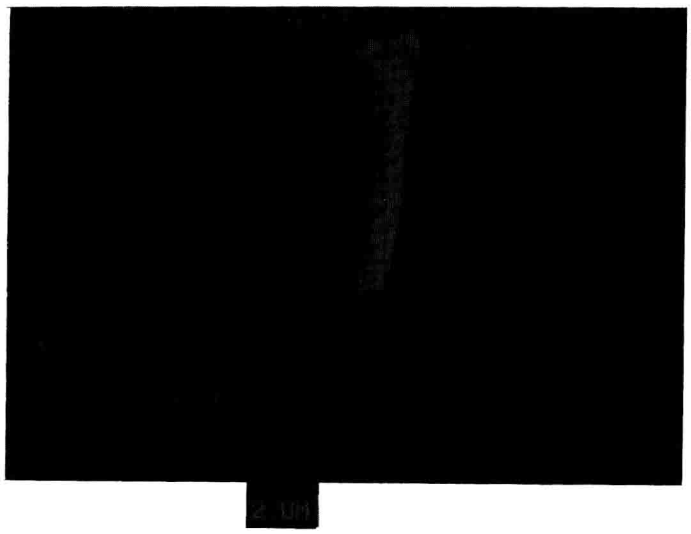
b

4) a) Evaporated Al film deposited on the contact window of a typical device, illustrating poor conformal coverage,
b) CVD Al film deposited on a similar contact window, illustrating nearly perfect conformal coverage, and
c) Thick CVD W film deposited on a small ($\sim 1\mu m$) contact window, illustrating the filling, or "plugging", of the window.

Low-Temperature Deposition. Many high melting point metals can be deposited at relatively low temperatures by CVD. For example, W can be deposited at 300°C, or 0.16 T_{mp}, by the H_2 reduction of WF_6. Such low homologous temperatures are useful in minimizing interdiffusion between the various layers of the device. Deposition of W films by evaporation, for example, would require heating of the W source to temperatures near its melting point by resistance heating or electron beam bombardment. The CVD apparatus is much simpler in that it operates at much lower temperatures.

Within the CVD field there has been a move towards the use of organometallic sources to achieve lower deposition temperatures. For example, Cr can be deposited from $CrCl_2$ at T = 1200-1325°C,[40] but from dicumene chromium, $(C_9H_{12})_2Cr$, at T = 320-545°C,[6] and V can be deposited from VCl_4 at T = 1140-1300°C,[9] but from $(C_5H_5)V(CO)_4$ at T = 325-500°C.[41]

Radiation-Damage Free Deposition. Sputtering can also deposit high temperature films at fairly low temperatures. However, sputtering is an energetic process that results in electron, x-ray and ion bombardment of the gate oxide and substrate. Defects called traps, produced at the gate oxide/silicon interface,[42] can affect device performance by altering threshold voltage characteristics, and must therefore be annealed out.



5) Thick selective plug of CVD W deposited in a window in SiO_2 to Si. Aspect ratio of window is 3:1. (from R. Wilson, GE Laboratories)

Deposition Selectivity. CVD film formation is fundamentally different from sputtering or evaporation in that nucleation and growth are catalyzed by the deposition surface. Therefore, by deactivating certain surfaces, films will tend not to nucleate and grow on them; consequently, one can selectively deposit films. Figure 5 is an example of W selectively deposited on Si, to the exclusion of SiO_2. This is very important because patterning steps (photolithography and etching) are not necessary for these films. Selectivity can occur on the basis of choosing reactants such that reactions with only certain substrate components will occur, as has been done with Ag,[11] Mo[7] or W[10,43] for deposition on Si to the exclusion of SiO_2, or by lowering the temperature and pressure so that film nucleation is easier on Si than on SiO_2, as has been done with W.

Of the various CVD metal processing schemes, CVD W, and to a lesser extent CVD Al, are closest to commercial acceptance. These two processes will now be discussed in detail.

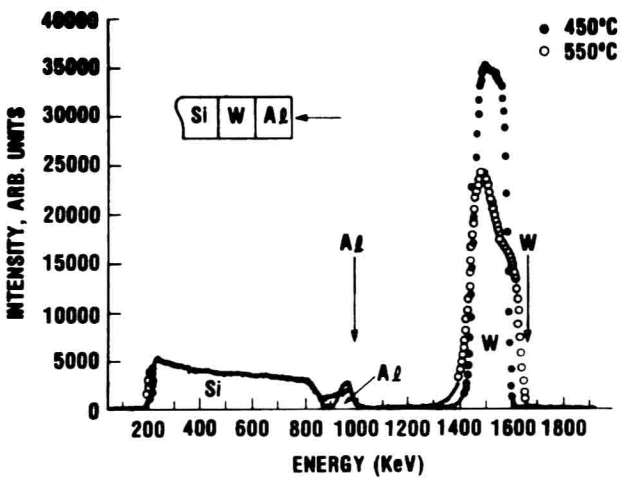
CVD Al. As is illustrated in Fig. 4b, LPCVD Al, deposited by the pyrolysis of i-$(C_4H_9)_3Al$,[19-21] (tri-isobutylaluminum or TIBAL), exhibits excellent conformal coverage. This is the major reason for its intended application as an interconnect metallization for submicron VLSI circuits. Safer (nonpyrophoric) source materials might accelerate the introduction of CVD Al processing into commercial practice. These have yet to be identified.

Selective CVD Al has recently been demonstrated,[44] thereby opening CVD Al technology to many of the same applications for which selective CVD W is now being considered. In addition, whereas Si can react extensively with WF_6 during the selective CVD W process,[45,46] causing damage to devices, TIBAL does not interact with Si, leaving it undamaged.

An important characteristic of the CVD Al film is its rough surface. This roughness manifests itself by rendering the films milky-white in appearance, with low reflectivity,[20] which can give rise to photolithographic processing problems. Thick CVD W films, e.g. in Fig. 4c, also exhibit rough surfaces, and, thus far, patterning has been successful.

CVD W. Due to recent intense interest in the commercialization of CVD W technology, its use in VLSI applications is imminent, although it is not clear now which application will be first. Properties such as resistivity and stress, which are important to every application of CVD W, are well documented and are found to be well within the acceptable range.[47] However, the stress of CVD W films on substrates other than Si (i.e. SiO_2 (with various "glue" layers), metals, etc.) needs to be investigated. Further, the electromigration resistance of W is more than adequate for VLSI device requirements, due to its high melting point.

That CVD W is an effective barrier to Al/Si interaction is illustrated in Fig. 6. The RBS spectra show that whereas after a 450°C/30 min anneal the Si/W/Al layered structure is essentially the same as it was in the as-deposited state, a 550°C/30 min anneal leads to the destruction of the layers due to interdiffusion. Although 450°C is a reasonable temperature limit for post-metallization integrated circuit processing, some processing schemes, notably those which involve multilevel metallization and intermediate dielectric layers, may necessitate process temperatures as high as 550°C. Diffusion barriers, other than W, may succeed in this temperature regime. CVD W films would probably also work in this higher temperature regime, if their grain size were not as small as it is, ~1000-3000Å.[47] Larger grain size films or "stuffed" grain-boundary films would undoubtedly be better barriers.



6) RBS spectra of an Al-W-Si structure (1500Å Al/1100Å W/Si substrate) after 30 min. anneals at 450°C and 550°C. Arrows mark the surface positions of the corresponding elements. The as-deposited spectrum, not shown, was identical to the 450°C spectrum.

In conclusion, the advantages of CVD processing, which include conformal coverage, low temperature and radiation-free deposition, the possibility of deposition selectivity, and high purity film formation are certain to insure the use of CVD metallization in future VLSI processing schemes. At this point, CVD W, and to a lesser extent CVD Al technologies are closest to commercial realization. The major applications of CVD W might be as follows:

a) As a multilevel metal via fill: deposited either selectively or nonselectively, the CVD W would not be in contact with Si, so potential problems such as Si consumption and high leakage current would not arise. However, the CVD W would have to be deposited on first level metal,

probably Al, requiring the use of a silicide, e.g., interlayer, due to the native Al_2O_3. Furthermore, the problem of surface roughness would have to be solved, perhaps by depositing W alloys rather than W.

b) As an interconnect or diffusion barrier or plug, but only if the WF_6/Si interactions can be avoided, perhaps through the use of a protective, conductive layer such as CVD TiN on top of the Si.

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