# Area Array Package Design

## Techniques in High-Density Electronics

Ken Gilleo, Ph.D.

McGraw Hill

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**Ken Gilleo, Ph.D.** Editor

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# PREFACE

Area array packaging provides the highest density with maximum performance of any concept yet devised, making it the most important technology in advanced packaging. Older and more familiar perimeter connection–style packages that first appeared about 40 years ago still serve many applications, but designs exploiting package area for connections are now essential for modern electronics, especially high-performance systems and portable products. This book begins with definitions of packaging, next details the numerous requirements, and later describes how packaging has evolved to satisfy these needs. Diagrams show details of various package constructions to highlight the all-important role as the "bridge" between semiconductor devices and circuit boards. Perimeter-style designs are compared to area array concepts with convincing arguments for the continued advance and deployment of this newer technology.

The book provides a comprehensive overview of chip- and board-level interconnection methods. Chip-level, or first-level, connections, such as wire bonding, TAB (tape automated bonding), and flip chip, are covered in detail. Increasingly popular flexible circuit–based packages, now extensively used, are described, showing how they utilize all three types of first-level connections. Substrate and routing considerations are discussed, followed by chip protection schemes. Finally, the package-to-board, or second-level, connection options are compared. Eutectic solder balls are the most common and are covered thoroughly, but high-melting columns, nonfusing metals, and polymer conductive adhesive options are included and contrasted.

Packaging materials are summarized to provide the necessary background to better understand concepts and designs. Package platforms, chip carriers, and substrates bring the focus to ceramics, metal, organic materials (including flexible circuits), and combinations. Materials topics include substrates, joining media, conductors, adhesives, encapsulants, fluxes, and underfills. Different solder alloys, including lead-free materials, are described, and the impact of resulting higher assembly temperatures is assessed.

The business overview chapter discusses needs, economics, and motivation for rapid and sustained growth for area array packaging. Both market drivers and technical benefit perspectives are included. A strong case is made for area array as the final packaging revolution since this architecture has retained key attributes from previous revolutions, like surface mount, but added new ones. The business and economic topics also show the importance of manufacturing technology, throughput, and yield on the electronics industry and the key role of packaging.

The book includes minimal area array designs like flip chip that achieve the smallest possible footprint, and stacked chip configurations that deliver the highest conceivable density. Undoubtedly, the most advanced designs will continue to employ area array concepts since a perimeter configuration is no longer an option for sophisticated active devices. Area array is essential for satisfying the mandate of "smaller-faster-cheaper," and new products continue to evolve. Modern cellular phones and virtually all personal computers now rely on area array packaging, and the role in these and other applications is described.

Since area array can provide the highest possible density, several chapters deal with designs and concepts that deliver the maximum, such as flip chip and chip scale packages (CSPs). Chapters cover details of flip chip, or direct chip attach (DCA), and discuss the subelements that include under-bump

metallization, bumping processes, fluxes, underfills, and compatibility. Special attention is given to the underfill step, its present limitations, and future improvements.

CSPs are described from several aspects to provide guidelines for designers, assemblers, and users. Information in the CSP and flip chip chapters allows the reader to decide where each concept can best be applied and how to avoid the pitfalls of both. Advanced CSP and flip chip topics, including the latest multichip package (MCP) designs like 3D (stacked), are described in several chapters. Multichip structures encompass wire bonding, tape carrier packages (TCPs), and flip chip configurations for the first-level assembly within the package, as well as combinations. Applications are discussed showing how stacked area array packages, the densest package designs possible, are rapidly moving into computers and telecommunications products.

Reliability is covered from several viewpoints that include materials, design styles, and assembly. Comparisons are made between ceramic, plastic, and metal systems and protection strategies. Subjects include solder ball void defects and influence factors, flip chip bump types, underfills, and thermomechanical effects. The discussion of ceramic area array packages also compares reliability of ball grid arrays and column grid arrays (CGAs) and the benefit of greater standoff height. Reliability as a function of rework, higher-temperature solders, moisture adsorbed by packages, and assembly process effects is included.

This book also looks into the future to access the needs of the latest emerging semiconductor technologies and includes MEMS (microelectromechanical systems) and MOEMS, or optical MEMS. A new industry is unfolding based on chips that combine mechanics with electronics. The MEMS chapter points to the need for new packaging designs specifically for MEMS to satisfy mechanical device special requirements in this rapidly expanding and diversifying field. MEMS, and related optical chips, have special requirements, such as free space above the device to allow movement of the mechanical elements. Concepts for replacing costly metal and ceramic perimeter packages with MEMS-specific designs are suggested.

The reader should conclude that every important packaging topic has been included and that a convincing case has been made for the continued success and growth of the area array revolution far into the foreseeable future.

*Ken Gilleo, Ph.D.*

## ABOUT THE EDITOR

KEN GILLEO, PH.D., is a well-known author/editor/columnist in the fields of circuitry, MEMS, and microelectronics packaging, and CEO of ET-Trends LLC, a consultancy and intellectual property company focused on emerging technology. His *Area Array Packaging Handbook: Manufacturing and Assembly*, also published by McGraw-Hill, is the premier professional guide in the field. Dr. Gilleo also has edited the *Handbook of Flexible Circuits* and *Polymer Thick Film*, and has written over 400 articles on packaging, circuitry, MEMS, and materials. He holds 35 U.S. patents, currently serves on the Board of Directors of the Surface Mount Technology Association, and is active in IEEE, IMAPS, and other professional organizations. He lives in Warwick, Rhode Island.

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# CHAPTER 1
# INTRODUCTION TO ELECTRONIC PACKAGING

**Ken Gilleo**
*Cookson Electronics*

## 1.0 DEFINITION OF THE PACKAGE

The ideal electronic package is an economical and manufacturable electromechanical platform for one or more electronic devices that affords protection, facilitates handling, and provides the geometric translations and compatible interface required for connection to the next system level by practical assembly processes.

## 1.1 INTRODUCTION AND REQUIREMENTS

This book covers much of the field of packaging, including the new minimal category, but with a focus on area array designs. This chapter will describe the functions of the electronic package, protective requirements, and issues as well as solutions for general packaging. This chapter emphasizes area array packages because this is the central theme of this handbook.

The electronic package is designed to perform an assortment of tasks. Some functions can be at variance with one another, requiring balance and compromise for optimization. The package must first house and protect the delicate integrated electronics devices from the external environment. This generally is accomplished by enclosing the chip in a protective cocoon of electrically insulative materials. Alternatively, the package can be a metal vacuum-sealed container with appropriate internal insulation or a similar structure made of gas-impervious ceramic. The package also may need to dissipate substantial heat generated by the electronics. Heat management generally is not an issue for the hermetic metal package or the ceramic type. However, the common plastic package has good thermal insulation characteristics that prevent efficient heat transfer to the outside. Plastics have low thermal conductivity, so enhancing thermal performance of plastic packages takes ingenuity in both design and materials. The general electronics industry also seeks to reduce size and weight while the devices to be packaged become faster and have more connections. There is also strong pressure to accomplish this while lowering the cost. Thus the paradoxical phrase, "faster, smaller, cheaper." The packaging industry therefore is tasked with achieving goals that appear mutually exclusive but is asked to do so more quickly. Surprisingly, the industry has succeeded to a large extent, but solutions have required major innovations that are defined accurately as the "packaging revolutions" (Fig. 1.1).

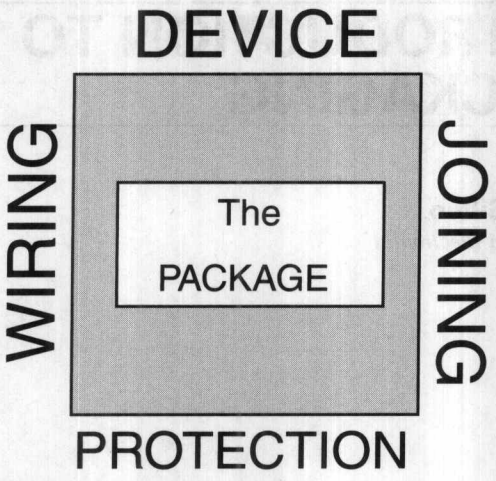


**FIGURE 1.1** Packaging diagram.

## 1.2 PACKAGING EVOLUTIONS AND REVOLUTIONS

### 1.2.1 SMT

Most people are familiar with the standard molded-plastic packages seen in computers and their plug-in cards. Many of these packages are feed-through types where the metal leads fit through holes in the circuit board. The most common design in the feed-through class typically is called a *dual-in-line package* (DIP) because of the two rows of leads on each side of the plastic encasement. In the early 1980s, a more efficient packaging design strategy, called *surface-mount technology* (SMT), was introduced to solve a host of problems. The SMT process makes the connections simply by soldering the package leads to the surface of the board. The surface-mount device (SMD) can be much smaller, accommodate many more connections, is easier to assemble with automated equipment, and does not require holes through the circuit board. Absence of feed-through holes allows components to be assembled on both sides of the board. The DIP-type packages not only use up more surface area but also consume circuit density because holes must be fabricated through all layers of the board that otherwise could accommodate inner circuitry. The clear benefits of SMT have allowed this style package to capture more than half of designs. SMT has advanced over the years to reduce size and accommodate more leads. It should be noted that feed-through packages are still used, and this will continue. In fact, SMT and feed-through packaging can be complementary, and there are assembly processes for connecting both types in one operation. Figure 1.2 compares the feed-through style with SMT.

### 1.2.2 Perimeter Paralysis

In the early 1990s, it once again was time for a major change in packaging style. The relentless advancements in the semiconductor industry were putting an ever-increasing demand on even the densest SMD-style packages. The number of connections, or inputs/outputs (I/OS), moved continuously, while more compact electronic products demanded smaller packages. Since the packaging leads, or terminations, were on the perimeter, this meant that more leads were being placed in a smaller space. In other words, there was an ever-increasing "perimeter paralysis." Some of the packaging fabricators, most notably in Japan, responded by making smaller leads and placing them closer together for finer pitch. This approach soon ran out of steam as leads became flimsy, solder bridging defects increased, and assembly lines struggled with alignment problems. Ultrafine-pitch perimeter packages were the wrong solution.

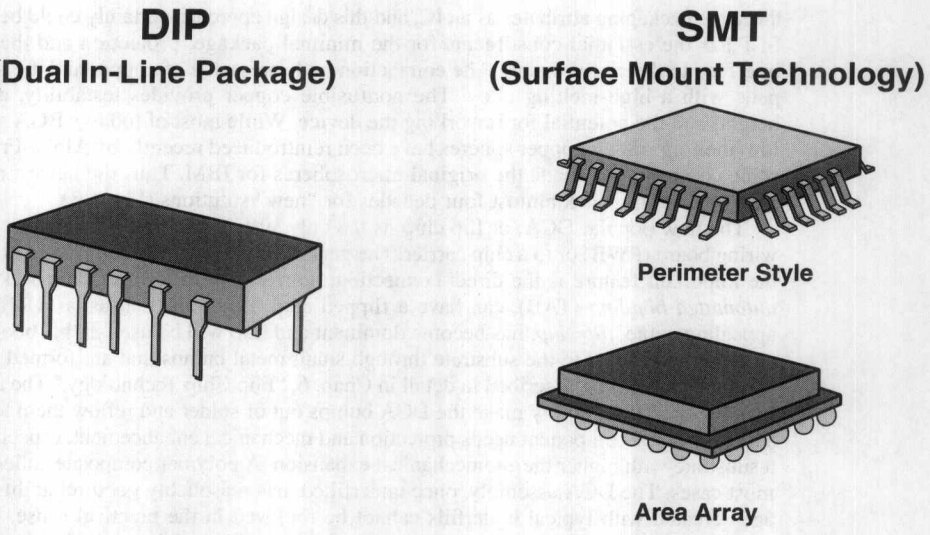


**FIGURE 1.2** DIP versus SMT.

Vertically integrated electronics companies in the United States, led by IBM and Motorola, recognized that the time was right for the next packaging revolution. The simple answer for packing more connections into a shrinking housing was to use the wasted area inside the perimeter. Area array packages simply exploit the area under the package for connection sites. This was not an overlooked solution waiting to be conceived. IBM had used area array packaging since the 1960s. The issues were that a move to area array for ordinary packaging would be a hard sell and a daunting implementation task. IBM had developed ceramic area packages, with some using columns of high-melting solder, called *column grid array* (CGA). Motorola introduced a lower-cost *ball grid array* (BGA) in which solder spheres were used to make the connection to the board. Motorola's announcement of the Ompack BGA caused a major stir within the packaging and assembly industries. Many of us view Ompack as the official launch for the area array packaging revolution that is still vigorously underway. The plastic Ompack, or *o*ver*m*olded *pac*kage, generally is referred to as a *PBGA,* with the *P* standing for plastic. The PBGA is the most common type of area array electronic package. This book will deal with design, manufacturing, testing, and assembly of PBGAs and other area array packages as well as the materials.

There are many subdivisions of the BGA, but all are surface mountable, and most are area array. The next discussion will include the minimal micropackage beginning with the flip chip. While packaging is necessary, many view it as a "necessary evil" that should be minimized. Admittedly, the package tends to add cost and increase the size. Many have sought to reduce it to a minimum; hence the minimal package. I will avoid the clumsy terms *minimalist package* and *minimalistic package* to stay with the more appropriate and more minimal term *minimal package.*

### 1.2.3 Direct Connections

I will start with the simplest and most minimal package, the flip chip that was pioneered by IBM and referred to as C4 or $C^4$, for *controlled collapse chip connection.* Actually, it is necessary to take just one more step back to find the beginning of area array, SMT, and BGA—all in one package. In the early 1960s, while the industry was still working on transistor packaging, IBM came up with *solid logic technology* (SLT). This package, shown in Fig. 1.3, appears to be the very first minimal package: the first BGA, the first SMD, and the original flip chip. A more generic and inclusive term for this type of package is *direct chip attach* (DCA). Some people may argue that the SLT is not a chip, or integrated circuit (IC), but rather a lowly transistor. However, a transistor requires most of

the same packaging attributes as an IC, and this design approach certainly could be used on an IC. The SLT has the essential constituents for the minimal package: protection and the electromechanical interface to the circuit board. The connection balls are made of copper and are soldered to the chip pads with a high-melting alloy. The nonfusible copper provides testability, an assured standoff height, and the potential for reworking the device. While most of today's BGA spheres are made of low-melting solder, copper spheres have been reintroduced recently by Alpha-Fry Technologies, the same company that made the original microspheres for IBM. Thus the newest area array packages may be reaching back almost four decades for "new" solutions (Fig. 1.3).

The now popular DCA, or flip chip, is the only system that directly attaches an IC to the printed wiring board (PWB) or to a chip carrier. The generic and descriptive term is *direct chip attach* because the important feature is the direct connection, not flipping the chip. Other packaging, such as *tape automated bonding* (TAB), can have a flipped chip; hence the confusion. Unfortunately, the more appealing name, *flip chip,* has become dominant and also will be used in this book. The DCA is most commonly attached to the substrate through small metal bumps that are formed on the chip pads by methods that will be described in detail in Chap. 6, "Flip Chip Technology." The most popular attachment method is to simply make the DCA bumps out of solder and reflow them to the substrate pads. The assembled component needs protection and mechanical enhancement, especially when bonded to a substrate with higher thermomechanical expansion. A polymer composite called *underfill* is used in most cases. The DCA assembly, once underfilled, has reasonably good reliability. The in situ "package" created with typical underfills cannot be removed in the practical sense. This means that the underfilled chip probably cannot be reworked, although special reworkable underfills recently have come to market. Some people would argue that a package must be removable and should be reworkable in the true and practical sense of the term. So is the DCA flip chip a package? Let's define the terms of packaging requirements and try to separate absolute essentials from desirables.

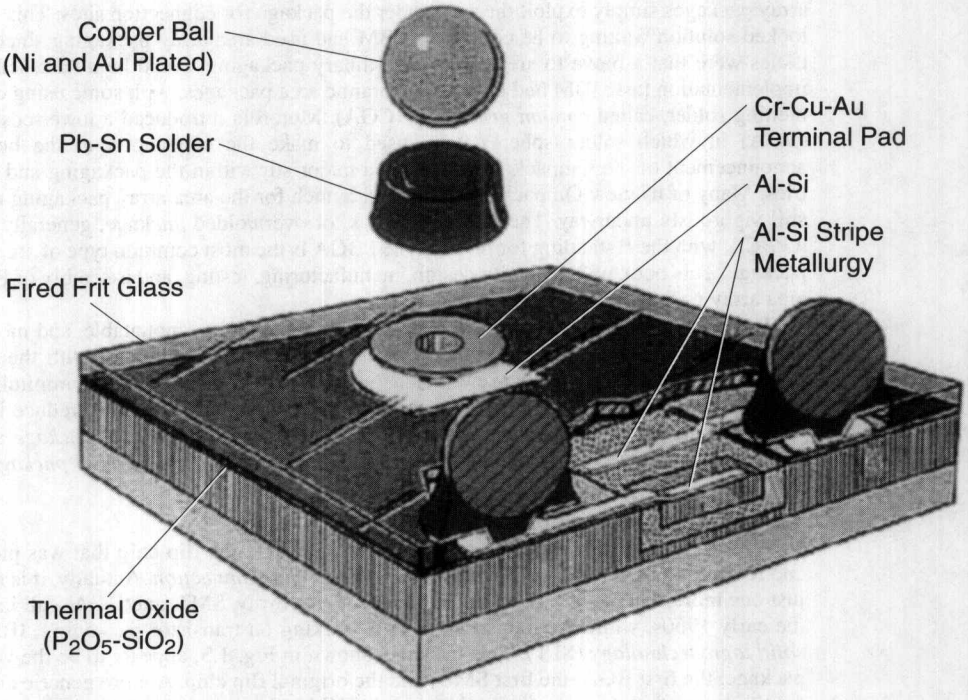


**FIGURE 1.3** IBM SLT package. (*Courtesy of IBM, P. Totta.*)

## 1.3 USEFUL VERSUS ESSENTIAL FEATURES

The essential features of the package listed in Table 1.1 are required to make the semiconductor chip compatible with the printed circuit board (PCB and to give it reliability. The IC and PCB, or printed wiring board (PWB), used to avoid the other acronym associated with a pollutant) come from different worlds with different materials. The package bridges the inherent incompatibility between the microworld of inorganic ICs and the more macroscopic environment of organic PWBs. Not only does the most common package design expand and fan out the IC's microgeometry to fit the circuit board, it also allows the very thin aluminum (and now copper) chip pad to be connected to the relatively thick copper circuit pads. The list of useful features has become the main focus of modern packaging and will be discussed briefly here.

Table 1.1 is a list of all the both essential and useful attributes of the electronic package. In some applications, a useful attribute can be essential. Thermal management may not even be useful for a low-power memory chip but a critical requirement for a powerful central processing unit (CPU).

### 1.3.1 Geometric Translation

The IC device is made using processing that can produce features sized down to nearly 0.10 μm or $1 \times 10^{-7}$ m, or about 1/10,000 in. Microelectronics is soon to become nanoelectronics as the feature size falls below 0.1 μm (100 nm). While the prefix *micro-* means one-millionth (of a meter), the prefix *nano-* means one-billionth ($1 \times 10^{-9}$ m). The printed circuit industry generally considers fine line to be about 3 to 4 mils (75 to 100 μm). There is nearly a 1000-fold feature size disparity between the two industries and their products. We can expect this ratio to remain somewhat constant or even to increase. The translator, the technology that spans the breach, is the package. The package has had to add a greater level of translation capability each time that the semiconductor industry has surged ahead with a smaller IC that required more connections or I/Os. The increasingly common strategy is to take the chip's perimeter pad connections and reroute them into an efficient area array. Although very high density interconnect (HDI) packages can accommodate chip pad dimensions, the HDI substrate is more expensive and only available from a limited number of suppliers. The economics can be better with a fan-out package, especially when many low-density components are used with one or a few high-density ones. Adding to the cost of packaging can save on the printed circuit costs to provide a net gain, especially if yield improves.

### 1.3.2 Material Compatibility: IC to PWB

There are two important material differences between the IC and PWB that make them incompatible. First, the IC substrate is inorganic silicon, with silicon compounds used as insulators. The most common PWB is made from epoxy resin with glass reinforcement. Silicon has a coefficient

**TABLE 1.1** Essential and Useful Attributes of Electronic Packaging

| Attribute | Absolutely essential | Very useful (not required) |
|---|---|---|
| Geometric translation | Usually | |
| Compatibility: IC to PWB | X | |
| Environmental protection | X | |
| Mechanical protection | Yes, most cases | |
| Handling ease | | X |
| Enable standardization | | X |
| Facilitate auto assembly | | X |
| Removability | X | |
| Reworkability | ? | X |
| Performance enhancement | | X |
| Thermal management | | In many cases |