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MICROPROCESSOR INTERFACING

A DESIGNER'S GUIDE TO MEMORY DEVICES, INPUT/OUTPUT PORTS, AND INTERFACING WITH THE ANALOG WORLD!

BY JOSEPH J. CARR

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Introduction

The microcomputer age is not a decade old, but seldom has any one component or concept so rapidly revolutionized the electronics industry! Engineering schools can now advise students that an electrical engineer who is not conversant with microprocessor design methods will not remain employable for long! At first we were told that this situation would be true "in five years," but history has shown that two years was nearer the truth. Everything from children's toys to complicated scientific instruments on-board space ships has been computerized.

The proper application of the microprocessor/microcomputer requires a person who is a synergism of the software and hardware people found on larger systems. With "dinosaur" computers there are completely separate engineering and programming functions—carried out by different people; but on the microcomputer level when you treat the microprocessor or microcomputer as a component in an instrument design, you as the designer must be good at both.

This book will bring you quickly up to date on the elements of hardware interface with microprocessors. Covered in this volume are methods for interfacing memory devices, creating I/O (input-output) ports, and interfacing with such devices as keyboards, printers, sensors, and the analog world.

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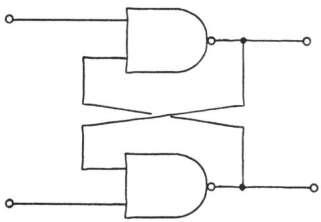
Chapter 1



Introduction to Digital Electronics

Digital electronics is a general field that encompasses digital computers, including microcomputers. Before you try to solve microprocessor interfacing problems you must learn the basics of digital electronics. Whether or not you are professionally involved in electronics, you should learn this material because no one any longer can safely ignore the world of digital electronics. Even radio and television technicians find digital circuits in the products they repair. Computerized color-television tuning and stereo-FM tuning are almost the rule, rather than the high-priced exception.

Digital electronics is, however, often simpler than analog electronics because digital IC (integrated circuit) devices recognize only two states, i.e., on and off. This makes digital circuits similar to relays and switches. In fact some digital circuits are little more than high-frequency-electronics versions of simple switches. It is my opinion that anyone who can understand simple relay and switch-logic circuits can also understand digital electronics. Certainly anyone who can understand color television, SSB (single sideband), FM two-way radios, and certain other complex products can understand digital electronics.

LOGIC STATES

Digital circuits respond to only two different input states. These states are called 1 and 0 (after the two permissible digits of the *binary*, or base-2, number system), high and low, or (in older texts) true and false. These designations are merely representations of two different voltage states. In this book the high/low designation is used because it graphically describes what is happening to the circuit.

Transistor-transistor-logic (TTL) responds only to 0 and +5 V for the two logic levels. If any other voltage levels are used the TTL device either (1) fails to work, (2) works unpredictably, or (3) burns out. Figure 1-1A shows the TTL levels.

Complimentary metal-oxide semiconductor (CMOS) IC logic devices can use the same 0 and +5 V logic levels as the TTL devices but may also be

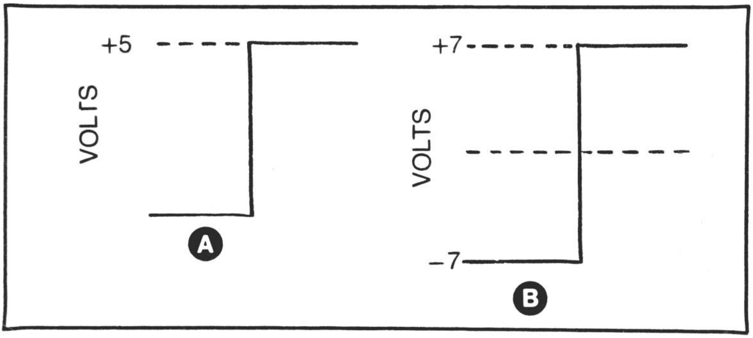


Fig. 1-1. (A) TTL logic levels and (B) CMOS logic levels.

used at any combination of voltage levels between ±4 V and ±15 V. In CMOS, illustrated in Fig. 1-1B, ±7 V is used. The voltage levels that represent high and low conditions in CMOS need not be equal. In fact many circuits use a positive voltage (i.e., +12 V), and 0 V for high and low conditions, respectively. Some CMOS digital devices, notably complex function devices, fail to operate properly and predictably if the applied voltage is less than 7 V. These devices sometimes refuse to operate properly on TTL levels of 0 and +5 V despite claims to the contrary.

POSITIVE AND NEGATIVE LOGIC

You may sometimes hear the terms positive and negative logic. These terms tend to confuse the newcomer and mean nothing more than how the high and low logic states are related to voltage levels. In *positive logic* the high is logical-1 and is a positive voltage (i.e., +5 V in the case of TTL). The low, logical-0, is 0 V in TTL. Logical-0 may be a negative voltage in some CMOS circuits.

In *negative logic* these designations are reversed (i.e., high = logical-0 and low =logical-1). In the vast majority of uses positive logic is specified. In fact the descriptive names given to digital IC devices reflect a bias toward positive logic. This potential confusion is why I prefer high/low designations. For the illustrations and truth tables 1/0 is used, but recall that positive logic is implied.

LOGIC FAMILIES

A logic family is a series of IC devices that may be interconnected without interfacing; they use similar technology in their construction. All of the devices within a given family have the same input and output circuits; so direct interconnection is possible.

The only major consideration is whether an output can supply sufficient current to drive all of the inputs that are connected to it. In any given logic family output voltage and current levels, also input voltage and current requirements, are fixed by agreement and defined in terms of *fan-in* and *fan-out*.

The unit used to describe these terms in most cases is the current requirement of a single standard-input at the fixed voltage level. Such an input has a fan-in of one unit. If a particular IC has a fan-out of five, this means that the device can drive five standard inputs. The device, therefore, can supply sufficient current to drive all five inputs satisfactorily. The total fan-in of all devices connected to any output must be equal to or less than the rated fan-out of the output.

The logic families considered are: RTL, DTL, TTL, HTL, ECL, and CMOS. Of these families CMOS and TTL are the most popular today RTL and DTL are obsolete and no longer used in new designs (although much of the older equipment, still in use, contains RTL and DTL devices).

SPEED VERSUS POWER

The principal factors governing the speed, or maximum operating frequency, of a digital IC are the internal resistances and capacitances. If resistances are increased, so that power consumption drops, then the resistance-capacitance time-constant of the device is increased. Long resistance-capacitance time-constants mean slower operating speeds. As a general rule, therefore, higher speed logic-families have high power requirements. CMOS devices, which require very little current (hence are low power), operate well only at 4 or 5 megahertz (MHz) with some devices operating as high as 10 MHz. TTL devices, on the other hand, usually work at 18 or 20 MHz, with some selected devices operating well over 80 MHz.

RTL DEVICES

Resistor-transistor-logic (RTL) is an obsolete logic family that was popular in the early to mid-1960s. Figure 1-2 shows a typical RTL inverter circuit, i.e., a circuit that produces a low output when the input is high and a high output when the input is low.

RTL IC devices use 0 V for logical-0 (low) and +3.6 V for logical-1 (high). If the input of the RTL inverter is grounded (i.e., placed low), then the output voltage is high, which in this case means +3.6 V. If the input voltage is high, the output is 0 V.

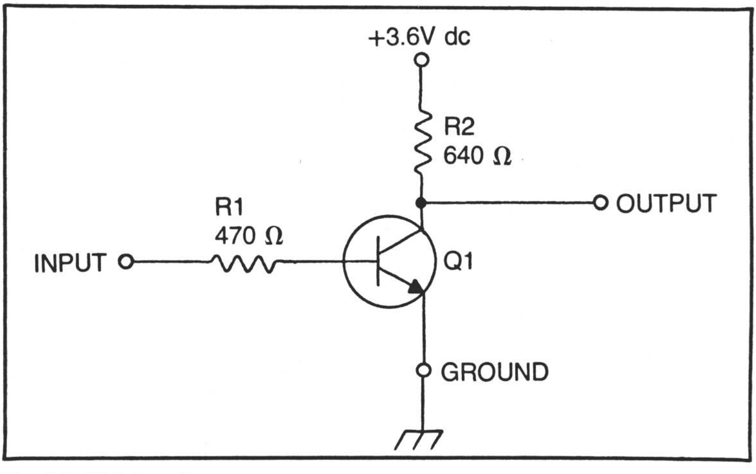


Fig. 1-2. RTL inverter.

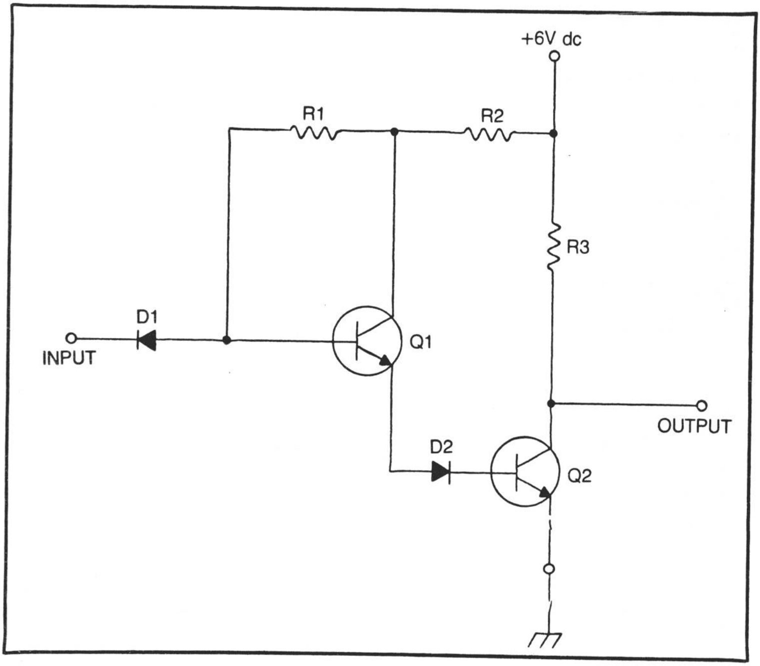


Fig. 1-3. DTL inverter.

RTL devices usually carry type numbers in the UL900 series (mostly 8 and 10 pin metal cans) and MC700 series (mostly 14 pin DIPS).

DTL DEVICES

The next popular IC logic family is diode-transistor-logic (DTL). These devices operate at speeds greater than most RTL devices. Figure 1-3 shows a typical DTL inverter.

When the DTL input is high, diode 1 is reverse-biased. In that condition resistor 1 forward-biases transistor 1, which in turn forward-biases diode 2 and transistor 2. Voltage levels in most digital circuits are selected to *saturate* the transistors; when transistor 2 (Q2) is turned on, it is turned on to full saturation. This means that the output of the inverter, which is the collector of Q2, goes within a few millivolts of ground.

When the input is low, the cathode of diode 1 (D1) is grounded. Since D1 is now forward-biased, the base of Q1 is essentially grounded. Under this condition Q1, D1 and Q2 are reverse-biased. With Q2 cut off, then, the output voltage rises to V_{CC} +.

Most DTL devices carry part numbers in the MC800 and MC900 ranges (Motorola designation).

TTL DEVICES

Probably the most widely used digital IC is the transistor-transistor-logic (TTL) logic family. When most people speak of digital ICs, it is the

TTL family of devices to which they refer. Most TTL devices carry type numbers in the 5400 or 7400 series. Those devices that are in the 5400-series are military equivalents to the 7400-series device (i.e., a 5447 is a 7447 in uniform). The principal difference between the 5400 and 7400 devices is the operating temperature range (−55-+125 degrees C for mil-specified devices).

Figure 1-4 shows the circuit for a typical TTL inverter IC. Like the DTL device, the TTL input acts as a current source, while the output acts as a current sink. The typical TTL input sources 1.8 mA (milliamps) and is low if the voltage is 0-0.8 V, and high if 2.4-5.0 V are applied. Performance at values of input potentials between 0.8 and 2.4 V is not defined; so operation of the devices is unpredictable.

When the TTL input is high, Q1 is cut off; so point A goes high. This condition turns on Q2 forcing point B high and C low. You find, that Q3 is turned on and Q4 is off. This forces the output low. Again, the transistors are operated either totally cutoff or totally saturated (on).

If the input is low, then exactly the opposite situation occurs: Q1 is turned on (forcing point A low), Q3 is off, and Q4 is turned on; i.e., it is connected to V_{CC} +.

TTL devices must have a regulated dc power supply of +4.75-+5.2 V. In fact there are some circuits or combinations of devices that require a more limited range of voltages nearer to +5 V dc. Voltages greater than +5.2 V often result in a high failure-rate of TTL devices.

Some TTL devices are described as being *open-collector*. They are essentially the same as regular TTL devices, except that the output circuit is modified, i.e., Q4 and D2 are missing. An example of an open-collector circuit is shown in Fig. 1-5. These devices require an external 1000-2000 ohm resistor between the output terminal and the 5 V dc power supply line.

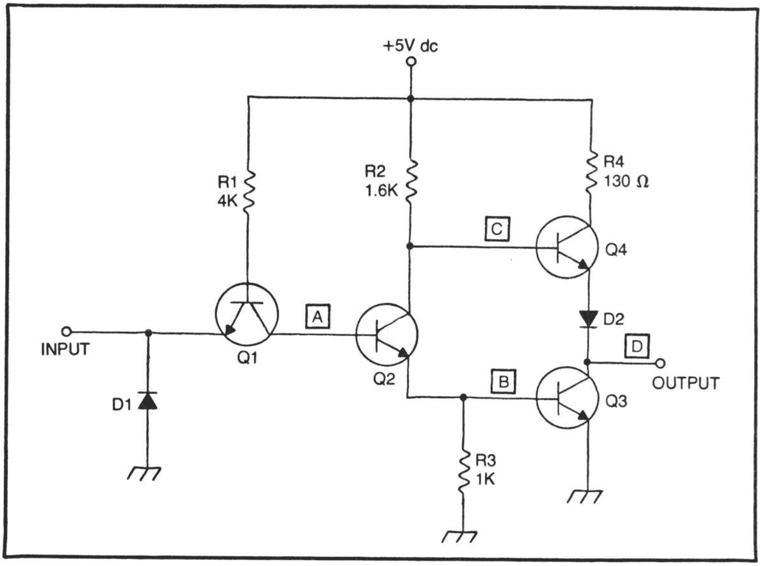


Fig. 1-4. TTL inverter.

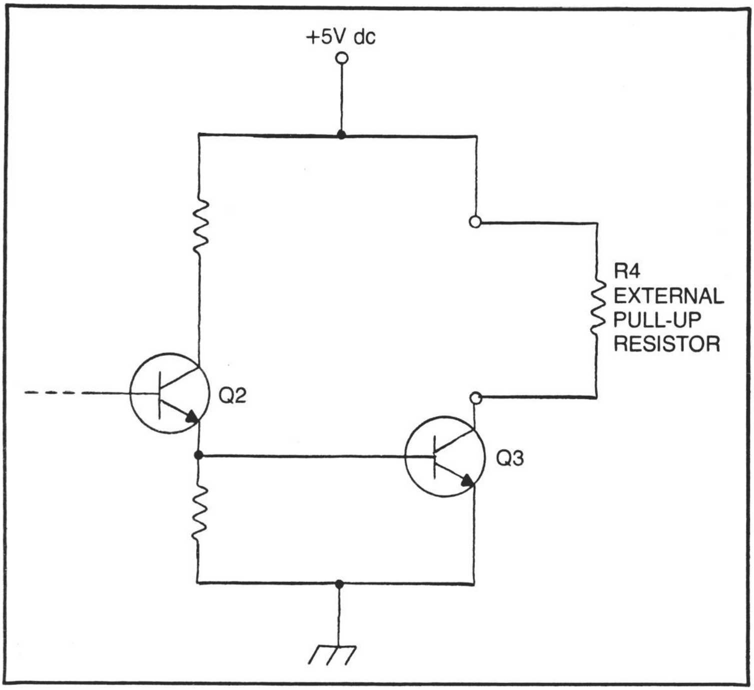


Fig. 1-5. TTL open-collector circuit.

CMOS DEVICES

Complementary metal-oxide semiconductor (CMOS) IC's use field-effect transistors (MOSFET), instead of the PNP or NPN bipolar transistors that are used in other IC logic families. CMOS inputs, therefore, offer very high impedance. Figure 1-6 shows a typical CMOS inverter circuit. Note that this family is called complementary because the output circuit consists of a complementary pair of MOSFET transistors i.e., an n-channel and a p-channel in series.

CMOS devices can use a monopolar power supply, like TTL or DTL, or they can use a bipolar power supply similar to operational amplifiers. When bipolar supplies are used, the positive voltage can be any potential between +4 V and +15 V, while the negative voltage can be −4 V to −15 V. In monopolar cases the V+ can also be +4 to +15 V, while the V− is actually 0 V.

CMOS outputs are not directly TTL compatible, although some specific ICs in the CMOS line are designed to have a TTL output stage (i.e., the 4049 and 4050 devices). These TTL-compatible devices are often used to directly interface CMOS and TTL devices.

Figures 1-7 and 1-8 show the equivalent circuits for a CMOS inverter in both possible input conditions (i.e., input high and input low). A p-channel MOSFET turns on when the gate is low, while the n-channel device turns on when the gate is high.

Figure 1-7 shows the situation when the input is low. In this case Q1 has a very low (i.e., 200 ohm) channel resistance. The output is equivalent to a 200-ohm resistor to the positive-voltage power-supply line.

In Fig. 1-8 you see the situation when the input is high. Q2 now has a very high channel resistance, and Q1 has a very low channel resistance (again, about 200 ohm). In this case the output looks like a 200-ohm resistance to ground; so the output is low.

The high/low or low/high output transition in a CMOS device occurs at a point when the input voltage is midway between the positive and negative voltages. If the negative and positive voltages are not equal, the transition occurs at a potential of $\frac{1}{2}((V+)-(V-))$. If, on the other hand, negative and positive voltages are equal, the transition occurs at 0 V. If the negative-voltage potential is 0 V, the transition occurs at $(V+)/2$.

The CMOS output stage always looks like a high and low resistor in series across the power supply (reexamine Figs. 1-7 and 1-8);so negligible current is drawn from the power supply (it sees a low resistance load) when the input voltage is at the transition point. The overall current drain, therefore, is very small.

But CMOS devices do have a problem: they contain MOSFETs; so they are sensitive to static electricity. All A-series CMOS devices (e.g., 4001A) have this problem, but it is less severe in B-series (e.g., 4001B) devices. The B-series has built-in diode gate-protection to bypass high static potentials around the sensitive gate structure. Nonetheless, they should be handled with care.

HTL DEVICES

Noise pulses are often seen by logic circuits as valid input pulses. This problem is especially bothersome in high speed TTL devices that are normally able to pass high frequency, short duration, pulses. The solution in noisy environments is to use a digital-IC logic family that requires a high

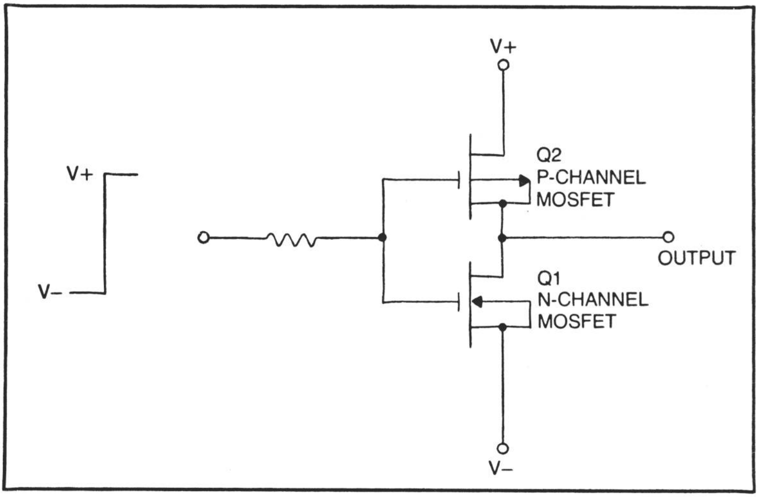


Fig. 1-6. CMOS inverter.

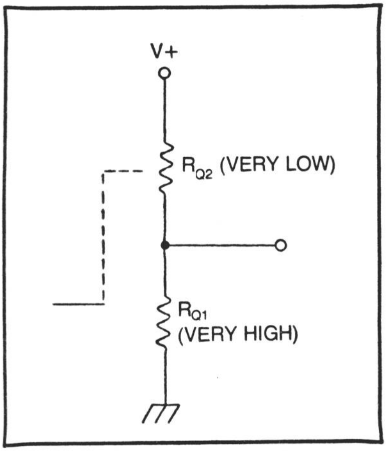


Fig. 1-7. Circuit model for low input.

input-voltage to trigger. CMOS, operated at high negative and positive-voltage values, meets this requirement, but an older, bipolar, ***high threshold logic*** (HTL) can also be used (Fig. 1-9).

HTL (also called high noise immunity logic, or HNIL), uses positive voltages of 12 or 15 V, depending upon the series. As a result, the logic levels are also high; so it requires a bigger noise pulse to cause trouble.

EMITTER-COUPLED LOGIC

Up until now I have talked about saturated logic families, i.e., the transistors in the ICs are either all the way on or all the way off (cutoff or saturated). *Emitter-coupled logic* (ECL) is called an *AC* logic family because the transistors are operated in a nonsaturated mode. As a consequence, ECL devices are capable of very fast operation. Most commonplace ECL devices can operate at 80 or 120 MHz, while some costly, special purpose, devices can operate at over 1 GHz (thats 1000 MHz!).

The usual *prescaler* for a digital frequency counter is nothing more than an ECL frequency divider that divides the 500 MHz input signal down to 50 MHz.

It is necessary to use VHF/UHF circuit design and layout techniques when working with ECL devices. The frequencies are, after all, in the VHF and UHF ranges.

GATES

A digital electronic *gate* is a circuit that either passes a signal or refuses to pass a signal, according to well-defined rules. The basic types of digital electronic gates are NOT, OR, AND, NOR, NAND, and Exclusive-OR (also called XOR). In the following paragraphs I discuss all of these basic gates.

NOT Gates (Inverters)

NOT gates, also called inverters, produce an output that is the opposite of the input signal. Recall that digital circuits respond only to high and low voltage levels. In an inverter circuit, therefore, the output is high when the input is low, and low when the input is high.

The circuit symbol for the inverter is shown in Fig. 1-10A Note that any digital symbol with a circle on the output produces an inverted output. Similarly, if one or more inputs have a circle, then they are inverted. The rules for the operation of the inverter are:

- A high on the input produces a low output.
- A low on the input produces a high output.

OR Gates

An OR gate passes a signal to the output if either input is high. The symbol for an OR gate is shown in Fig. 1-10B, while the truth table is given in Table 1-1B. The truth table shows the rules of operation for the gate. These are:

- If both inputs A and B are low, the output is low.
- If either input A or B are high, the output is high.
- If both inputs A and B are high, the output is high.

AND Gates

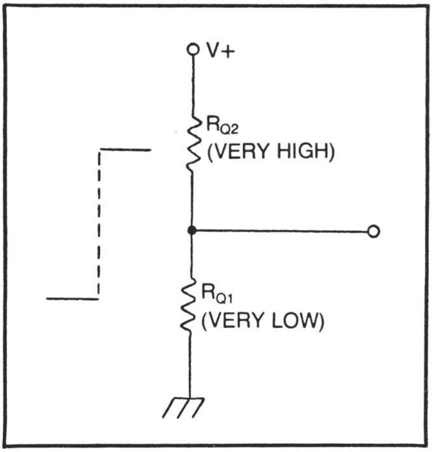
The AND gate is the opposite of the OR gate. The AND gate produces a high output only when both inputs are also high. The circuit symbol for the AND gate is given in Fig. 1-10C, and the truth table is shown in Table 1-1C. The rules for the operation of the AND gate are as follows:

- If both inputs A and B are low, then the output is low.
- If either input A or B is low, then the output is low.
- If both inputs A and B are high, then the output is high.

NOR Gates

The NOR gate is a combination of a NOT gate (inverter) and an OR gate, hence the designation NOR means "not OR." It is, therefore, an OR gate with an inverted output. The NOR gate is, in fact, sometimes represented in text books as an OR gate with an inverter following. The NOR

Fig. 1-8. Circuit for high input.



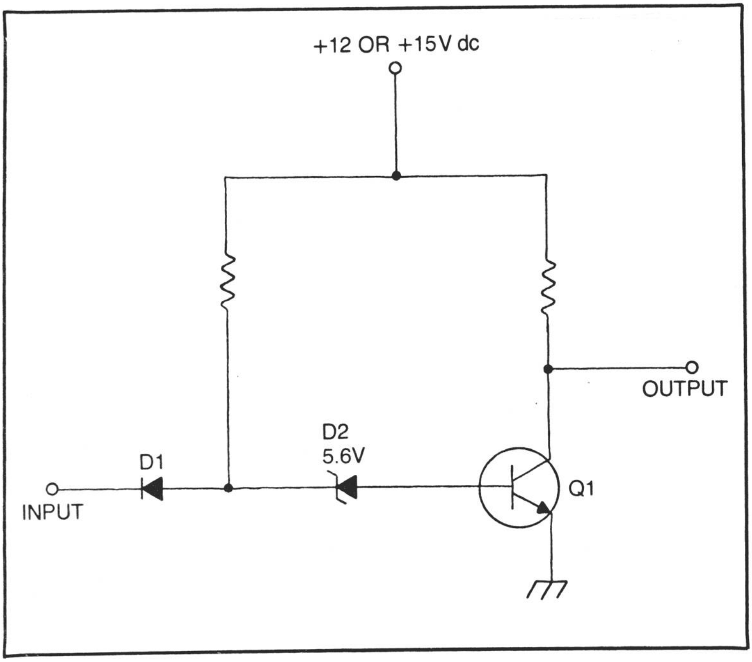


Fig. 1-9. HTL inverter.

gate symbol, shown in Fig. 1-10D, is an OR gate symbol with the circle denoting inversion at the output. The truth table for the NOR gate is shown in Table 1-1D and is also summarized below:

- If both inputs A and B are low, then the output is high.
- If either A or B input is high, then the output is low.
- If both A and B inputs are high, then the output is low.

NAND Gates

The NAND gate is a NOT-AND gate, i.e., an AND gate followed by an inverter. The symbol for the NAND gate is shown in Fig. 1-10E. This symbol is the AND gate symbol with the circle at the output to denote inversion.

The truth table for the NAND gate is shown in Table 1-1E. The rules are presented in summary below:

- If both A and B inputs are low, the output is high.
- If either input A or B is low, the output is high.
- If both A and B are high, the output is low.

TTL AND CMOS EXAMPLES

Earlier in this chapter, I introduced several different families of digital-logic ICs. Several of these are considered obsolete and are not covered further. The TTL and CMOS families, however, are very much alive and form the basis of most digital design today.

TTL/CMOS NAND Gates

In the TTL IC family the most popular NAND gate is the 7400 (see Fig. 1-11). This device contains four two-input NAND gates, and usually sells for less than 25 cents, or around 6 cents per gate. Each of the four NAND gates in the 7400 package is an independent entity, but shares a common power supply and ground connection (pins 14 and 7, respectively).

The 7401 is similar to the 7400, however, the pin-outs are somewhat different, and it is an open-collector device. This means that pull-up resistors are needed, i.e., one 2- 4-K ohm resistor from each output to the +5 V line.

The 7403 is also an open collector, but uses exactly the same pin-outs as the 7400. Of these three devices, the 7400 is by far the most popular.

The 7430 is an eight-input NAND gate (one per 14-pin DIP package). The 7430 device, therefore, has eight distinct inputs. All eight must be high before the output drops low. If any one of the eight inputs remains low, then the output stays high. Since most microcomputers today are eight-bit machines, the 7430 is often used as an address or I/O-port decoder.

The 7410 and 7420 are three and four-input TTL NAND gates, respectively.

In the CMOS line there are several different types of NAND gates. The 4011 is a quad two-input NAND gate, reminiscent of the 7400. The current required for the CMOS device, however, is a lot lower than that required for the equivalent TTL.

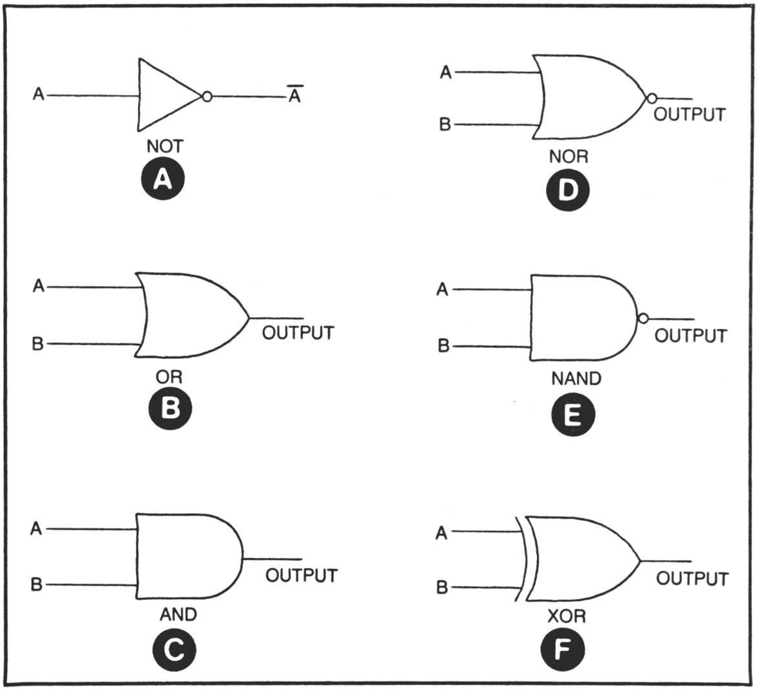


Fig. 1-10. Digital logic symbols for gates.