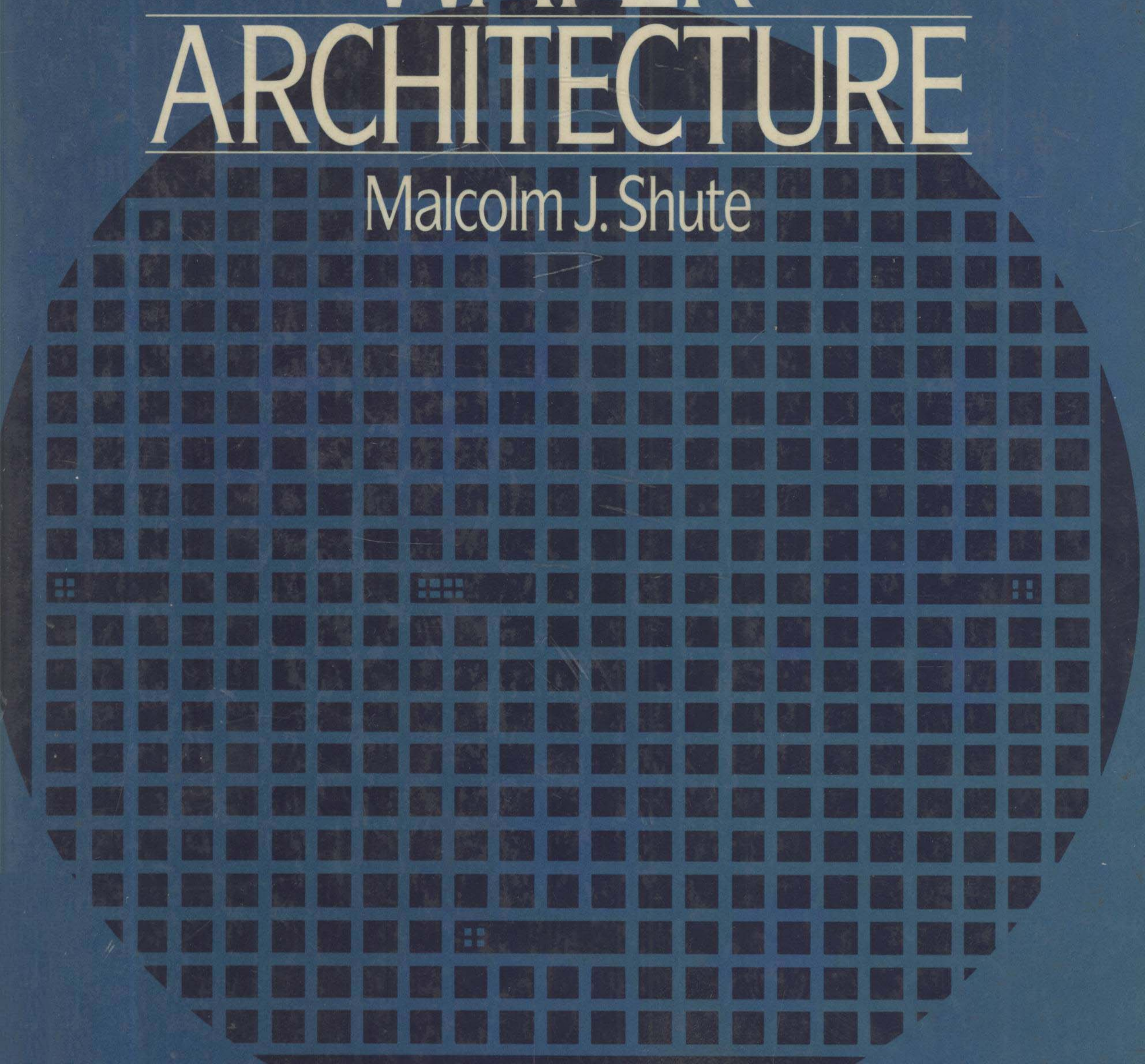
FIFTH GENERATION WAFER ARCHITECTURE

Malcolm J. Shute



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FIFTH GENERATION WAFER ARCHITECTURE

Remembering Gran and Grandpa,
whose inspired purchase (Hellyer 1971)
started me along this path

PREFACE

This volume explores the possible realisation of fifth generation computer architectures through wafer scale integration. It looks at architectural considerations, and designs for fifth generation, non-von-Neumann computer architectures. It also considers fault tolerance, failure tolerance, reconfiguration and wafer scale integration.

As integrated circuit technology improves, the demands on it increase too. Invariably, as hardware is developed for one application, such as a computer architecture, the demands for more functionality, and a consequential proliferation of its components, promptly follow.

Present technology now allows the fabrication of circuits with more than 100 000 transistors per die. Future systems will require even more than this, but how can these circuits be fabricated, given that present technology is stretched nearly to the limit? How can they be designed, given that present designs are already more complicated than the combined road, rail, electricity, gas, water and telephone layouts of a major city? What principles of operation will be employed, given that the current ones now show severe signs of limitation?

This book sets out to answer these questions. It describes a number of the techniques and problems of building the largest single chip computers possible, namely those which occupy an entire wafer of semiconductor. It necessarily spans the many subject areas which influence computer design, in particular those of computer science, suggesting that which is desirable in a computer, and those of microelectronics, indicating that which is possible in a computer.

The skills of the computer engineer will be in great demand to design new architectures for the future breeds of supercomputer. The exciting prospect of finding a successor to a system which has not been surpassed in forty years is now realistic.

The academic study of this subject seems to be polarised into two classes of department: those which study computing, and those which study electronic engineering. However, this book is neither a computer science text, nor one for microelectronics, though both areas are introduced here. Instead, it reports on some exciting research work from various sources around the world which is relevant to computer engineering and computer architecture design.

Although the work which is reported here is currently the subject of research, this book has been written with Master's level teaching in mind. Some of the introductory material is included simply because it is useful to have a basic introduction included in the one text rather than be constantly referred elsewhere. Ample references are given though for further reading.

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Indeed, I am doubly indebted to Chris Hankin, and also to Andrew McCabe, both of whom gave me the highly critical, yet encouraging reviews which an earlier draft of this book needed. I am also very grateful to Drs Chris Jesshope and Tony Ambler, both of whom gave similarly constructive critisms of an even earlier draft.

From the Alvey Wafer Scale Integration project (Alv/Prj/Arch/073) I would like to thank Dr Geoff Sumerling, and Dr Russell Aubusson for their contributions to my general understanding of wafer scale integration; Dr Will Moore for his help with the performance and economics of water scale integration; Professor Mike Lea and Steve Clarke for their frequent seminars, discussions and reports on many aspects of wafer scale integration; Andrew McCabe for his contributions in systolic array and photolithography discussions; Ken Warren for his contributions to my discussion of electrical design issues; Richard Illman who helped me to understand some of the issues of built-in self test and electronic computer-aided design; Ray McKirdy for his help with my discussion of the physical design issues of wafer scale packaging; and each of the group leaders, whose reports I have used as the basis for Chapters 7 and 8.

The help given by my collegues at Middlesex Polytechnic has been invaluable, notably that from: Richard Bayford for his suggestions on the systolic array and built-in self-test sections; Kevin Johnstone for his comments on the electrical design issues sections; Keith Pitt for his contributions to the section on packaging; John White for his help with aspects of ion implantation; Dave Court for his general comments about microelectronics fabrication; Dick Gledhill for his critical comments on the final draft; Dr Richard Seals and Ray Ruocco for their many helpful suggestions concerning the presentation of Chapters 2 and 3. Thank you too, to Linda Moore and her long-suffering team of computer operation and reception staff who bore with me during the writing stages of the lecture notes which finally lead to this book.

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GLOBALLY RESERVED NAMES

A number of terms are used consistently throughout this book. These are listed here, along with a brief definition. Fuller definitions can be found in the glossary at the back of the book, and in the text, mainly on pages 125–35.

a	area of cell	A	area of device
δa	area of fault/failure tolerant overhead per circuit	δA	area of non fault/failure tolerant overhead per device
$\mathbf{a}$	area of circuit with fault/failure tolerance logic	A'	area of complete fault/failure tolerant device
b	reliability of cell	B	reliability of device
δb	reliability of failure tolerant overhead per circuit	δB	reliability of non failure tolerant overhead per device
$\mathbf{b}$	reliability of circuit with failure tolerance logic	B'	reliability of complete failure tolerant device
c	number of cells needed	C	number of cells fabricated
$\mathbf{c}$	number of cells per circuit		
d	diameter of water	D	fault density
δd	unusable margin round wafer		
d'	usable diameter of wafer		
		F	number of faults/failures tolerated by device
h	harvest of cells	H	harvest of devices
j	an integer		
k	an integer	K	number of faults/failures to kill the device
m	number of rows of cells needed	M	number of rows fabricated
n	number of columns of cells needed	N	number of columns fabricated
p	a probability $(0 \leq p \leq 1)$		
r	distance from centre of wafer	R	replication factor
s	number of sides on a cell	S	speed ratio
t	time		
v	yield of circuits	V	yield of fault/failure tolerant devices
		W	usable area of wafer
y	yield of cells	Y	yield of devices

y	yield of circuits with fault/failure tolerance logic	Y'	yield of fault/failure tolerant devices
z	number of test processors per device		

α	fault clustering factor	λ	unit length in circuit layout
θ	angle relative to the major water flat	σ	standard deviation
$\varkappa$	transistor	τ	transistor switching time

crop	number of working devices obtained per wafer	*rco*	relative cell overhead
crop'	number of working fault/failure tolerant devices obtained per wafer	*rda*	relative device area
num	number of devices fabricated per wafer	*rdo*	relative device overhead
rca	relative cell area	*rpa*	relative processor area
		rpo	relative processor overhead
		TC	test coverage
		TQ	test quality

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1

FIFTH GENERATION COMPUTING BACKGROUND

Digital electronic computer design has been an engaging subject for forty years. In this time, some five orders of magnitude of improvement of performance have been attained, but solely through trimming the original design to its present highly honed state. There is no doubt that further improvement of performance is needed, but this cannot be expected to be achieved by mere tuning of the current design any further. As a result, radically new types of computer are being investigated by research groups throughout the world, and this book reports on some of the implications of this work. A study is made of some possible applications in which these machines might be used, programmed and implemented. Necessarily, some degree of conjecture is involved, along with a backward glance at how the predecessors are used, programmed and implemented. The latter is necessary in order to understand why certain techniques and styles are still adopted, and others have been modified or dropped in the light of the lessons of the past.

Over recent decades, many lessons have been learned. Not least, there is a striking similarity between many of the problems and their possible solutions which are found in electronic engineering and computer programming. Both disciplines have learned that the design task becomes very much easier if the system is *hierarchical*, highly *regular* and highly *modular*. They have also learned how efficiency of the final product benefits from the use of *local*, highly *parallel* interconnections within the regular arrangement of modules. However, it is critical that the right *granularity* be found in all cases, and at *all* levels of detail. In other words, the modules must neither be too small and plentiful, nor too large and scarce; similarly, communications should involve messages which are neither too short and prolific, nor too long and infrequent (Figure 1.1).

From the hardware end, computer architects want programming languages which make efficient use of their hardware primitives. From the software end, functional language designers want new computer architectures which support their ideas

Parallel interconnectivity
Local interconnectivity
High modularity
High regularity
Optimum granularity

FIGURE 1.1 *Recurring themes*

efficiently. In a third corner, computer engineers need computer-aided design programs to describe the structures which they intend to implement (Ullman 1984, Sheeran 1985). There are, therefore, many lessons which each group can learn from the others, and much virtue in a closer co-operation between the disciplines to solve the imminent problems in computer design. Since this idea is so central to the aim of this book, the common themes, as listed above, are repeated in Figure 1.1. They will appear many times in this text, even across many subject boundaries. The computer architect must be on the alert for this sort of commonality, and ready to exploit it at all times.

This book concentrates on two seemingly unrelated ideas, namely functional language programming, and wafer scale integration (WSI), and uses them to illustrate the common points of computer science and microelectronics. It does not matter whether WSI ever becomes economically viable. It is not certain even that functional programming will become economic. What is important is that the techniques which are eventually adopted will bear the same sort of interrelationships. Functional language programming and WSI are therefore used here merely as the vehicles with which to illustrate, to catalogue and to classify the points which are made in this book.

A summary is given in the next section (Section 1.1) of the aims and concerns of the fifth generation programme. This helps to set the context: the goals towards which the computer engineering ideas of this book hope to contribute, at least in some small way. The section after (Section 1.2) describes the ideas on which the new architectures must be built if forty years of work and lessons are not to be ignored.

1.1 BACKGROUND STUDY OF FIFTH GENERATION COMPUTING

The fifth generation programme was initiated by the Japanese in 1981 (Simons 1983) to develop computer systems which are faster, more reliable and more intelligent than those of the present, and was scheduled, rather optimistically, for completion in 1991. Western countries, perceiving an imminent domination by the Japanese, followed with their own initiatives. Respectively, they are Alvey (in the UK), ESPRIT (in the EEC), DARPA and MCC (both in the USA). Along with the Japanese ICOT programme, they can be grouped collectively under the 'fifth generation' label.