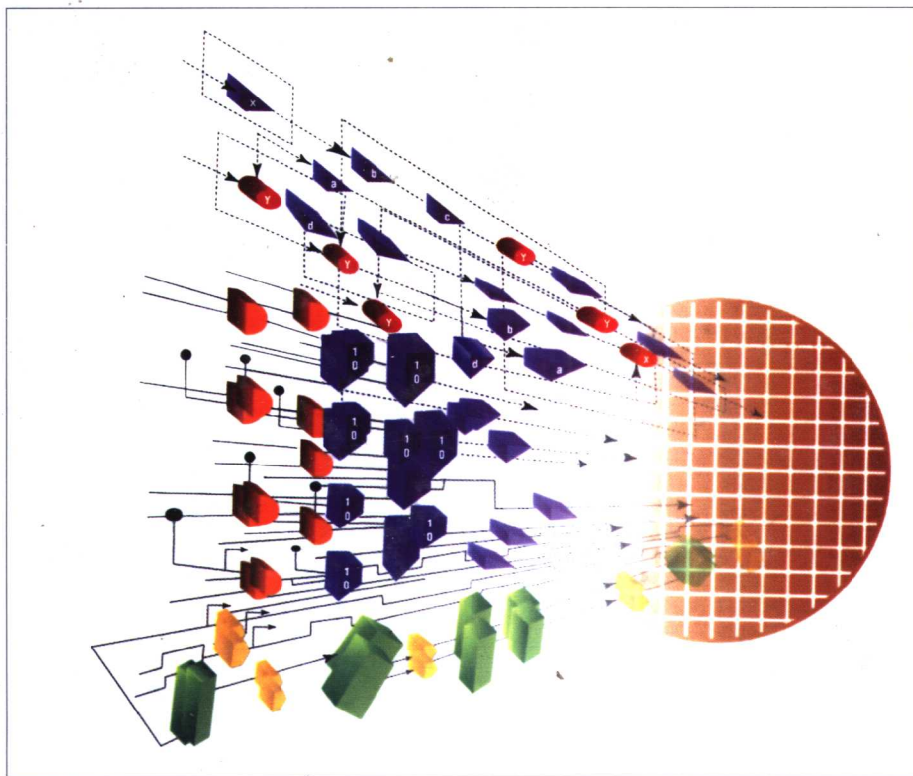




电子工程系列丛书 (影印版)

The ASIC HANDBOOK

ASIC 完备指南



NIGEL HORSPOOL · PETER GORMAN

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Nigel Horspool

Peter Gorman

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出版前言

电子工程是信息科学的基础。高等学校新的教学要求指出：计算机专业和电子学专业的学生应相互学习并渗透到彼此的专业领域，拓宽知识面，以适应信息技术飞速发展的时代。培养通晓相关专业领域知识的人才，已成为 21 世纪理工科教育的迫切要求。为此，我们挑选与信息科学、电子学有关的国外优秀著作，组成“电子工程系列丛书（影印版）”，奉献给国内读者。1999 年我们曾推出了奥本海姆的《信号与系统第 2 版》、奥法尼德斯的《信号处理导论》和拉贝的《数字集成电路》。这三本影印版图书获得了读者的广泛支持。本世纪我们将继续进行这项工作。根据读者的意见，今后我们出版的影印版图书，其开本尺寸不再缩小，基本保持其原版开本尺寸。

我们希望，这套丛书能为国内高校师生、工程技术人员以及科研单位的工作人员提供新的知识和营养，也衷心期待着读者对我们一如既往的支持。

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About the Authors

NIGEL HORSPPOOL has nearly 15 years experience as a designer and project manager on ASIC and other projects. He has worked extensively in image processing, networking, signal processing, and computer graphics, and is now an independent consultant for the Philips International Technology Centre, Leuven, Belgium.

PETER GORMAN has spent over a decade working in FPGA and ASIC design for companies such as 3Com and Philips—where he now serves as senior design consultant. He has held senior design engineering, project management, and design team management roles in projects ranging from digital video and data networking to CD/DVD and USB.

PREFACE

This book is a practical, step-by-step guide to the process of designing digital Application-Specific Integrated Circuits, or ASICs, as they are universally referred to in the industry. These components lie at the heart of nearly all successful electronic products. In the early 1990s, only a relatively small number of companies had in-house ASIC design teams. Outside of these, third-party ASIC design companies serviced the rest of what was still a relatively small market. ASIC know-how was considered an esoteric subject. By the late 1990s, less than 10 years later, this situation had transformed far beyond what anyone could have projected. Access to ASIC expertise had become and remains a survival requirement for all the major companies in the electronics industry and for many small and medium-sized enterprises, too. Such has been the explosive growth in demand for experienced ASIC teams that there is now a significant shortfall in supply. Those companies that do succeed in attracting ASIC expertise and developing it to its maximum potential hold the key to making market-winning products that can yield enormous returns on investment. Herein lies the value of this publication.

The book's aim is to highlight all the complex issues, tasks and skills that must be mastered by an ASIC design team in order to achieve successful project results. It targets ASIC and non-ASIC readers in its scope. The techniques and methodologies prescribed in the book, if properly employed, can significantly reduce the time it takes to convert initial ideas and concepts into right-first-time silicon. Reducing this ever-critical time to market does not simply save on development costs. For new products or new market segments, it provides the opportunity for getting the product there ahead of the competition and, thus, creates the potential for significantly increased market share.

The book covers all aspects of ASIC-based development projects. It includes a detailed overview of the main phases of an ASIC project. Dedicated chapters provide comprehensive coverage of the key technical issues, and a further section of the book deals with relevant management techniques. The technical methods include design for reuse, high-quality design approaches, VHDL/Verilog coding tips and synthesis guidelines. Management skills such as team building are presented, as are ASIC leader tasks such as planning, risk reduction and managing relationships with ASIC vendors.

The book has been written by two ASIC consultants who have worked on many successful ASIC projects in a variety of companies. They are interested in both the technical and management aspects of ASIC design. They are motivated by a desire to find and formulate continuous improvements in approaches to design and development processes. The book was written partly for their own benefit, to capture their own experiences with a view to helping them reproduce successful techniques and methodologies on future projects. Their hope now is that others can also benefit from their work. The book is intended to act as a companion guide to an ASIC team. It can be read in its entirety or subject by subject, as the need arises. It should be reread at the outset of each project and referred to frequently as the project progresses.

Who Should Read This Book

The book is aimed at anyone who wants to understand the elements of an ASIC project. It is also aimed at anyone interested in improving quality, reducing risks and improving time to market. Although some prior knowledge is an advantage in reading some of the more technical chapters, many sections of the book can be read and understood by beginners; therefore, the book is a good starting point for people beginning ASIC careers or contemplating this as an option. Broadly speaking, three groups of people will be interested in the book: non-ASIC engineers, ASIC project managers and ASIC design engineers.

Non-ASIC People

There are many people who have a vested interest in ASIC projects achieving their goals. The ASIC often forms part of a larger overall project that combines software, printed circuit board, mechanical and system design disciplines. In a multi-disciplined team, it is essential that at least a number of key people have a degree of cross-discipline knowledge. Such knowledge enables them to understand the opportunities and limitations that exist when the various disciplines come together, and it allows them to make educated decisions and trade-offs. Additionally, most progressive engineers have

a natural desire to learn about other disciplines on their own initiative, whether it is an absolute requirement or not. This book provides the non-ASIC engineer with the opportunity to understand the world of ASICs.

Senior managers, many of whom predate the ASIC revolution or come from completely different backgrounds, such as marketing or finance, also stand to benefit from this book. In addition to the management essentials that are covered, sections from several of the technical chapters will be within their grasp and will add to their knowledge of what they are dealing with.

ASIC Project Managers

ASIC projects are very complex and require project managers with a wide range of knowledge and skills. Project managers are frequently promoted from design engineering positions, where they may have been focused on relatively narrow or specialist areas. They are, therefore, often thrown in at the deep end when it comes to knowledge of the wider design process and knowledge of management techniques. This book is aimed at those project managers who want to understand and improve the entire ASIC design process. The book clearly explains the project flow and quality approaches to design. It is also useful for project managers who want to improve their project management skills covering issues such as team motivation, managing third-party ASIC vendors and monitoring and managing risks through all the phases of a project.

Design Engineers

Good design engineers are always keen to improve their knowledge and the quality of their work. They may initially participate in only a limited part of the ASIC design process, and it may take several years before they get hands-on exposure to the full spectrum of activities involved. This book defines the full ASIC process, describing good design practices, guidelines for reuse, top-down methodologies and coding and synthesis approaches. The design techniques described will enable engineers to design to a higher quality in shorter time scales.

The Structure of the Book

The book is structured into a number of parts that are formed from one or more chapters. The first chapter, "Phases of an ASIC Project," in section 1, "Project Overview," gives a detailed description of each of the phases of an ASIC project. It provides an overview of technical issues and planning tasks that are required at each stage of the design.

The second section, “Design Techniques,” deals with technical issues, including design reuse, quality design approaches, simulation techniques, VHDL/Verilog coding tips, and synthesis guidelines. These chapters provide practical advice on these topics. They address higher-level problems, such as design approach and quality test environments, rather than presenting an academic course on low-level device physics. They are useful for both seasoned and less experienced design engineers.

The next section, “Project Management,” deals with project management aspects such as planning, risk reduction and dealing with ASIC vendors. The techniques described here can be reapplied to successive projects and refined to match best the characteristics of each new project that is undertaken. Although there are numerous books available on project management, they tend to be quite broad in their scope. The project management section in this book treats the subject in an ASIC-specific context.

The fourth section, “People and Team Management,” aims to provide the project manager with an introduction to the subject of people and team management. Again, this is framed in an ASIC development context. Some basic knowledge of motivation techniques, communication issues and team management theory will help projects to run more smoothly. A well-structured and highly motivated team will bring a project to a successful conclusion sooner and produce quality results that can be reused in future designs.

The book closes with “EDA Tools.” There is an abundance of EDA tools on the market. This chapter picks out a few of the more commonly used types and explains their purpose.

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