PCI & PCI-X 硬件和软件结构与设计（第五版）

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PCI & PCI-X Hardware and Software Architecture and Design, Fifth Edition

[美] Edward Solari　George Willse 著

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内 容 简 介

目前所有新型个人计算机和大多数的服务器均采用 PCI 局部总线规范 2.2 版。PCI-X 代表最先进的 PCI 技术。本书涵盖了 PCI 局部总线规范和 PCI 总线规范 2.2 版和 3.0 版迄今为止的所有内容，最新的工程修改说明（ECN）及工程修改要求（ECR），以及 PCI-X 补充规范 1.0a 版中的新内容。包含了采用所有这三个总线规范进行设计或与之兼容设计的最为完整和正确的信息，全面涵盖了总线段的硬件设计，以及多桥、多总线系统的硬件和软件需求。本书由 Intel 与 Compaq 的设计工程师们协手编写和修订，被认为是 PCI 的“圣经”，同时被认为是 PCI 及 CompactPCI 设计的国际标准。

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序　言

本书讲述了有关 PCI 局部总线硬件和软件方面的知识。不仅仅局限于正式规范中的内容，还进一步阐述了在日常的设计和编程中可能遇到的情况。

本书旨在将 PCI 和 PCI-X 总线的硬件和软件结构的相关知识汇集一起。本书基于 PCI 局部总线规范 2.2 版和 3.0 版（2001 年初颁布）、PCI-to-PCI 桥结构规范 1.1 版、PCI BIOS 规范 2.1 版、PCI-X 补充规范 1.0a 版以及在它们中没有涵盖的其他内容（仅在本书中出现），因此可使读者快速获得有关正确设计基于 PCI 和 PCI-X 的系统、组件或插卡的所有必要信息。

何谓 PCI 3.0？到本书付印时，PCI 3.0 是由 PCI 局部总线规范 2.2 版（PCI 2.2）、PCI-X 补充规范 1.0 版（PCI-X 1.0a）加上最近的工程修改说明合并而成。它还摒弃了只在 5V 电压下的设计。因此本书保留了 PCI 2.2 的中心内容，增加了 PCI-X 1.0a，并指出在 PCI 3.0 规范下新的要求。

本书提供了对 PCI 的完整概述，包括 PCI 与 ISA 总线和即插即用结构的关系。PCI 操作包括 32 位和 64 位数据设计。PCI-X 通过提供分散式交易协议和更高的时钟信号线频率，进一步改进了系统性能。

书中用相当的篇幅讨论了 PCI 资源的信号线定义以及功能相互作用。

书中篇幅最长的一章用于详细讨论总线交易操作，包括不同数据宽度的总线主设备和目标设备之间的相互作用。并通过许多详细的时序图来说明这些交易。

本书涉及了一些重要的硬件细节，比如连接器的使用，平台及插卡设计和机械规范等，还讨论了交易终止和总线所有权等问题。

PCI 总线结构的特性也延伸到软件中。PCI 设备中包含有寄存器，储存了与设备相关的信息。通过这些信息，系统 BIOS 和操作系统软件可以自动配置并管理 PCI 总线资源和插卡。利用自动设备配置功能可以免除硬件跳线和软件配置实用程序。另外，该特性减少了系统资源冲突的可能。当同一资源被分配给两个或多个设备时就可能产生资源冲突。有关 BIOS 和 BIOS 软件接口的内容用两章和几个附录来讨论，并提供了正确使用的详细示例。附录中还叙述了要避免的常见问题，以及其他有用的信息，比如端口地址别名（aliasing）和 VGA 调色板侦测等。

本书分成三个部分。第 1 章和第 2 章提供了 PCI 和 PCI-X 总线比较概括的说明，第 3 章到 15 章专门研究讨论了 PCI 和 PCI-X 硬件的规范细节，第 16 到第 24 章研究讨论了 PCI 和 PCI-X 软件的规范细节。

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The publisher and authors reserve the right to make changes in this publication without notice and without incurring any liability. Changes and corrections will be posted at www.annabooks.com as promptly as practicable.

New to the Fifth Edition

The first four editions of this book covered the PCI local bus specification and the changes due to Engineering Change Notices and Engineering Change Requests. This edition of the book includes everything relative to revision 2.2 and 3.0 (as of press time) of the PCI local bus specification, plus the most recent Engineering Change Notices and Engineering Change Requests. This fifth edition also includes the new information concerning revision 1.0a of the PCI-X addendum specification. PCI-X represents an enhancement to PCI; consequently, this book has retained the emphasis on PCI and provides the PCI-X information as incremental to PCI. Please see further discussion in the *Preface* relating to PCI 3.0, PCI 2.2, and PCI-X 1.0a.

This edition of the book references the power management and hot plug attributes of PCI and PCI-X. Due to the complexity of these topics, this book leaves complete discussion of these topics to other books. Please see *PCI Power Management* by George Willse *et. al.* and *PCI Hot-Plug Application and Design* by Alan Goodrum. Both of these books are available at www.annabooks.com.

This edition of the book also references PCI/PCI BRIDGES and PCI-X/PCI-X BRIDGES. Due to the complexity of these topics, this book leaves complete discussion of these topics to the actual specifications from the PCI SIG and to the specifications from the manufacturers of the actual bridge chips. The exact bridge characteristics can vary depending on the architecture of the bridge chip.

In addition, the authors and publisher appreciate the feedback we have received from alert readers, who are responsible for some of the corrections and clarifications that have been added to this edition. You are always welcome to contact us at *feedback@annabooks.com.*

Dedications

As with my previous books

The patience and understanding by my wife (who never sees me when I undertake a project like this) is greatly appreciated.

The education, discipline, and dedication imparted to me by my mother and father continues to be invaluable to projects like this.

Finally, working with George Willse on this and other projects continues to be a great pleasure. His dedication to a quality product is refreshing – it is very rare to find someone who is willing to do on-going work to maintain and update a published book in a timely fashion.

Ed

To Brigitte –
The best compass for my life this side of heaven.

To Travis and Tyler -
What a privilege to hear you call me "Dad". I am so proud of you.

And to Ed -
For the encouragement years ago to take the road less traveled, for which I shall always be grateful.

George

Preface
... Including "What is PCI 3.0 ?"

The major cause of low performance in computer systems is the time it takes to execute memory and I/O functions related to peripheral devices such as LAN, SCSI, and motion video. Low bus bandwidth adversely impacts data processing and screen output. In recent years, two independent approaches have been taken to solve this low bandwidth obstacle. First, peripheral device vendors have implemented new architectures to increase the data transfer rates between their devices and other system resources. The second approach is the movement of peripheral devices from lower to higher performance buses.

The PCI Bus (originally named Peripheral Component Interconnect, a name that is now inappropriate and that should no longer be used) was the first widely accepted bus architecture to address the performance issues associated with personal computers. The PCI bus also addresses multiple bus master support. The PCI bus resource and add-in card interface is also processor independent, allowing full support of present and future processors of different architectures.

The features of the PCI bus architecture also extend into the software realm. PCI devices incorporate registers that contain device-specific information. This information enables System BIOSs and operating system level software to automatically configure and manage PCI bus resources and add-in cards. Automatic device configuration eliminates the need for hardware jumpers and software configuration utilities. In addition, this feature reduces the possibility of system resource conflicts that can occur when two or more devices are assigned the same resource.

Recently, the PCI bus architecture has been enhanced by PCI-X. The purpose of PCI-X is to improve system performance by enhancing PCI with the inclusion of Split Transaction protocol and higher CLK signal line frequencies.

The major goal of this book is to document in one location both the hardware and software architectures of the PCI and PCI-X buses. This book is based on the PCI local bus specification Revision 2.2, PCI-to-PCI Bridge Architecture Specification Revision 1.1, PCI BIOS Specification Revision 2.1, PCI-X addendum specification 1.0a, and additional information not incorporated in any of these (and only available in this book). This enables you to quickly access ALL the information necessary to ensure the proper design of PCI and PCI-X based systems, components, or add-in cards.

The book is divided into three sections. Chapters 1 and 2 are introductory and provide a very general overview of the hardware and software for the PCI and PCI-X buses. Chapters 3 through 15 are dedicated to the detailed specification

and discussion of PCI and PCI-X bus hardware. Finally, Chapters 16 through 24 are dedicated to the detailed specification and discussion of PCI and PCI-X bus software.

What is PCI 3.0? ... Just prior to printing this book, the PCI SIG announced Revision 3.0 of PCI local addendum specification (PCI 3.0). As of this book's printing date, PCI 3.0 primarily consists of the merger of Revision 2.2 of the PCI local bus specification (PCI 2.2) and Revision 1.0a of the PCI-X addendum specification (PCI-X 1.0a). PCI 3.0 of course includes any ECNs (Engineering Change Notices) subsequent to PCI 2.2 and PCI-X 1.0a; this book includes all of the ECNs approved at the time of printing. PCI 3.0 also places one new requirement not part of PCI 2.2 and PCI-X 1.0a. This requirement allows the implementation only of add-in cards that are compliant to either the 3.3 volt only or the universal I/O signaling add-in card protocols. The purpose is to facilitate the adoption of PCI-X by removing the "design comfort" of 5 volt only signaling permitted by PCI 2.2. That is, PCI 3.0 compliant bus segments will not support add-in cards keyed for 5 volt only signaling. There has been a concern that the adoption of PCI-X (and thus the associated benefits) have been slow because bus segments operating in PCI-X mode require 3.3 volt signaling. Prior to PCI 3.0, bus segments operating in PCI mode only required support of 5 volt signaling. PCI 3.0 forces the PCI mode to move to 3.3 volt signaling and thus removes the "perceived" 3.3 volt signaling barrier of PCI-X 1.0a. See further discussion in Chapter 11: *Reset, Power, and Signal Line Initialization*, Chapter 13: *Connector, Platform, and Add-in Card Design,* and Chapter 15: *Mechanical Specification* for more information.

This book has retained the focus of PCI 2.2 while adding the incremental information relative to PCI-X 1.0a. This approach permits those of you working with the "traditional" PCI add-in cards and components to have a clear understanding of the PCI requirements. Those of you interested in designing add-in cards and components compliant to PCI-X 1.0a will also easily see the incremental design requirements. You are advised to periodically check with the PCI SIG web site (http://www.pcisig.com) and the errata sheet for this book (posted at http://www.annabooks.com.) for the latest information.

Annabooks and we are all interested in the continuing evolution, clarification, and corrections to this book. Please direct any related inputs to Annabooks at *feedback@annabooks.com.*

The publisher and authors would also like to thank Norm Rasmussen, Brad Hosler, Scott McMorrow, Laurie Fleisher, and Suba Vanka for taking the time to review the original PCI centric text prior to publication. We would also like to thank Mr. Nagumo and Mr. Fukushima of IDES Japan for their corrections made during their Japanese translation of this book. We are also grateful for the efforts

extended by Tim Bohan of Annabooks during the production of both the Japanese and English editions of this work.

Of special note is the assistance rendered by Norman Rasmussen and Brad Hosler ... two of the key PCI experts on the planet. They dedicated excessive hours of their own time to this project. Their diligent review, comments, corrections, and insights were invaluable during the preparation of this book. We would also like to acknowledge the help provided by Alan Goodrum and Dwight Riley on the PCI-X portions of the book. Both of these gentlemen were instrumental in the technical definition and implementation of PCI-X.

We would also like to thank the PCI Special Interest Group and, in particular, David Schuler and Mike Bailey (the previous PCI SIG Steering Committee Chairman) for permission to extract and use portions of the PCI local bus specifications. Also thanks go to William Samaris for his help with the details of the electrical specifications. Most recently, relative to PCI-X, we would like to acknowledge the help we received from Dwight Riley and Roger Tipley (the current PCI SIG Steering Committee Chairman).

Last, but certainly not least, we would like to thank John Choisser for editing this and other editions of the book. A book of this size and technical detail requires a tremendous amount of quality editing ... which John provided.

Ed Solari and George Willse

Oregon

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CHAPTER 1

ISA SYSTEM ARCHITECTURAL OVERVIEW

This chapter consists of the following subchapters:

1.0 ISA SYSTEM ARCHITECTURE

The architecture of ISA compatible systems can be viewed as four individual layers. Each layer has a defined interface between itself and the other layers. Utilizing this layered architecture permits each layer to be developed and modified independently of the others. It also translates into portability for the upper software layers.

Even though not specifically mentioned, the architectural concepts described for an ISA system also apply to EISA and Micro Channel systems.

The term "system" represents the entire hardware and software required to create an ISA compatible personal computer. The term "platform" represents the physical collection of hardware on a single circuit board. The platform usually contains connectors to support the attachment of add-in cards.

1.1 LAYER 1-PLATFORM HARDWARE

At the innermost layer of the architecture lies the platform hardware. This hardware consists of the platform with its integrated components and add-in cards that expand platform features. The simplest architecture of an ISA compatible platform is shown in Figure 1-1. The HOST CPU, cache, and memory (HDRAM) all reside on the HOST bus. The HOST bus is attached to an ISA bus (or EISA or Micro-Channel, depending on the platform) via a BRIDGE. The ISA bus contains ISA bus connectors and ISA compatible resources.

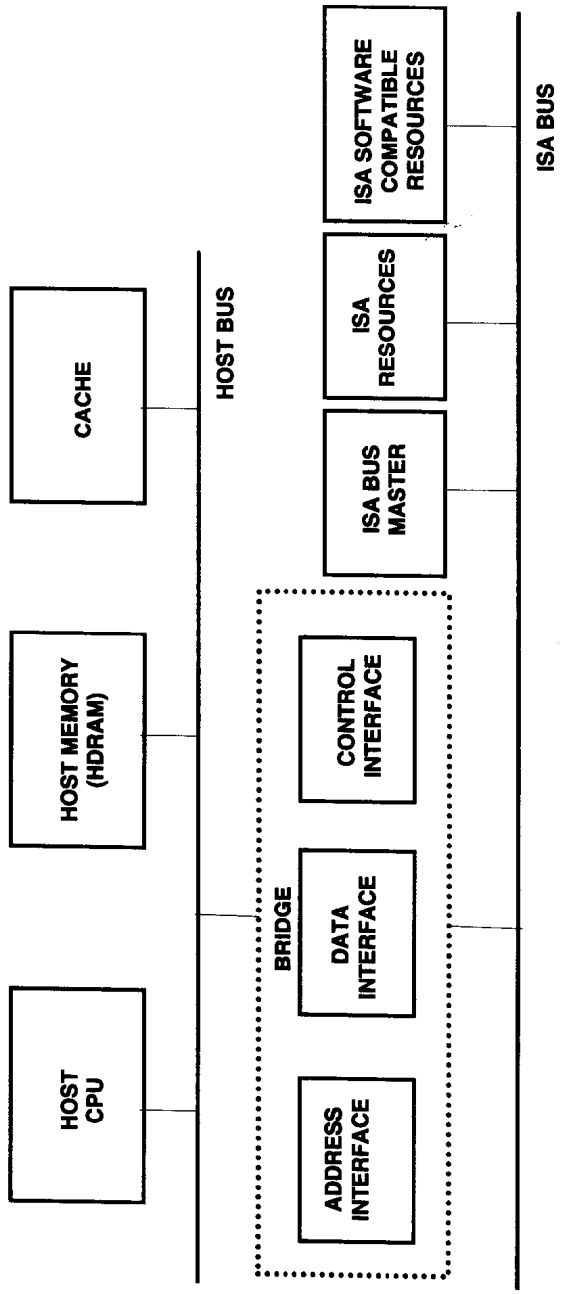

Figure 1-1: Generic ISA Platform Architecture