电子信息前沿技术丛书

Design of Analog CMOS Integrated Circuits, Second Edition

模拟CMOS集成电路设计

（第2版）

◎[美] Behzad Razavi 著　池保勇 编译

清華大學出版社

电子信息前沿技术丛书

模拟CMOS
集成电路设计

（第2版）

◎［美］Behzad Razavi 著
池保勇 编译

常州大学图书馆
藏书章

清華大學出版社
北京

Behzad Razavi
Design of Analog CMOS Integrated Circuits，second edition
ISBN：978-0-07-252493-2

Copyright © 2018 by McGraw-Hill Education.
All Rights reserved. No part of this publication may be reproduced or transmitted in any form or by any means，electronic or mechanical，including without limitation photocopying，recording，taping，or any database，information or retrieval system，without the prior written permission of the publisher.
This authorized English Adaptation is jointly published by McGraw-Hill Education and Tsinghua University Press Limited. This edition is authorized for sale in the People's Republic of China only，excluding Hong Kong，Macao SAR and Taiwan.
Copyright © 2018 by McGraw-Hill Education and Tsinghua University Press Limited.
版权所有。未经出版人事先书面许可，对本出版物的任何部分不得以任何方式或途径复制或传播，包括但不限于复印、录制、录音或通过任何数据库、信息或可检索的系统。
本授权英文影印删减版由麦格劳-希尔（亚洲）教育出版公司和清华大学出版社有限公司合作出版。此版本经授权仅限于中华人民共和国境内（不包括中国香港、澳门特别行政区及中国台湾地区）销售发行。
版权© 2018 由麦格劳-希尔（亚洲）教育出版公司与清华大学出版社有限公司所有。

北京市版权局著作权合同登记号　图字：01-2017-5691

本书封面贴有 McGraw-Hill 公司防伪标签，无标签者不得销售。
版权所有，侵权必究。侵权举报电话：010-62782989　13701121933

图书在版编目（CIP）数据

模拟 CMOS 集成电路设计：第 2 版＝Design of Analog CMOS Integrated Circuits 2nd Edition：英文/（美）毕查德·拉扎维（Behzad Razavi），池保勇编译. —北京：清华大学出版社，2018
（电子信息前沿技术丛书）
ISBN 978-7-302-48985-6

Ⅰ. ①模…　Ⅱ. ①毕…　②池…　Ⅲ. ①CMOS 电路－电路设计－教材－英文　Ⅳ. ①TN432.02

中国版本图书馆 CIP 数据核字（2017）第 287680 号

责任编辑：文　怡
封面设计：台禹微
责任校对：白　蕾
责任印制：王静怡

出版发行：清华大学出版社
　　网　　址：http://www.tup.com.cn，http://www.wqbook.com
　　地　　址：北京清华大学学研大厦 A 座　　**邮　　编**：100084
　　社 总 机：010-62770175　　**邮　　购**：010-62786544
　　投稿与读者服务：010-62776969，c-service@tup.tsinghua.edu.cn
　　质量反馈：010-62772015，zhiliang@tup.tsinghua.edu.cn
　　课件下载：http://www.tup.com.cn，010-62795954
印 装 者：三河市君旺印务有限公司
经　　销：全国新华书店
开　　本：185mm×260mm　　**印　　张**：41.75　　**字　　数**：1008 千字
版　　次：2005 年 8 月第 1 版　2018 年 1 月第 2 版　　**印　　次**：2018 年 1 月第 1 次印刷
印　　数：1～2000
定　　价：128.00 元

产品编号：075764-01

影印版序

拉扎维教授编著的《模拟 CMOS 集成电路设计》一书出版于 2001 年。由于其内容编排合理，讲述方式由浅入深，注重电路直观分析能力的培养，并安排了大量的例题及课后习题，该书一经面世，即在世界范围内引起了强烈反响，迅速被国内外各大高校采用为微电子、电子工程等专业的本科生或研究生教材，成为与 P. R. Gray 等编著的 *Analysis and Design of Analog Integrated Circuits* 齐名的模拟集成电路经典教材。

但是，从 2001 年至今，CMOS 工艺已经发生了巨大变化，晶体管特征尺寸不断缩小，导致衡量晶体管性能的电路参数（跨导效率、特征频率和本征增益）发生了很大变化，加之电源电压不断下降导致传统电路拓扑结构的应用受到限制，其间也出现了新的模拟集成电路分析与设计方法，以上这些因素都要求对原来的教材内容进行改写。本书第 2 版正是在此背景下编写的。该版在保留第 1 版编写特色的前提下，大幅增加了电路设计的叙述篇幅，如第 11 章专门讨论了纳米 CMOS 工艺下的电路设计策略和循序渐进的运算放大器设计方法，有利于培养读者的电路设计能力。该版本还引入了波特图和 MiddleBrook 分析法来分析反馈网络的特性，增加了奈奎斯特稳定性判据、鳍式晶体管（FinFET）、新偏置电路技术及低压能隙基准源等内容，有利于读者跟踪最新的模拟集成电路设计技术。该版本还增加了很多新的例题，并更新了课后习题。我相信改版后的这本教材更加适合于现阶段相关专业本科生和研究生课程教学的需要，也适合作为一线工作的集成电路设计工程师的常用参考书。

由 McGraw-Hill 出版社出版的《模拟 CMOS 集成电路设计（第 2 版）》共包含 19 章内容。清华大学出版社在引进影印版本时，根据国内教育教学情况进行了删减：①考虑到振荡器和锁相环属于高频电路内容，专门的通信电路或射频电路教材均会对其进行详细介绍，故将原版本中的第 15 章“振荡器”和第 16 章“锁相环”相关内容删除；②考虑到国内相关专业普遍开设了专门的“半导体器件物理”“集成电路工艺”等课程，将原版本中的第 17 章“MOS 器件与模型”和第 18 章“CMOS 制造工艺”相关内容删除。

池保勇

2017 年 10 月

第 2 版前言

当我将这本书第 1 版的出版提案交给出版商时，他们向我提出了两个问题：①在数字化世界中，模拟电路书籍有什么样的未来需求？②出版一本仅介绍 CMOS 工艺的电路设计书籍是否明智？这本书标题中的关键词“模拟”和 CMOS 正好反映了他们的问题。

幸运的是，这本书出版后受到了学生、教师和工程师的热烈欢迎，已经被世界范围内的数百所高校采用为教材或参考书，翻译成五种语言，并被引用 6500 余次。

从这本书的第 1 版出版至今，尽管模拟电路设计的许多基本原理没有变化，但由于下面的这些原因，需要对这本书进行改版：CMOS 工艺向更小尺寸、更低电源电压的技术迁移，新的分析与设计方法以及某些内容需要更详细的阐述。这次改版主要体现在如下方面：

- 更加强调现代 CMOS 工艺，并汇聚成新增加的一章（第 11 章），该章讨论了纳米 CMOS 工艺下的设计策略和循序渐进的运算放大器设计方法；
- 通过引入波特图和 Middlebrook 分析法，扩展了反馈内容；
- 考虑到通常使用的波特图判据无法用来判断某些通用系统的稳定性，增加了使用奈奎斯特判据进行稳定性分析的新章节；
- 增加了鳍式晶体管（FinFET）的内容；
- 增加了边栏突出纳米 CMOS 电路设计的重要知识点；
- 增加了偏置电路技术的新章节；
- 增加了介绍低压能隙基准源的内容；
- 新增加了 100 多个例题。

一些任课教师问我们为何仍以平方率器件来开始讲解。这主要有两个原因：① 这样的安排作为一个直观的切入点，为分析放大器的可允许电压摆幅等性能提供了特别的价值；②尽管 16nm 及更先进工艺的 FinFET 器件具有非常短的沟道长度，这些器件仍近似表现出平方率器件特性。

本书附有课后习题解答和一套新的课件，可以从 www.mhhe.com/razavi 下载。

毕查德・拉扎维

2015 年 7 月

试读结束：需要全本请在线购买： www.ertongbook.com

第1版前言

在过去的20年中，CMOS工艺在模拟集成电路领域得到广泛应用，提供了低成本、高性能的实现方案，并逐渐占据主流市场位置。虽然硅基双极型工艺和Ⅲ-Ⅴ族器件仍能发现应用商机，但对于目前复杂的混合信号系统集成来说，只有CMOS工艺是一种可行的实现方案。随着沟道长度逐步缩小到0.05μm，CMOS工艺将在未来的20年中继续在电路设计中得到广泛应用。

模拟电路设计技术也随着工艺技术的发展而发展。包含几十个晶体管、处理微弱连续时间信号的高压、高功耗模拟电路已经逐渐被包含数千个器件、以处理强离散时间信号为主的低压、低功耗系统所代替。举例来说，10年前使用的许多模拟电路技术由于无法适应在低压下工作而不再被采用。

本书讲述模拟CMOS集成电路的分析与设计方法，重点阐述当前产业背景下学生和一线工作的工程师需要掌握的基本原理和新理念新方法。由于模拟电路设计同时强调直观认识和严密分析，每一个概念都先从直观认识的角度引入，然后进行仔细的分析。目标是打下坚固的基础，并培养通过审视来分析电路的方法，从而使读者能了解在哪些电路中可以做何种简化，并预期每一步简化中引入的误差大小。这种处理方式也使读者不需花费额外的精力就可以用这本书中学到的概念来分析双极型电路。

我已经在UCLA和工业界讲授过这本书中的绝大部分内容，每一次授课时都会对讲授的顺序、方式和内容进行重新梳理。就像读者能从此书中看到的那样，我在编著或讲授时遵从了四条黄金法则：①我会就读者为什么需要了解即将要学习的概念进行解释；②我将自己放在读者的位置，预测他/她在第一次阅读各部分内容时可能会遇到的问题；③考虑到第二条规则，我假设自己只掌握了读者第一次阅读时所拥有的知识，并尽力和读者一起成长，因此会经历与读者同样的思索过程；④我先以简单但可能不太精确的语言来介绍核心概念，并逐渐增加必要的修正来达到最终精确的想法。最后一条规则在讲授电路课时尤为重要，因为它允许读者观察拓扑的演变，从而能够同时学会电路的分析与综合。

这本教材包含有16章，每章内容和章节顺序都经过仔细衡量，从而为无论是自学还是3个月或6个月的学期课程学习提供自然的流程。与一些其他的模拟电路设计教科书不同，我们在开始时仅介绍最少量的MOS器件物理的内容，而将更深入的器件特性和制造工艺细节分配到了后面的各章中。对于一个专家来说，这本书介绍的初级器件物理内容可能显得过度简化了，但是我的经验表明：①初次接触本书内容的读者在他们学习电路知识前并不能领会高阶器件效应和制造工艺，因为他们不明白其中的相关性；②如果表达合适，这种简单阐述也包含了学习基本电路所需要的足够知识；③在读者进行了大量的电路分析和设计之后，能够更加有针对性地学习先进的器件机理和工艺步骤。

第1章为读者提供了学习这本书的背景。

第2章讲述了MOS器件的基本物理知识和工作原理。

第3～5章分别讲述单级放大器、差分放大器和电流镜，介绍了通过有效的分析工具来审视定量分析基本电路的行为。

第6～7章介绍了噪声和频率响应这两个电路的非理想特性。比较早地介绍噪声有利于读者领会在后续电路分析时考虑其影响。

第8～10章分别讲述了反馈、运算放大器和反馈系统中的稳定性。通过对反馈特性的分析，激励读者去设计高性能、稳定的运算放大器并理解在速度、精度和功耗等方面的折中考虑。

第11～13章涵盖了更深入的内容：能隙基准源、基本的开关电容电路、非线性和失配效应。这些内容在目前绝大多数的模拟和混合信号系统中非常重要，因此被纳入本书中。

第14章涉及高阶MOS器件效应和模型，重点在电路设计方面的含义。如果喜欢，这一章可以直接跟在第2章之后学习。

第15章描述了CMOS制造工艺，并简单介绍了版图设计规则。

第16章讲述了模拟和混合信号电路的版图设计和封装技术，描述了许多直接影响电路性能的工程性因素和各种解决技术。

读者需要具有电子电路和器件的基本知识，包括pn结、小信号工作的概念、等效电路和简单偏置。如果用作高年级本科生的选修课程，3个月学期的课程可以讲授第1～8章的内容，6个月学期的课程可以讲授第1～10章的内容。如果用作研究生一年级的课程，3个月学期的课程可以讲授第1～11章及第12～14章中某一章的内容，6个月学期的课程可以讲授本书的全部内容。

每一章内容后的课后习题可以扩展读者对本章内容的理解，并补充对实际工程因素的认识。授课教师可以获取课后习题的解答。

Brief Contents

1 **Introduction to Analog Design** **1**
2 **Basic MOS Device Physics** **7**
3 **Single-Stage Amplifiers** **45**
4 **Differential Amplifiers** **100**
5 **Current Mirrors and Biasing Techniques** **134**
6 **Frequency Response of Amplifiers** **173**
7 **Noise** **219**
8 **Feedback** **274**
9 **Operational Amplifiers** **344**
10 **Stability and Frequency Compensation** **410**
11 **Nanometer Design Studies** **459**
12 **Bandgap References** **509**
13 **Introduction to Switched-Capacitor Circuits** **539**
14 **Nonlinearity and Mismatch** **576**
15 **Layout and Packaging** **607**

Contents

1 Introduction to Analog Design 1
  1.1 Why Analog? 1
    1.1.1 Sensing and Processing Signals 1
    1.1.2 When Digital Signals Become Analog 2
    1.1.3 Analog Design Is in Great Demand 3
    1.1.4 Analog Design Challenges 4
  1.2 Why Integrated? 4
  1.3 Why CMOS? 5
  1.4 Why This Book? 5
  1.5 Levels of Abstraction 5

2 Basic MOS Device Physics 7
  2.1 General Considerations 8
    2.1.1 MOSFET as a Switch 8
    2.1.2 MOSFET Structure 8
    2.1.3 MOS Symbols 9
  2.2 MOS I/V Characteristics 10
    2.2.1 Threshold Voltage 10
    2.2.2 Derivation of I/V Characteristics 12
    2.2.3 MOS Transconductance 19
  2.3 Second-Order Effects 20
  2.4 MOS Device Models 26
    2.4.1 MOS Device Layout 26
    2.4.2 MOS Device Capacitances 27
    2.4.3 MOS Small-Signal Model 31
    2.4.4 MOS SPICE models 34
    2.4.5 NMOS Versus PMOS Devices 35
    2.4.6 Long-Channel Versus Short-Channel Devices 35
  2.5 Appendix A: FinFETs 36
  2.6 Appendix B: Behavior of a MOS Device as a Capacitor 37

3 Single-Stage Amplifiers ... 45
- 3.1 Applications ... 45
- 3.2 General Considerations ... 45
- 3.3 Common-Source Stage ... 47
  - 3.3.1 Common-Source Stage with Resistive Load ... 47
  - 3.3.2 CS Stage with Diode-Connected Load ... 52
  - 3.3.3 CS Stage with Current-Source Load ... 58
  - 3.3.4 CS Stage with Active Load ... 59
  - 3.3.5 CS Stage with Triode Load ... 60
  - 3.3.6 CS Stage with Source Degeneration ... 61
- 3.4 Source Follower ... 68
- 3.5 Common-Gate Stage ... 75
- 3.6 Cascode Stage ... 82
  - 3.6.1 Folded Cascode ... 90
- 3.7 Choice of Device Models ... 92

4 Differential Amplifiers ... 100
- 4.1 Single-Ended and Differential Operation ... 100
- 4.2 Basic Differential Pair ... 103
  - 4.2.1 Qualitative Analysis ... 104
  - 4.2.2 Quantitative Analysis ... 106
  - 4.2.3 Degenerated Differential Pair ... 116
- 4.3 Common-Mode Response ... 118
- 4.4 Differential Pair with MOS Loads ... 123
- 4.5 Gilbert Cell ... 126

5 Current Mirrors and Biasing Techniques ... 134
- 5.1 Basic Current Mirrors ... 134
- 5.2 Cascode Current Mirrors ... 139
- 5.3 Active Current Mirrors ... 146
  - 5.3.1 Large-Signal Analysis ... 149
  - 5.3.2 Small-Signal Analysis ... 152
  - 5.3.3 Common-Mode Properties ... 156
  - 5.3.4 Other Properties of Five-Transistor OTA ... 159
- 5.4 Biasing Techniques ... 160
  - 5.4.1 CS Biasing ... 161
  - 5.4.2 CG Biasing ... 164
  - 5.4.3 Source Follower Biasing ... 165
  - 5.4.4 Differential Pair Biasing ... 166

6 Frequency Response of Amplifiers ... 173
- 6.1 General Considerations ... 173
  - 6.1.1 Miller Effect ... 174
  - 6.1.2 Association of Poles with Nodes ... 179
- 6.2 Common-Source Stage ... 180
- 6.3 Source Followers ... 188

6.4 Common-Gate Stage ... 193
6.5 Cascode Stage ... 196
6.6 Differential Pair ... 198
6.6.1 Differential Pair with Passive Loads ... 198
6.6.2 Differential Pair with Active Load ... 201
6.7 Gain-Bandwidth Trade-Offs ... 203
6.7.1 One-Pole Circuits ... 204
6.7.2 Multi-Pole Circuits ... 205
6.8 Appendix A: Extra Element Theorem ... 206
6.9 Appendix B: Zero-Value Time Constant Method ... 208
6.10 Appendix C: Dual of Miller's Theorem ... 212

7 Noise ... 219
7.1 Statistical Characteristics of Noise ... 219
7.1.1 Noise Spectrum ... 221
7.1.2 Amplitude Distribution ... 224
7.1.3 Correlated and Uncorrelated Sources ... 225
7.1.4 Signal-to-Noise Ratio ... 226
7.1.5 Noise Analysis Procedure ... 227
7.2 Types of Noise ... 228
7.2.1 Thermal Noise ... 228
7.2.2 Flicker Noise ... 234
7.3 Representation of Noise in Circuits ... 236
7.4 Noise in Single-Stage Amplifiers ... 243
7.4.1 Common-Source Stage ... 244
7.4.2 Common-Gate Stage ... 249
7.4.3 Source Followers ... 253
7.4.4 Cascode Stage ... 254
7.5 Noise in Current Mirrors ... 254
7.6 Noise in Differential Pairs ... 256
7.7 Noise-Power Trade-Off ... 263
7.8 Noise Bandwidth ... 264
7.9 Problem of Input Noise Integration ... 265
7.10 Appendix A: Problem of Noise Correlation ... 265

8 Feedback ... 274
8.1 General Considerations ... 274
8.1.1 Properties of Feedback Circuits ... 275
8.1.2 Types of Amplifiers ... 282
8.1.3 Sense and Return Mechanisms ... 284
8.2 Feedback Topologies ... 286
8.2.1 Voltage-Voltage Feedback ... 286
8.2.2 Current-Voltage Feedback ... 291
8.2.3 Voltage-Current Feedback ... 294
8.2.4 Current-Current Feedback ... 297
8.3 Effect of Feedback on Noise ... 298

试读结束：需要全本请在线购买： www.ertongbook.com

8.4 Feedback Analysis Difficulties ... 299
8.5 Effect of Loading ... 303
  8.5.1 Two-Port Network Models ... 303
  8.5.2 Loading in Voltage-Voltage Feedback ... 304
  8.5.3 Loading in Current-Voltage Feedback ... 308
  8.5.4 Loading in Voltage-Current Feedback ... 310
  8.5.5 Loading in Current-Current Feedback ... 313
  8.5.6 Summary of Loading Effects ... 315
8.6 Bode's Analysis of Feedback Circuits ... 315
  8.6.1 Observations ... 315
  8.6.2 Interpretation of Coefficients ... 317
  8.6.3 Bode's Analysis ... 320
  8.6.4 Blackman's Impedance Theorem ... 325
8.7 Middlebrook's Method ... 331
8.8 Loop Gain Calculation Issues ... 332
  8.8.1 Preliminary Concepts ... 332
  8.8.2 Difficulties with Return Ratio ... 334
8.9 Alternative Interpretations of Bode's Method ... 336

9 Operational Amplifiers ... 344
9.1 General Considerations ... 344
  9.1.1 Performance Parameters ... 344
9.2 One-Stage Op Amps ... 349
  9.2.1 Basic Topologies ... 349
  9.2.2 Design Procedure ... 353
  9.2.3 Linear Scaling ... 354
  9.2.4 Folded-Cascode Op Amps ... 355
  9.2.5 Folded-Cascode Properties ... 358
  9.2.6 Design Procedure ... 359
9.3 Two-Stage Op Amps ... 361
  9.3.1 Design Procedure ... 363
9.4 Gain Boosting ... 364
  9.4.1 Basic Idea ... 364
  9.4.2 Circuit Implementation ... 368
  9.4.3 Frequency Response ... 371
9.5 Comparison ... 373
9.6 Output Swing Calculations ... 373
9.7 Common-Mode Feedback ... 374
  9.7.1 Basic Concepts ... 374
  9.7.2 CM Sensing Techniques ... 377
  9.7.3 CM Feedback Techniques ... 380
  9.7.4 CMFB in Two-Stage Op Amps ... 386
9.8 Input Range Limitations ... 388
9.9 Slew Rate ... 390

9.10 High-Slew-Rate Op Amps 397
  9.10.1 One-Stage Op Amps 397
  9.10.2 Two-Stage Op Amps 399
9.11 Power Supply Rejection 400
9.12 Noise in Op Amps 402

10 Stability and Frequency Compensation 410
10.1 General Considerations 410
10.2 Multipole Systems 414
10.3 Phase Margin 416
10.4 Basic Frequency Compensation 420
10.5 Compensation of Two-Stage Op Amps 426
10.6 Slewing in Two-Stage Op Amps 433
10.7 Other Compensation Techniques 436
10.8 Nyquist's Stability Criterion 439
  10.8.1 Motivation 439
  10.8.2 Basic Concepts 440
  10.8.3 Construction of Polar Plots 442
  10.8.4 Cauchy's Principle 447
  10.8.5 Nyquist's Method 447
  10.8.6 Systems with Poles at Origin 450
  10.8.7 Systems with Multiple 180° Crossings 454

11 Nanometer Design Studies 459
11.1 Transistor Design Considerations 459
11.2 Deep-Submicron Effects 460
11.3 Transconductance Scaling 463
11.4 Transistor Design 466
  11.4.1 Design for Given I_D and $V_{DS,min}$ 466
  11.4.2 Design for Given g_m and I_D 469
  11.4.3 Design for Given g_m and $V_{DS,min}$ 470
  11.4.4 Design for a Given g_m 471
  11.4.5 Choice of Channel Length 472
11.5 Op Amp Design Examples 472
  11.5.1 Telescopic Op Amp 473
  11.5.2 Two-Stage Op Amp 487
11.6 High-Speed Amplifier 495
  11.6.1 General Considerations 496
  11.6.2 Op Amp Design 500
  11.6.3 Closed-Loop Small-Signal Performance 501
  11.6.4 Op Amp Scaling 502
  11.6.5 Large-Signal Behavior 505
11.7 Summary 507

12 Bandgap References **509**
12.1 General Considerations 509
12.2 Supply-Independent Biasing 509
12.3 Temperature-Independent References 513
12.3.1 Negative-TC Voltage 513
12.3.2 Positive-TC Voltage 514
12.3.3 Bandgap Reference 515
12.4 PTAT Current Generation 523
12.5 Constant-G_m Biasing 524
12.6 Speed and Noise Issues 525
12.7 Low-Voltage Bandgap References 529
12.8 Case Study 533

13 Introduction to Switched-Capacitor Circuits **539**
13.1 General Considerations 539
13.2 Sampling Switches 543
13.2.1 MOSFETS as Switches 543
13.2.2 Speed Considerations 547
13.2.3 Precision Considerations 549
13.2.4 Charge Injection Cancellation 553
13.3 Switched-Capacitor Amplifiers 555
13.3.1 Unity-Gain Sampler/Buffer 555
13.3.2 Noninverting Amplifier 562
13.3.3 Precision Multiply-by-Two Circuit 567
13.4 Switched-Capacitor Integrator 568
13.5 Switched-Capacitor Common-Mode Feedback 571

14 Nonlinearity and Mismatch **576**
14.1 Nonlinearity 576
14.1.1 General Considerations 576
14.1.2 Nonlinearity of Differential Circuits 579
14.1.3 Effect of Negative Feedback on Nonlinearity 581
14.1.4 Capacitor Nonlinearity 583
14.1.5 Nonlinearity in Sampling Circuits 584
14.1.6 Linearization Techniques 585
14.2 Mismatch 591
14.2.1 Effect of Mismatch 593
14.2.2 Offset Cancellation Techniques 598
14.2.3 Reduction of Noise by Offset Cancellation 602
14.2.4 Alternative Definition of CMRR 603

15 Layout and Packaging **607**
15.1 General Layout Considerations 607
15.1.1 Design Rules 608
15.1.2 Antenna Effect 610

15.2 Analog Layout Techniques 610
 15.2.1 Multifinger Transistors 611
 15.2.2 Symmetry 613
 15.2.3 Shallow Trench Isolation Issues 617
 15.2.4 Well Proximity Effects 618
 15.2.5 Reference Distribution 618
 15.2.6 Passive Devices 620
 15.2.7 Interconnects 627
 15.2.8 Pads and ESD Protection 631
15.3 Substrate Coupling 634
15.4 Packaging 638

CHAPTER 1 Introduction to Analog Design

1.1 ■ Why Analog?

We are surrounded by "digital" devices: digital cameras, digital TVs, digital communications (cell phones and WiFi), the Internet, etc. Why, then, are we still interested in analog circuits? Isn't analog design old and out of fashion? Will there even be jobs for analog designers ten years from now?

Interestingly, these questions have been raised about every five years over the past 50 years, but mostly by those who either did not understand analog design or did not want to deal with its challenges. In this section, we learn that analog design is still essential, relevant, and challenging and will remain so for decades to come.

1.1.1 Sensing and Processing Signals

Many electronic systems perform two principal functions: they sense (receive) a signal and subsequently process and extract information from it. Your cell phone receives a radio-frequency (RF) signal and, after processing it, provides voice or data information. Similarly, your digital camera senses the light intensity emitted from various parts of an object and processes the result to extract an image.

We know intuitively that the complex task of *processing* is preferably carried out in the digital domain. In fact, we may wonder whether we can directly digitize the signal and avoid *any* operations in the analog domain. Figure 1.1 shows an example where the RF signal received by the antenna is digitized by an analog-to-digital converter (ADC) and processed entirely in the digital domain. Would this scenario send analog and RF designers to the unemployment office?

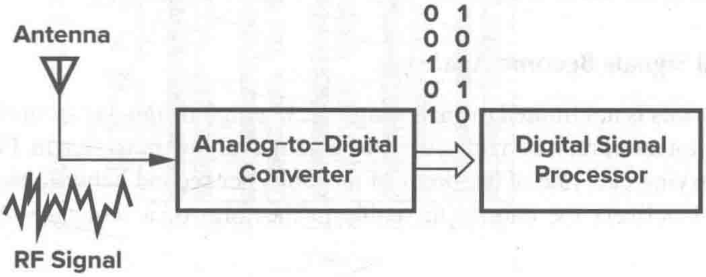

Figure 1.1 Hypothetical RF receiver with direct signal digitization.

The answer is an emphatic no. An ADC that could digitize the minuscule RF signal[1] would consume much more power than today's cell phone receivers. Furthermore, even if this approach were seriously considered, only *analog* designers would be able to develop the ADC. The key point offered by this example is that the sensing *interface* still demands high-performance analog design.

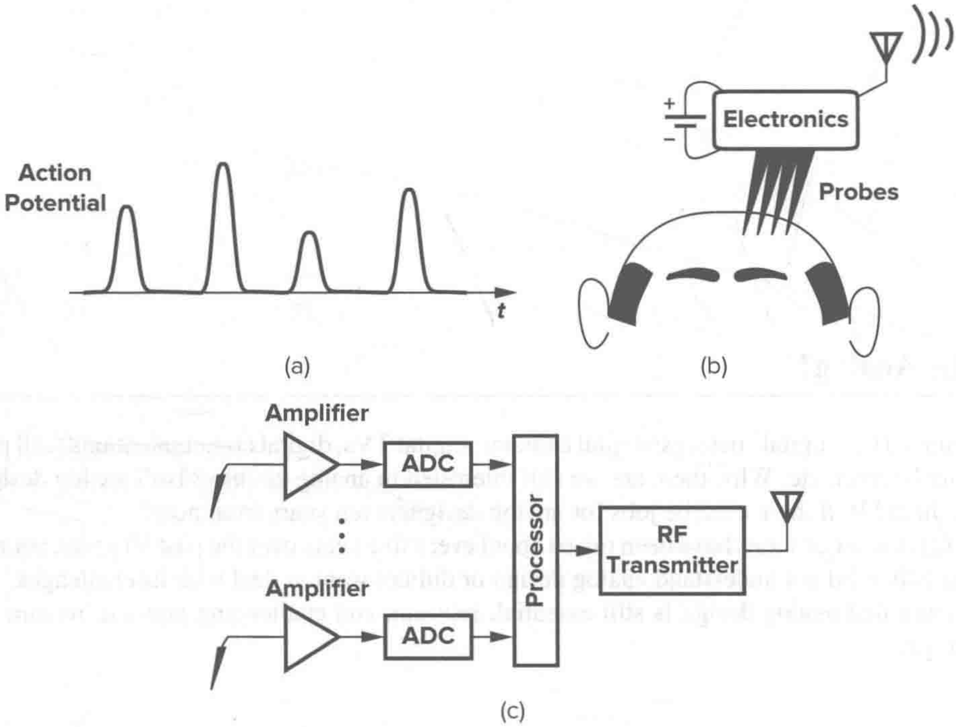

Figure 1.2 (a) Voltage waveform generated as a result of neural activity, (b) use of probes to measure action potentials, and (c) processing and transmission of signals.

Another interesting example of sensing challenges arises in the study of the brain signals. Each time a neuron in your brain "fires," it generates an electric pulse with a height of a few millivolts and a duration of a few hundred microseconds [Fig. 1.2(a)]. To monitor brain activities, a neural recording system may employ tens of "probes" (electrodes) [Fig. 1.2(b)], each sensing a series of pulses. The signal produced by each probe must now be amplified, digitized, and transmitted *wirelessly* so that the patient is free to move around [Fig. 1.2(c)]. The sensing, processing, and transmission electronics in this environment must consume a low amount of power for two reasons: (1) to permit the use of a small battery for days or weeks, and (2) to minimize the rise in the chip's temperature, which could otherwise damage the patient's tissue. Among the functions shown in Fig. 1.2(c), the amplifiers, the ADCs, and the RF transmitter—all analog circuits—consume most of the power.

1.1.2 When Digital Signals Become Analog

The use of analog circuits is not limited to analog signals. If a digital signal is so small and/or so distorted that a digital gate cannot interpret it correctly, then the analog designer must step in. For example, consider a long USB cable carrying data rate of hundreds of megabits per second between two laptops. As shown in Fig. 1.3, Laptop 1 delivers the data to the cable in the form of a sequence of ONEs and ZERO.

---

[1] And withstand large unwanted signals.

试读结束：需要全本请在线购买： www.ertongbook.com