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杨曾宪　张　凌　编译

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内 容 提 要

本书内容选自国外优秀教材和期刊杂志，主要包括模拟电子技术和数字电子技术基础理论，以及各种实用电路。编译者以国家教委颁发的“电子技术教学基本要求”为指导，根据多年教学经验与教育改革实践，精心选材，以中英对照方式编译成电子专业技术文集。

本书可作为电子专业英语阅读教材，也可作为电子技术基础或电子线路课程的辅助教材。对理工科大学生和工程技术人员学习专业英语和提高阅读能力是一本非常实用的读物。

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前　言

本书可作为电子专业英语阅读教材使用，亦可作为电子技术基础或电子线路课程的辅助教材使用，还可作为工程技术人员自学电子专业英语或电子专业英语晋级考试的课本。

本书是在教学改革中孕育而出的。改革开放后，社会主义市场经济的高速发展，电子学科日新月异的变化，电子学科与其他学科的交叉发展，使电子行业的各种国际交流更加频繁。电子专业师生及工程技术人员深感提高专业外语水平的必要性。为了适应社会需求，国家教委在1994年颁发的“普通高等学校理工科教育培养目标和毕业生的基本要求”中明确指出，“毕业生应基本掌握一门外语，能比较顺利地阅读本专业外文书刊。具有听、说、写的基础。”为了达到这一要求，在基础外语教学达到一定水平（4级左右）后，提高专业外语阅读能力，已成为广大师生的迫切愿望。但是目前外语专业阅读存在学时少、任务重的矛盾，教材也十分短缺。为了解决这些问题，在重点主干课程中贯穿外语专业阅读，是切实可行的有效方法。从1986年开始我们在电子技术基础课中贯穿外语专业阅读。教师从国外优秀教材及期刊杂志中选出与电子学课程内容有关的外语专业阅读资料作为辅助教材，学生以自学为主，边阅读外语资料，边复习本课程内容，可获取一举两得的效果。这项教学改革在院部级一类课程评比及华北地区教学研讨活动中，得到了专家及同行的肯定。为了使全国更多的大学生及有关工程技术人员受益，我们将阅读资料精选编译成系列丛书，正式出版，以加强电子专业外语阅读教材与电子学课程辅助教材的建设，促进电子专业师生及工程技术人员专业外语水平的提高。

本书在选材编排方面具有以下特点：

1. 以国家教委颁发的电子技术教学基本要求的内容为主线，由浅入深，循序渐进，以便与课堂教学内容相结合。

2. 介绍了大量集成实用电路，既与课程内容结合，又注意了内容的先进性、实用性和趣味性，如9～15篇、23篇等。

3. 本书可分为三个阅读阶段：1～7，8～15，16～23，每阶段后有1～2篇提高篇，共4篇文章（7、10、15、23）可作为国际学术交流论文的范例，使读者通过阅读，体会到在国际学术交流中如何写论文。

4. 采用英文、中文对照方式编辑，便于读者自学电子专业英语。

5. 本书中文部分，亦可作为电子技术基础或电子线路课程的参考书。

参加本书编译工作的有张凌同志（1～6，11-1、13、16～12）杨曾宪同志（7～12，14、15、23、24）。杨曾宪同志负责全书的组织及定稿。

本书由北京邮电大学谢沅清教授主审。

在教学改革及本书的编译过程中，得到了华北电力学院各级领导及同行的支持与关怀，得到了清华大学、东南大学、北京邮电大学、北京航天航空大学、西安交通大学、天津大学、太原工业大学、中国人民解放军军械工程学院等兄弟院校同行的支持与帮助，在此一并致谢。

CONTENTS
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1 FULL-WAVE RECTIFICATION

Two types of full-wave rectifier circuits are shown in Figs. 1-1 and 1-2. The circuit in Fig. 1-1 uses only two diodes, but its power must be supplied from a transformer with a center-tapped secondary winding. When the transformer output voltage is positive at the top, as shown in the figure, D_1 is forward biased and D_2 is reverse biased. During the negative half-cycle of transformer output, D_2 is forward biased and D_1 is reverse biased. The result is a load waveform composed of continuous positive half-cycles of the diode input waveform, i. e., full-wave rectification.

Because center-tapped transformers are usually more expensive and require much more space than additional diodes, the bridge rectifier shown in Fig. 1-2 is the circuit most frequently used for full-wave rectification.

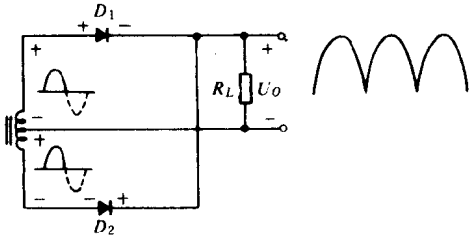

Fig. 1-1 Full-wave rectifier circuit using two diodes and a center-tapped transformer.

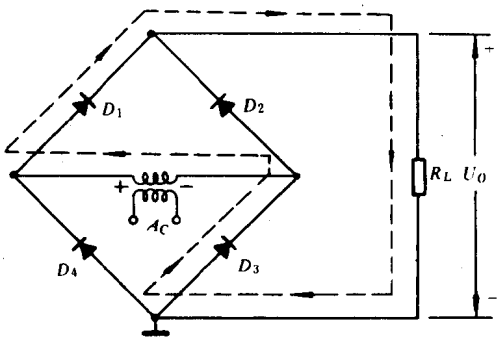

Fig. 1-2 Full-wave bridge circuit.

To understand the action of this circuit, it is necessary only to note that two diodes conduct simultaneously. For example, during the portion of the cycle when the transformer polarity is that indicated in Fig. 1-2, diodes D_1 and D_3 are conducting, and current passes from the positive to the negative end of the load. The conduction path is shown in the figure. During the next half cycle, the transformer voltage reverses its polarity, and diodes D_2 and D_4 send current through the load in the same direction as during the previous half cycle.

The principal features of the bridge circuit are the following: The currents drawn in both the primary and the secondary of the supply transformer are sinusoidal, and therefore a smaller transformer may be used than for the full-wave circuit of the same output; a transformer without a center tap is used; and each diode has only transformer voltage across it on the inverse cycle. The bridge circuit is thus suitable for high-voltage applications.

2 COMMON EMITTER CIRCUIT

2.1 Principles of Common Emitter Circuit

An npn transistor is shown in Fig. 2-1 with a load resistor (R_L=10kΩ) in series with the collector terminal. A collector supply voltage (V_{CC}=20V) is provided with a polarity that reverse biases the collector-base junction. A base current I_B is also provided via R_B, and this results in a forward bias (V_{BE}) at the base-emitter junction.

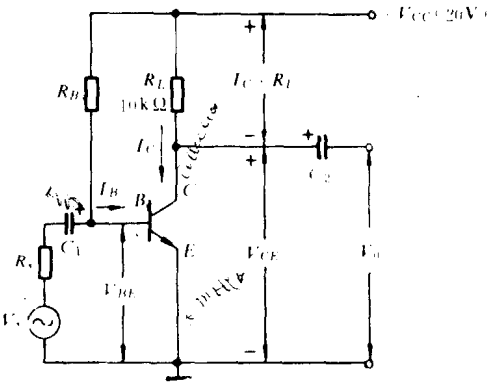

Fig. 2-1 Common emitter circuit.

A signal voltage V_s having a source resistance R_s is capacitor coupled via C_1 to the transistor base. The output is derived via another capacitor C_2 connected to the transistor collector. Both capacitors are open circuit to direct currents, but offer a very low impedance to AC signals. If the signal source were direct connected instead of capacitor coupled, there would be a low resistance path from the base to the negative supply line, and this would affect the circuit bias conditions. Similarly, an external load directly connected to the transistor collector might alter the collector voltage.

Assume that R_B is selected to give a base current of I_B=20 μA. Also, let the DC current gain factor of the transistor be β=50. Then

$$I_C \approx \beta I_B$$
$$= 50 \times 20 \times 10^{-6} = 1 \text{ mA}$$

The voltage drop across R_L is $I_C R_L$=1 mA×10kΩ=10V, and the collector to emitter voltage V_{CE} is V_{CC}− ($I_C R_L$) =20V−10V=10V.

The circuit dc conditions have been established as I_B=20 μA, I_C=1 mA, V_{CE}=10V, V_{CC} =20V,

If V_{BE} is increased until I_B=25 μA,

$$I_C \approx \beta I_B$$
$$= 50 \times 25 \times 10^{-6} = 1.25\text{mA}$$

The voltage drop across R_L is $I_C R_L$=1.25mA×10kΩ=12.5V, and V_{CE}=V_{CC}−$I_C R_L$= 20V−12.5V=7.5V.

When I_B is 20 μA, V_{CE}=10V, and when I_B is 25 μA, V_{CE}=7.5V.

Hence, for an increase in I_B of 5 μA, V_{CE} decreases by 2.5V (i.e., V_{CE} changed by the

same amount as the voltage change across R_L).

Similarly, if V_{BE} is decreased until I_B is 15 μA, I_C becomes $=50\times15\times10^{-6}=0.75$ mA and $I_C R_L=0.75$ mA$\times$10 k$\Omega=7.5$ V. Thus, $V_{CE}=20\text{V}-7.5\text{V}=12.5\text{V}$. Therefore, for a 5-$\mu$A decrease in I_B, V_{CE} increases by 2.5V.

The variation in base-emitter voltage could be produced by the AC signal V_s. This might require a signal amplitude of perhaps $\pm$10mV. If $V_s=\pm10$mV produces $V_o=\pm2.5$V, the signal may be said to be amplified by a factor of

$$V_o/V_s=2.5\text{V}/10\text{mV}=250$$

or circuit amplification$=250$.

The transistor current and voltage variations have no effect on the supply voltage (V_{CC}). So, when assessing the AC performance of the circuit, V_{CC} can be treated as a short circuit. The coupling capacitor C_1 also becomes a short circuit to AC signals. Redrawing the circuit of Fig. 2-1 with V_{CC} and C_1 shorted gives the AC equivalent circuit shown in Fig. 2-2.

In Fig. 2-2 the circuit input terminals are the base and the emitter, and the output terminals are the collector and the emitter. Thus, the emitter is common to both input and output, and the circuit is designated common emitter, or sometimes grounded emitter. It is also seen from the figure that resistors R_B and R_L are in parallel with the circuit input and output terminals, respectively.

2.2 Common Emitter h-Parameter Analysis

The h-parameter equivalent of the common emitter circuit in Fig. 2-1 is shown in Fig. 2-3. Figure 2-3 is drawn simply by replacing the transistor in the common emitter AC equivalent circuit (Fig. 2-2) with its h-parameter equivalent circuit. When an external emitter resistance (R_E) is included in the circuit, as shown in Fig. 2-4 (a), the h-parameter equivalent circuit becomes that of Fig. 2-4 (b).

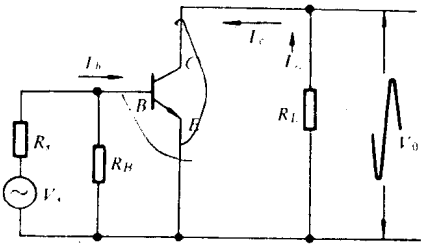

Fig. 2-2 Common emitter AC equivalent circuit.

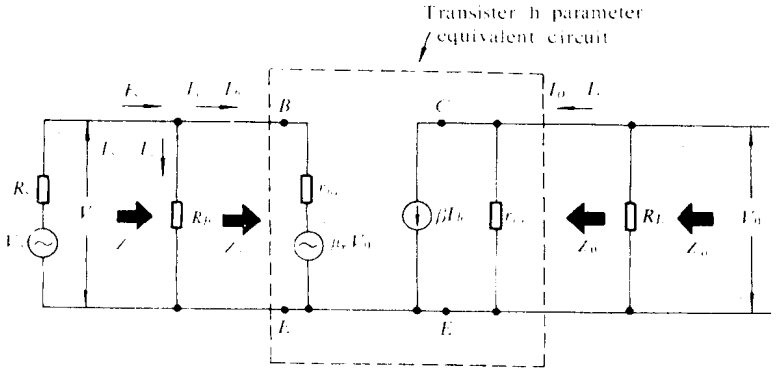

Fig. 2-3 Common emitter h-parameter equivalent circuit.

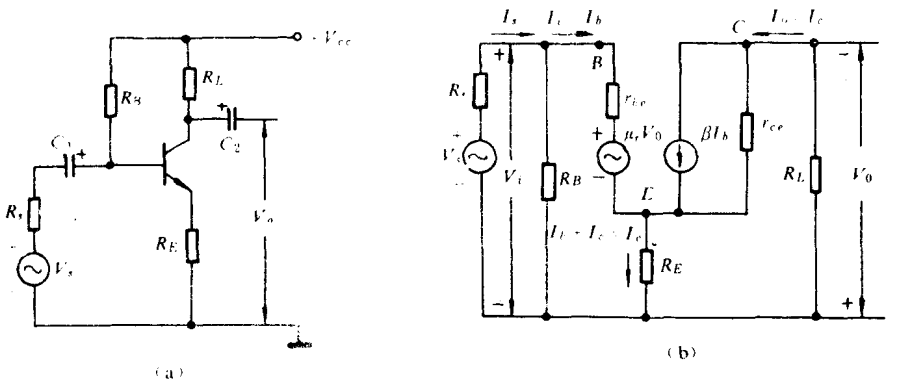

Fig. 2-4 CE circuit with emitter resistance and h-parameter equivalent circuit.

(a) CE circuit with emitter resistance (b) h-parameter equivalent circuit for CE circuit with R_E

The current directions and voltage polarities shown in Figs. 2-3 and 2-4 (b) are those that occur when the input signal goes positive. The h-parameter circuits could be analyzed rigorously to obtain exact expressions for voltage and current gains as well as input and output impedances. However, with a knowledge of the circuit operation and of typical h-parameter values, approximations may be made to quickly produce useful and reasonably accurate expressions for calculations of circuit performance.

2.3 Input Impedance

Looking into the device base and emitter terminals (Fig. 2-3), r_{be} is seen in series with $\mu_r V_o$. For a CE circuit μ_r is normally a very small quantity, so that the voltage fedback ($\mu_r V_o$) from the output to the input circuit is much smaller than the voltage drop across r_{be}. Thus,

$$Z_i \approx r_{be} \tag{2-1}$$

A typical value of r_{be} is 1.5kΩ.

When an external emitter resistance is connected in the circuit (Fig. 2-4), the calculation of Z_i becomes a little more complicated.

$$\begin{aligned} V_i &= I_b r_{be} + I_e R_E \qquad \text{(again ignoring } \mu_r V_o\text{)} \\ &= I_b r_{be} + R_E\ (I_b + I_e) \\ &= I_b r_{be} + R_E I_b + R_E \beta I_b \\ &= I_b\ [r_{be} + R_E\ (1+\beta)] \end{aligned}$$

and

$$Z_i = \frac{V_i}{I_i} = \frac{V_i}{I_b}$$

Therefore,

$$Z_i = r_{be} + R_E\ (1+\beta) \tag{2-2}$$

An examination of Eq. (2-2) shows that it is possible to look at a CE circuit with an external emitter resistance and very quickly estimate its input impedance. For example, in Fig.

2-4 (a), if $R_E=1\ \text{k}\Omega$, $r_{be}=1.5\ \text{k}\Omega$, and $\beta=50$, Z_i is calculated as $52.5\ \text{k}\Omega$.

Equations (2-1) and (2-2) give the input impedance to the device base. The actual circuit input impedance is R_B in parallel with Z_i [see Figs. 2-3 and 2-4 (b)]. Therefore,

$$Z'_i=R_B/\!/Z_i \tag{2-3}$$

2.4 Output Impedance

Since output voltage variations have little effect upon the input of a CE circuit, only the output half of the circuit need be considered in determining the output impedance. Looking into the collector and emitter terminals, a large resistance (r_{ce}) is seen. Thus,

$$Z_o\approx r_{ce} \tag{2-4}$$

Z_o is the device output impedance. The actual circuit output impedance is Z_o in parallel with R_L.

$$Z'_o=r_{ce}/\!/R_L \tag{2-5}$$

Since r_{ce} is typically 1 MΩ and R_L is usually very much less than 1 MΩ, the circuit output impedance is approximately R_L. Using this information it is possible to tell the approximate output impedance of a CE circuit just by looking at it. If R_L in Figs. 2-3 and 2-4 is 10 kΩ, then the circuit output impedance is approximately 10 kΩ.

2.5 Voltage Gain

$$\text{Voltage gain}=A_v=V_o/V_i$$

From Fig. 2-3, $V_o=I_c R_L$ and $V_i=I_b r_{be}$. Therefore,

$$A_v=\frac{I_c R_L}{I_b r_{be}}=\frac{I_c}{I_b}\times\frac{R_L}{r_{be}}=\frac{-\beta R_L}{r_{be}} \tag{2-6}$$

The minus sign indicates that V_o is 180° out of phase with V_i (When V_i increases, V_o decreases, and vice versa.). Knowing the appropriate h- parameters and R_L, the voltage gain of a CE circuit can be quickly estimated. Using typical values such as $R_L=10\ \text{k}\Omega$, $\beta=50$, and $r_{be}=1.5\text{k}\Omega$, a typical CE voltage gain is −330.

With an external emitter resistance (R_E) in the circuit,

$$\begin{aligned}V_i&=I_b r_{be}+I_c R_E\\&=I_b r_{be}+R_E\ (I_b+I_c)\\&=I_b r_{be}+R_E I_b\ (1+\beta)\\&=I_b\ [r_{be}+R_E\ (1+\beta)]\end{aligned}$$

and

$$A_v=\frac{V_o}{V_i}=\frac{I_c R_L}{I_b\ [r_{be}+R_E\ (1+\beta)]}=\frac{-\beta R_L}{r_{be}+R_E\ (1+\beta)} \tag{2-7}$$

Usually $R_E\ (1+\beta)\gg r_{be}$, so that

$$A_v\approx -R_L/R_E$$

Using this expression, the voltage gain of a CE circuit with an external emitter resistance can easily be estimated. If in Fig. 2-4 $R_L=10\ \text{k}\Omega$ and $R_E=1\ \text{k}\Omega$, the circuit voltage gain is ap-

3 CLASS B AMPLIFIERS

3.1 Principles

A class B amplifier is one in which the operating point is at an extreme end of its characteristic, so that the quiescent power is very small. Hence either the quiescent current or the quiescent voltage is approximately zero. If the signal excitation is sinusoidal, amplification takes place for only one half of a cycle. For example, if the quiescent output circuit current is zero, this current will remain zero for one half of a cycle.

If $V_{BB}=0$ in Fig. 3-1, the quiescent current is $I_C=0$. From the definitions given above, this zero-bias circuit is a class B amplifier. Similarly, the emitter follower in Fig. 3-2 (a) operates in class B. Let us assume that the transistor output characteristics are equally spaced for equal intervals of excitation. For such an idealized transistor the dynamic transfer curve (i_C versus i_B) is a straight line passing through the origin (Fig. 3-2 (b)). The graphical construction from which to determine the collector-current waveshape is indicated. Note that for this class B circuit the load current $i_L \approx i_C$ is sinusoidal during one half of each period and is zero during the second half cycle. In other words, this circuit behaves as a rectifier rather than as a power amplifier.

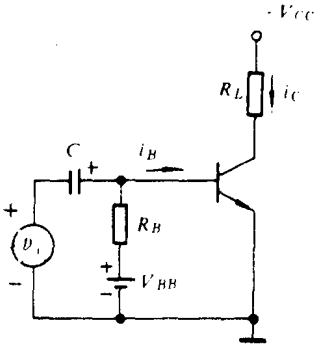

Fig. 3-1 The circuit of a simple transistor amplifier.

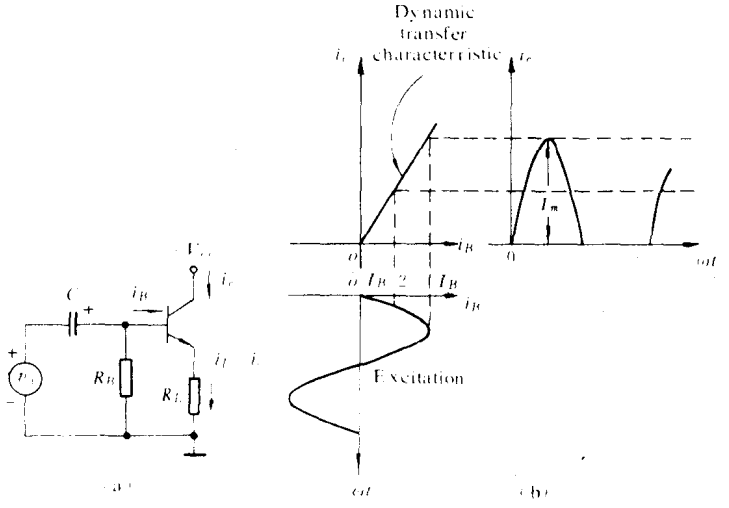

Fig. 3-2 (a) An emitter follower with zero bias operating as a class B amplifier
(b) Graphical construction for determining the output current waveform

The foregoing difficulty is overcome by using the complementary emitter-follower OP AMP output stage, which is repeated in Fig. 3-3 for convenience. This configuration is called a class B push-pull amplifier. For positive values of the sinusoidal input v_i, T_1 conducts and T_2 is OFF ($i_2=0$), so that i_1 is the positive half sinewave of Fig. 3-2 (b). For negative values of v_i, T_1 is nonconducting ($i_1=0$), and T_2 conducts, resulting in a positive half sinusoid for i_2, which is 180° out of phase with that shown in Fig. 3-2 (b). Since the load current is the difference between the two transistor emitter currents,

$$i_L=i_1-i_2 \tag{3-1}$$

Consequently, for the idealized transfer characteristic of Fig. 3-2 (b), the load current is a perfect sinusoid.

The advantages of class B as compared with class A operation are the following: It is possible to obtain greater power output, the efficiency is higher, and there is negligible power loss at no signal. For these reasons, in systems where the power supply is limited, such as those operating from solar cells or a battery, the output power is usually delivered through a push-pull class B transistor circuit. The disadvantages are that the harmonic distortion may be higher and the supply voltages must have good regulation. The power output circuit in most modern IC amplifiers is the complementary emitter-follower push-pull stage.

3.2 Efficiency

In Fig. 3-3 the peak load voltage is $V_m=I_m R_L$. The power output is

$$P=\frac{I_m V_m}{2} \tag{3-2}$$

The corresponding direct collector current in each transistor under load is the average value of the half sine loop of Fig. 3-2 (b). Since $I_{dc}=I_m/\pi$ for this waveform, the dc input power from the supply is

$$P_i=2\frac{I_m V_{CC}}{\pi} \tag{3-3}$$

The factor 2 in this expression arises because two transistors are used in the push-pull system.

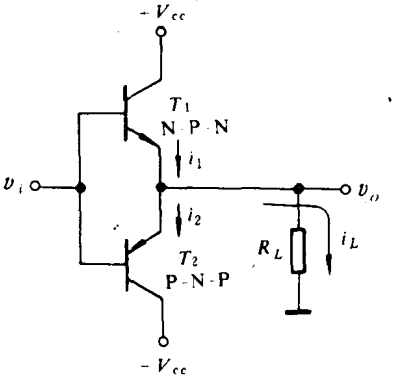

Fig. 3-3 A class B push-pull amplifier.

Taking the ratio of Eqs. (3-2) and (3-3), we obtain for the collector circuit-efficiency

$$\eta\equiv\frac{P}{P_i}\times 100=\frac{\pi}{4}\frac{V_m}{V_{CC}}\times 100 \text{ percent} \tag{3-4}$$

If the drop across a transistor is negligible compared with the supply voltage, then $V_m\approx V_{CC}$. Under these conditions, Eq. (3-4) shows that the maximum possible conversion efficiency is $25\pi=78.5$ percent for a class B system compared with 50 percent for class A operation. This large value of η results from the fact that there is no current in a class B system if there is no excitation, whereas there is a drain from the power supply in a class A system

even at zero signal. We also note that in a class B amplifier the dissipation at the collectors is zero in the quiescent state and increases with excitation, whereas the heating of the collectors of a class A system is a maximum at zero input and decreases as the signal increases. Since the direct current increases with signal in a class B amplifier, the power supply must have good regulation.

3.3 Dissipation

The dissipation P_C (in both transistors) is the difference between the power input to the collector circuit and the power delivered to the load. Since $I_m=V_m/R_L$,

$$P_C=P_i-P=\frac{2}{\pi}\frac{V_{CC}V_m}{R_L}-\frac{V_m^2}{2R_L} \tag{3-5}$$

This equation shows that the collector dissipation is zero at no signal ($V_m=0$), rises as V_m increases, and passes through a maximum at $V_m=2V_{CC}/\pi$. The peak dissipation is found to be

$$P_{C(\max)}=\frac{2V_{CC}^2}{\pi^2R_L} \tag{3-6}$$

The maximum power which can be delivered is obtained for $V_m=V_{CC}$ or

$$P_{\max}=\frac{V_{CC}^2}{2R_L} \tag{3-7}$$

Hence

$$P_{C(\max)}=\frac{4}{\pi^2}P_{\max}\approx 0.4P_{\max} \tag{3-8}$$

If, for example, we wish to deliver 10W from a class B push-pull amplifier, then $P_{C(\max)}=4$W, or we must select transistors which have collector dissipations of approximately 2W each. In other words, we can obtain a push-pull output of five times the specified power dissipation of a single transistor. On the other hand, if we paralleled two transistors and operated them class A to obtain 10W out, the collector dissipation of each transistor would have to be at least 10W (assuming 50 percent efficiency). This statement follows from the fact that $P_i=P/\eta=10/0.5=20$W. This input power must all be dissipated in the two collectors at no signal, or $P_C=10$W per transistor. Hence at no excitation there would be a steady loss of 10W in each transistor, whereas in class B the standby (no-signal) dissipation is zero. This example clearly indicates the superiority of the push-pull over the parallel configuration.

4 THE DIFFERENTIAL AMPLIFIERS

4.1 Symmetrical Emitter-coupled Difference Amplifier

The circuit of Fig. 4-1 is an excellent DIFF AMP if the emitter resistance R_e is large. This statement can be justified as follows: If $V_{S1}=V_{S2}=V_S$, then we have $V_d=V_{S1}-V_{S2}=0$ and $V_o=A_C V_S$. However, if $R_e=\infty$, then, because of the symmetry of Fig. 4-1, we obtain $I_{e1}=I_{e2}=0$. Since $I_{b2}\ll I_{c2}$, then $I_{c2}\approx I_{e2}$, and it follows that $V_o=0$. Hence the common-mode gain A_c becomes zero, and the common-mode rejection ratio is infinite for $R_e=\infty$ and a symmetrical circuit.

We now analyze the emitter-coupled circuit for a finite value of R_e. A_c can be evaluated by setting $V_{S1}=V_{S2}=V_S$ and making use of the symmetry of Fig. 4-1. This circuit can be bisected as in Fig. 4-2 (a). Using the approximate h-parameter model, the value of A_c is given by

$$A_c=\frac{-\beta R_c}{R_s+r_{be}+(1+\beta)\,2R_e} \tag{4-1}$$

Similarly, the difference mode gain A_d can be obtained by setting $V_{S1}=-V_{S2}=V_S/2$. From the symmetry of Fig. 4-1 we see that, if $V_{S1}=-V_{S2}$, then the emitter of each transistor is grounded for small-signal operation. Under these conditions the circuit of Fig. 4-2 (b) can be used to obtain A_d. Hence

$$A_d=\frac{V_o}{V_S}=\frac{1}{2}\,\frac{\beta R_c}{R_S+r_{be}} \tag{4-2}$$

provided $\frac{1}{r_{ce}}R_e\ll 1$.

From Eqs. (4-1) and (4-2) it is seen that the CMRR$=A_d/A_c$ increases without limit as $R_e\to\infty$, as predicted above. There are, however, practical limitations on the magnitude of R_e because of the quiescent dc voltage drop across it; the emitter supply V_{EE} must become larger as R_e is increased, in order to maintain the quiescent current at its proper value. If the operating currents of the transistors are allowed to decrease, this will lead to higher r_{be} values and lower values of β. Both of these effects will tend to decrease the common-mode rejection ratio.

4.2 Differential Amplifier Supplied with a Constant Current

Frequently, in practice, R_e is replaced by a transistor circuit, as in Fig. 4-3, in which R_1, R_2, and R_3 can be adjusted to give the same quiescent conditions for T_1 and T_2 as the original circuit of Fig. 4-1. This modified circuit of Fig. 4-5 presents a very high effective emitter re-

sistance R_e for the two transistors T_1 and T_2. Since R_e is also the effective resistance looking into the collector of transistor T_3, R_e is hundreds of kilo-ohms even if R_3 is as small as 1 k.

We now verify that transistor T_3 acts as an approximately constant current source, subject to the condition that the base current of T_3 is negligible. Applying KVL to the base circuit of T_3, we have

$$I_3 R_3 + V_{BE3} = V_D + (V_{EE} - V_D) \frac{R_2}{R_1 + R_2} \quad (4\text{-}3)$$

where V_D is the diode voltage. Hence

$$I_o \approx I_3 = \frac{1}{R_3}\left(\frac{V_{EE} R_2}{R_1 + R_2} + \frac{V_D R_1}{R_1 + R_2} - V_{BE3} \right) \quad (4\text{-}4)$$

If the circuit parameters are chosen so that

$$\frac{V_D R_1}{R_1 + R_2} = V_{BE3} \quad (4\text{-}5)$$

then

$$I_o = \frac{V_{EE} R_2}{R_3 (R_1 + R_2)} \quad (4\text{-}6)$$

Since this current is independent of the signal voltages V_{s1} and V_{s2}, then T_3 acts to supply the DIFF AMP consisting of T_1 and T_2 with the constant current I_o.

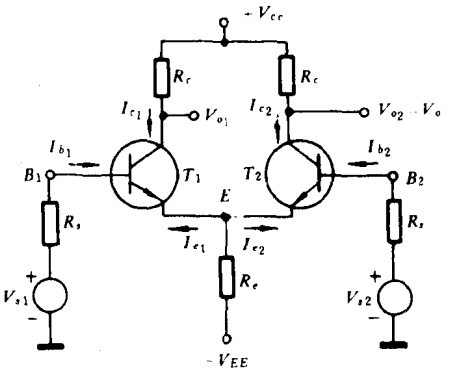

Fig. 4-1 Symmetrical emitter coupled difference amplifier.

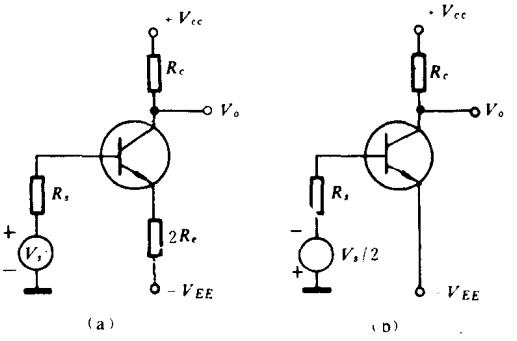

Fig. 4-2 Equivalent circuit for a symmetrical differential amplifier used to determine.
(a) the common-mode gain A_c and
(b) the difference gain A_d

The above result for I_o has been rendered independent of temperature because of the added diode D. Without D the current would vary with temperature because V_{BE3} decreases approximately 2.5 mV/°C. The diode has this same temperature dependence, and hence the two variations cancel each other and I_o does not vary appreciably with temperature. Since the cutin voltage V_D of a diode has approximately the same value as the base to-emitter voltage V_{BE3} of a transistor, then Eq. (4-5) cannot be satisfied with a single diode. Hence two diodes in series are used for V_D.

Consider that T_1 and T_2 are identical and that T_3 is a true constant current source. Under these circumstances we can demonstrate that the common-mode gain is zero. Assume that $V_{s1} = V_{s2} = V_s$, so that from the symmetry of the circuit, the collector current I_{c1} (the increase over the quiescent value for $V_s = 0$) in T_1 equals the current I_{c2} in T_2. However, since the total current increase $I_{c1} + I_{c2} = 0$ if I_o = constant, then $I_{c1} = I_{c2} = 0$ and $A_c = V_{o2}/V_s = -I_{c2} R_c/V_s = 0$.

4.3 Practical Considerations

In some applications the choice of V_{s1} and V_{s2} as the input voltages is not realistic because

the resistances R_{s1} and R_{s2} represent the output impedances of the voltage generators V_{s1} and V_{s2}. In such a case we use as input voltages the base-to-ground voltages V_{b1} and V_{b2} of T_1 and T_2, respectively.

The differential amplifier is often used in dc applications. It is difficult to design dc amplifiers using transistors because of drift due to variations of β, V_{BE}, and I_{CBO} with temperature. A shift in any of these quantities changes the output voltage and cannot be distinguished from a change in input-signal voltage. Using the techniques of integrated circuits, it is possible to construct a DIFF AMP with T_1 and T_2 having almost identical characteristics. Under these conditions any parameter changes due to temperature will cancel and the output will not vary.

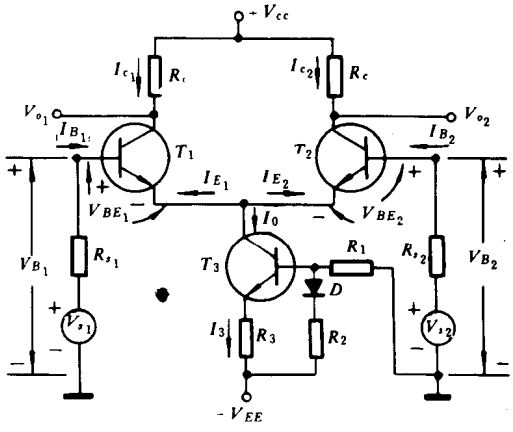

Fig. 4-3 Differential amplifier with constant-current stage in the emitter circuit. Nominally, $R_{S1}=R_{S2}$.

Differential amplifiers may be cascaded to obtain larger amplifications for the difference signal. Outputs V_{o1} and V_{o2} are taken from each collector (Fig. 4-3) and are coupled directly to the two bases, respectively, of the next stage.

Finally, the differential amplifier may be used as an emitter-coupled phase inverter. For this application the signal is applied to one base, whereas the second base is not excited (but is, of course, properly biased). The output voltages taken from the collectors are equal in magnitude and 180° out of phase.