世界微处理器与微控制器 第二卷

WORLD MICROPROCESSOR & MICROCONTROLLER Volume Ⅱ

——电路数据手册

電子工業出版社

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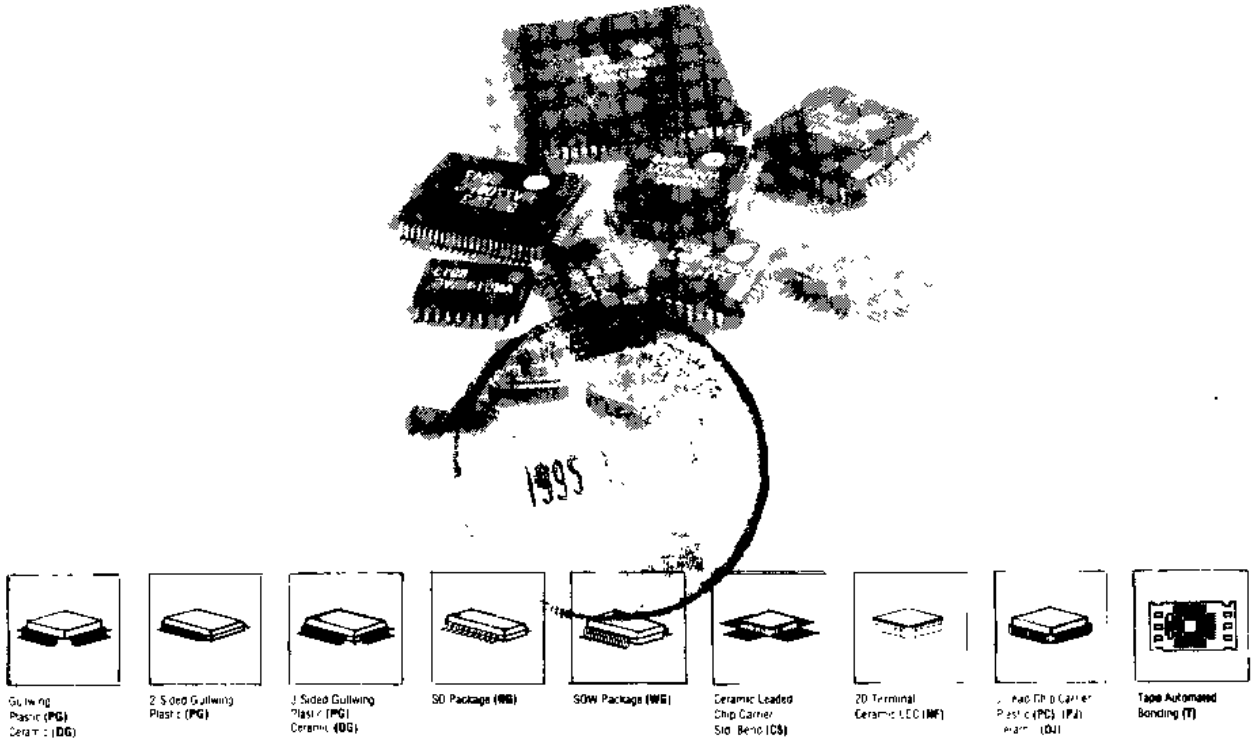

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内 容 提 要

本书收集了 INTEL、MOTORALA、AMD、NSC、FUJITSU、HARRIS、OKI、NEC、MITSUBISHI 等世界知名厂商生产的十六位微处理器及部分微控制器，资料均取材于各厂商的 OEM 手册，数据翔实准确，资料新颖全面，并直接采用原文，避免因翻译而引起的失真。为了便于读者快速阅读和浏览，在每章的开头，都有一个简单的中文简介，言简意赅地描述了本章所介绍的微处理器或控制器的主要特性。

本书可供科研院所的科研人员，大专院校师生在科研学习过程中作为参考书使用，也可供系统维护及维修人员，硬件营销人员参考。

世界微处理器与微控制器
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十六位机
奥森选编
责任编辑　韩瑞宗

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编 者 的 话

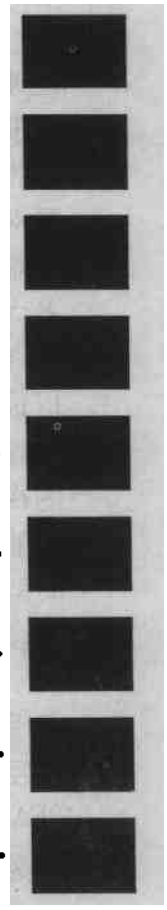
随着计算机产业的蓬勃发展，作为计算机心脏的微处理器的应用越来越广泛，从家用电器到航空航天事业，无处不用到微处理器和微控制器。而国内的科研人员面对浩若繁星的国外各厂商的微处理器与微控制器，常有茫然不知所措的感觉。有鉴于此，为了帮助国内科研人员对世界各大厂商生产的微处理器与微控制器有一个全面的了解，北京瑞特电子技术公司集多年器件、信息资料服务之经验，凭借与国外各大厂商之密切关系，搜集国外最新资料，与电子工业出版社通力合作，编纂而成这套《电路数据手册》，以奉献给国内读者。本书编排思想以最新、最全、最实用为主旨，紧跟国际潮流，适应国内需求，力求能解决读者在工作中遇到的实际问题，在选型上力求全而新，以扩大读者的视野，在此基础上，侧重国内外流行的微处理器与微控制器，并注重当前流行的"绿色浪潮"，较多地选用了一些低功耗，高集成度，小型化的型号，另外，根据国内客观环境和市场调研，本书也注意选用一些军用、工业用抗恶劣环境的高性能微处理器与微控制器。

另外，在此书成书之前，我们作了大量的调查研究工作，广泛听取了用户和科研人员的意见和建议，吸取了国内其他单位编写同类书刊的经验，根据此书读者的知识结构和外语水平，在内容上大胆采用OEM手册中的原文，以避免因翻译而引起失真和笔误。这样作会给部分读者造成阅读上的困难，在此深表抱歉。

因时间仓促，且编者能力有限，本书必有不少不尽人意之处，望各界同仁给我们提出宝贵意见和建议，以期我们进一步改进。

编　　者

公司索引



型号索引

第一章
先进微器件公司(AMD)

本书主要介绍了 AMD 公司生产的 8086/8088 微处理器，此处理器与 Intel 8086/8088 完全兼容，采用分段内存寻址，最大可寻址 1Mb 内存，64K I/O 端口。有灵活的寻址方式和丰富的指令集，有 256 个中断矢量，还支持 HOLD/HLDA 协议用以组成多主系统，既可以单片以最小方式运行也可以多片组成最大方式运行。其中 8086 外部数据总线是 16 位，8088 外部数据总线是 8 位。

8086/8088 组成整机产品现已被淘汰，但因其功能强大，价格低廉，兼容性好，尤其是基于 8086/8088 的无以数计的软件资源，使得它们在其它方面仍有广泛的应用，如工业控制用 SKD—86 单板机，Intel 公司的 ISBC88/45 高速通信板，以及 PC/104 嵌入式模板等。

8086

16-Bit Microprocessor
iAPX86 Family
FINAL

DISTINCTIVE CHARACTERISTICS

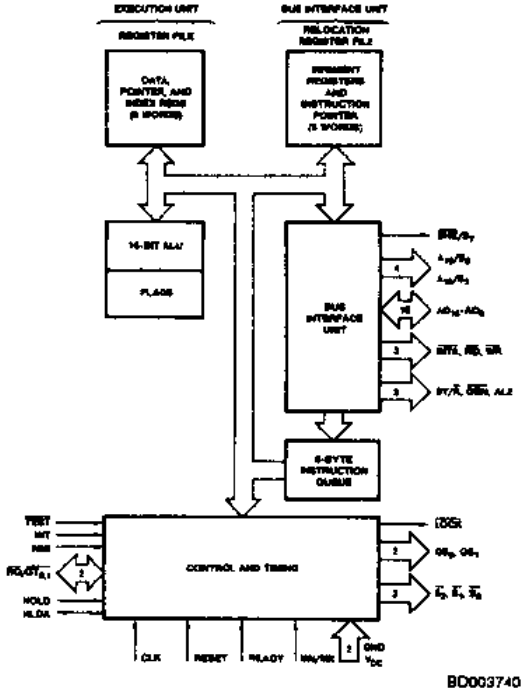
- Directly addresses up to 1 Mbyte of memory
- 24 operand addressing modes
- Efficient implementation of high level languages
- Instruction set compatible with 8080 software
- Bit, byte, word, and block operations
- 8 and 16-bit signed and unsigned arithmetic in binary or decimal
- MULTIBUS® system interface
- Three speed options
  - 5MHz for 8086
  - 8MHz for 8086-2
  - 10MHz for 8086-1

GENERAL DESCRIPTION

The 8086 is a general purpose 16-bit microprocessor CPU. Its architecture is built around thirteen 16-bit registers and nine 1-bit flags. The CPU operates on 16-bit address spaces and can directly address up to 1 megabyte using offset addresses within four distinct memory segments, designated as code, data, stack and extra code. The 8086 implements a powerful instruction set with 24 operand addressing modes. This instruction set is compatible with that of the 8080 and 8085. In addition, the 8086 is particularly effective in executing high level languages.

The 8086 can operate in minimum and maximum modes. Maximum mode offloads certain bus control functions to a peripheral device and allows the CPU to operate efficiently in a multi-processor system. The CPU and its high performance peripherals are MULTIBUS compatible. The 8086 is implemented in N-channel, depletion load, silicon gate technology and is contained in a 40-pin CERDIP package, Molded DIP package, or Plastic Leaded Chip Carrier.

BLOCK DIAGRAM



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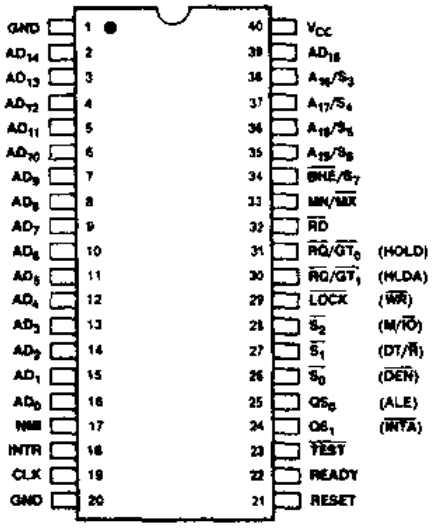
CONNECTION DIAGRAMS
Top View

DIP



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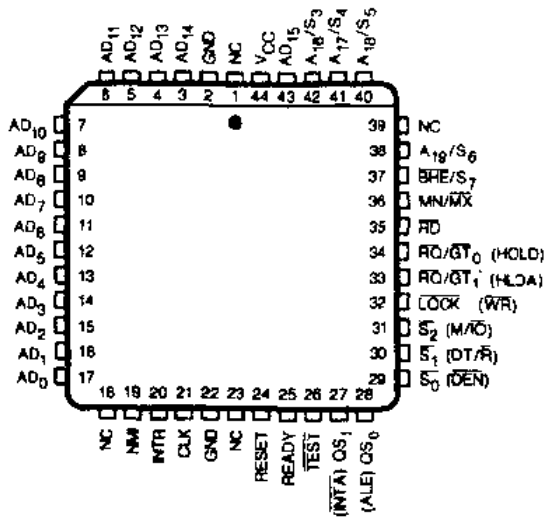

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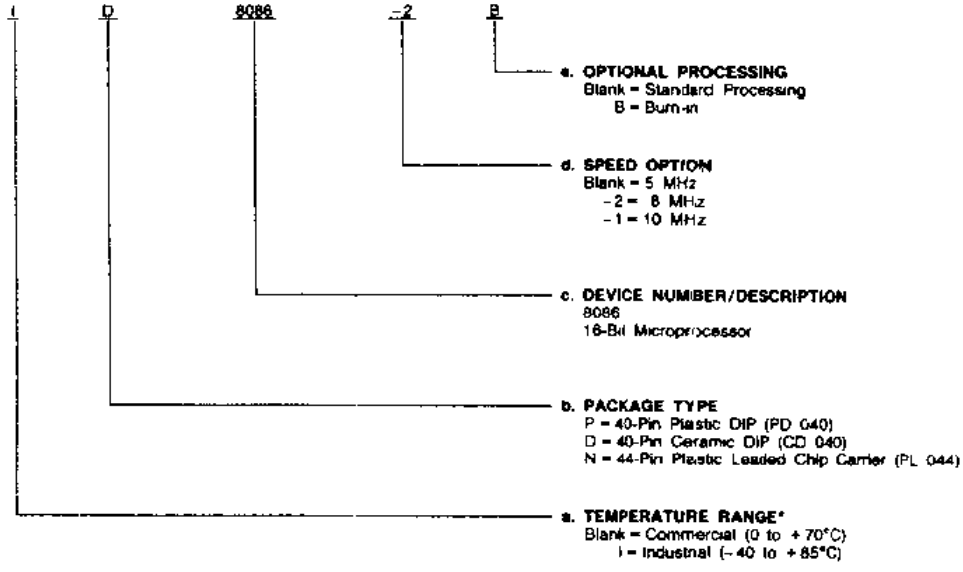
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Commercial Products

AMD commercial products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, D, N	8086
	8086-2
	8086-1
D, ID	8086-2B
D	8086-1
ID	8086B

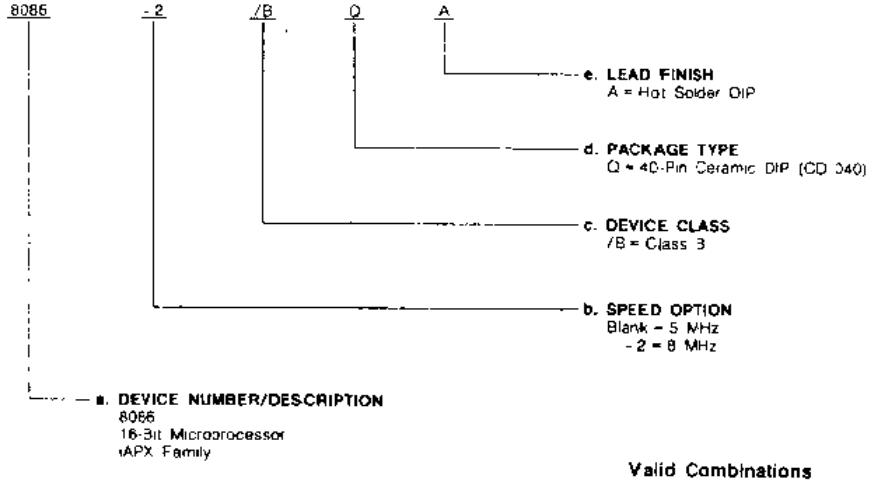
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

Military Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8086	/BQA
8086-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

Pin No.*	Name	I/O	Description
39, 2–16	AD_{15}–AD_0	I/O	Address Data Bus These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7–D_0 It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions (See $\overline{BHE}$) These lines are active HIGH and float to three-state OFF during interrupt acknowledge and local bus "hold acknowledge."
35–38	A_{19}/S_6 A_{18}/S_5 A_{17}/S_4 A_{16}/S_3	O	Address/Status During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle A_{17}/S_4 and A_{16}/S_3 are encoded as shown This information indicates which relocation register is presently being used for data accessing These lines float to three-state OFF during local bus "hold acknowledge" **A_{17}/S_4 | A_{16}/S_3 | Characteristics** 0 (LOW) | 0 | Alternate Data 0 | 1 | Stack 1 (HIGH) | 0 | Code or None 1 | 1 | Data S_6 is 0 (LOW) | |
34	$\overline{BHE}/S_7$	O	Bus High Enable/Status During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}–D_8 Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus The S_7 status information is available during T_2, T_3, and T_4 The signal is active LOW and floats to three-state OFF in "hold" It is LOW during T_1 for the first interrupt acknowledge cycle **$\overline{BHE}$ | A_0 | Characteristics** 0 | 0 | Whole word 0 | 1 | Upper byte from/ to odd address 1 | 0 | Lower byte from/ to even address 1 | 1 | None
32	$\overline{RD}$	O	Read Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the S_2 pin This signal is used to read devices which reside on the 8086 local bus $\overline{RD}$ is active LOW during T_2, T_3, and T_W of any read cycle and is guaranteed to remain HIGH in T_2 until the 8086 local bus has floated This signal floats to three-state OFF in "hold acknowledge"
22	READY	I	READY is the acknowledgment from the addressed memory or I/O device that it will complete the data transfer The READY signal from memory/IO is synchronized by the 8284A Clock Generator to form READY This signal is active HIGH The 8086 READY input is not synchronized Correct operation is not guaranteed if the set-up and hold times are not met.
18	INTR	I	Interrupt Request Is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation A subroutine is vectored to via an interrupt vector lookup table located in system memory It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized This signal is active HIGH
23	$\overline{TEST}$	I	$\overline{TEST}$ input is examined by the "Wait" instruction If the $\overline{TEST}$ input is LOW, execution continues, otherwise, the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
17	NMI	I	Non-Maskable Interrupt An edge-triggered input which causes a type 2 interrupt A subroutine is vectored to via an interrupt vector lookup table located in system memory NMI is not maskable internally by software A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction This input is internally synchronized
21	RESET	I	Reset Causes the processor to immediately terminate its present activity The signal must be active HIGH for at least four clock cycles It restarts execution, as described in the Instruction Set description, when RESET returns LOW RESET is internally synchronized
19	CLK	I	Clock Provides the basic timing for the processor and bus controller It is asymmetric with a 33% duty cycle to provide optimized internal timing
40	V_{CC}		V_{CC} The +5 V power supply pin
1, 20	GND		Ground The ground pin
33	$MN/\overline{MX}$	I	Minimum/Maximum Indicates what mode the processor is to operate in The two modes are discussed in the following sections

*Pin numbers correspond to DIPs only

PIN DESCRIPTION (continued)

Pin No.*	Name	I/O	Description
28-26	$\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$	O	Status Active during T_4, T_1, and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by S_2, S_1, or S_0 during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These signals float to three-state OFF in "hold acknowledge." These status lines are encoded as shown.

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

31, 30	$\overline{RQ}/GT_0$, $\overline{RQ}/GT_1$	I/O	Request/Grant. Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/GT_0$ having higher priority than $\overline{RQ}/GT_1$. $\overline{RQ}/GT$ has an internal pull-up resistor so it may be left unconnected. The request/grant sequence is as follows: 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 8086 (pulse 1). 2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the "hold" request is about to end and that the 8086 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met: 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made, two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
29	$\overline{LOCK}$	O	$\overline{LOCK}$ Output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to three-state OFF in "hold acknowledge."
24, 25	QS_1, QS_0	O	Queue Status. The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal 8086 instruction queue.
28	M/$\overline{IO}$	O	Status line. Logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, $\overline{IO}$ = LOW). M/$\overline{IO}$ floats to three-state OFF in local bus "hold acknowledge."
29	$\overline{WR}$	O	Write. Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW and floats to three-state OFF in local bus "hold acknowledge."
24	$\overline{INTA}$	O	$\overline{INTA}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3, and T_W of each interrupt acknowledge cycle.
25	ALE	O	Address Latch Enable. Provided by the processor to latch the address into 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
27	DT/$\overline{R}$	O	Data Transmit/Receive. Needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S}_1$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to three-state OFF in local bus "hold acknowledge."
26	$\overline{DEN}$	O	Data Enable. Provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T_2 until the middle of T_4, while for a write cycle, it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to three-state OFF in local bus "hold acknowledg

*Pin numbers correspond to DIPs only.

PIN DESCRIPTION (continued)

Pin No.*	Name	I/O	Description
31, 30	HOLD, HLDA	I/O	HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T_4 or T_1 clock cycle. Simultaneous with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer HLDA and when the processor needs to run another cycle, it will again drive the local bus and control lines. The same rules as for $\overline{RQ}/\overline{GT}$ apply, regarding when the local bus will be released. HOLD is not asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set-up time.

*Pin numbers correspond to DIPs only.

DETAILED DESCRIPTION

The 8086 CPU is internally organized into two processing units. These two units are the Bus Interface Unit (BIU) and the Execution Unit (EU). A block diagram of this organization is shown on page 1.

The BIU performs instruction fetch and queuing, operand fetch and store, address relocation, and basic bus control. The EU receives operands and instructions from the BIU and processes them on a 16-bit ALU. The EU accesses memory and peripheral devices through requests to the BIU. The BIU generates physical addresses in memory using the 4 segment registers and offset values.

The BIU and EU usually operate asynchronously. This permits the 8086 to overlap execution fetch and execution. Up to 6 instruction bytes can be queued. The instruction queue acts as a FIFO buffer for instructions, from which the EU extracts instruction bytes as required.

Memory Organization

The 8086 addresses up to 1 megabyte of memory. The address space is organized as a linear array, from 00000 to FFFFF in hexadecimal. Memory is subdivided into segments of 64K bytes each. There are 4 segments: code, stack, data, and extra (usually employed as an extra data segment). Each segment thus contains information of a similar type. Selection of a destination segment is automatically performed using the rules in the table below. This segmentation makes memory more easily relocatable and supports a more structured programming style.

Physical addresses in memory are generated by selecting the appropriate segment, obtaining the segment "base" address from the segment register, shifting the base address 4 digits to the left, and then adding this base to the "offset" address. For programming code, the offset address is obtained from the instruction pointer. For operands, the offset address is calculated in several ways, depending upon information contained in the addressing mode. Memory organization and address generation are shown in Figure 1a.

Certain memory locations are reserved for specific CPU operations. These are shown in Figure 1b. Addresses FFFF0H through FFFFFH are reserved for operations which include a jump to the initial program loading routine. After RESET, the CPU will always begin execution at location FFFF0H, where the jump must be located.

Addresses 00000H through 003FFH are reserved for interrupt operations. The service routine of each of the 256 possible interrupt types is signaled by a 4-byte pointer. The pointer elements must be stored in reserved memory addresses before the interrupts are invoked.

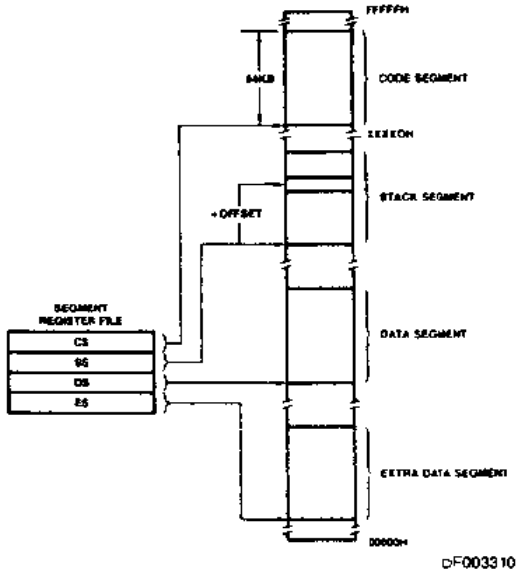


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Figure 1a. Memory Organization

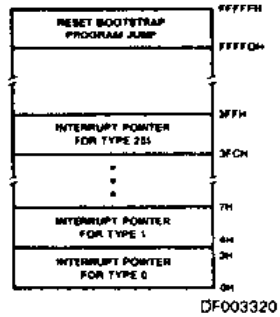

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Figure 1b. Reserved Memory Locations

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic for all prefetching of instructions
Stack	STACK (SS)	All stack pushes and pops and all memory references relative to BP base register except data references
Local Data	DATA (DS)	Data references which are relative to the stack, the destination of a string operation, or explicitly overridden
External (Global) Data	EXTRA (ES)	Destination of string operations, when they are explicitly selected using a segment override

Minimum and Maximum Modes

The 8086 has two system configurations, minimum and maximum mode. The CPU has a strap pin, MN/$\overline{MX}$, which defines the system configuration. The status of this strap pin defines the function of pin numbers 24 through 31.

When MN/$\overline{MX}$ is strapped to GND, the 8086 operates in maximum mode. The operations of pins 24 through 31 are redefined. In maximum mode, several bus timing and control functions are "off-loaded" to the 8288 bus controller, thus freeing up the CPU. The CPU communicates status information to the 8288 through pins S_0, S_1, and S_2. In maximum mode, the 8086 can operate in a multiprocessor system, using the LOCK signal within a Multibus format.

When MN/$\overline{MX}$ is strapped to V_{CC}, the 8086 operates in minimum mode. The CPU sends bus control signals itself through pins 24 through 31. This is shown in the Connection Diagrams (in parentheses). Examples of minimum and maximum mode systems are shown in Figure 2.

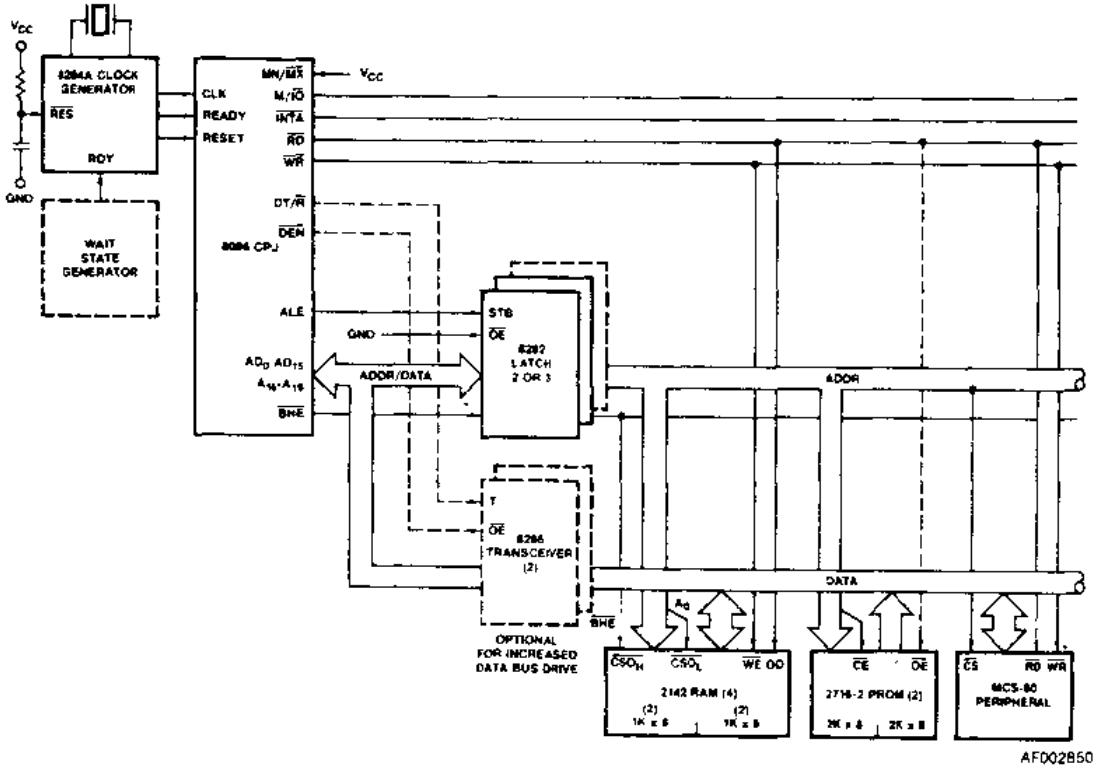

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Figure 2a. Minimum Mode 8086 Typical Configuration