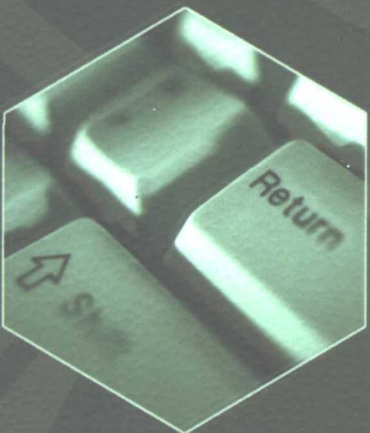
高等学校专业英语教材

计算机专业英语教程

（第3版）



金志权　张幸儿　主编

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内容简介

本书旨在使读者掌握计算机专业英语术语，培养和提高读者阅读和笔译专业英语文献资料的能力，并通过课堂英语交流，提高学生英语口语能力。

本书素材取自国外最近几年计算机科学各个领域的最新教材、专著、论文和计算机网络信息，内容新颖、覆盖面广、系统性强、可读性好。为了方便教学，本书附有部分参考译文，以及取材所用的参考文献。

本书可以作为高等院校计算机专业的专业英语教材，也可供计算机专业人员及其他有兴趣的读者学习参考。

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第 3 版前言

本书旨在使读者掌握计算机专业英语术语，培养和提高读者阅读和笔译专业英语文献资料的能力，并通过课堂英语交流，提高学生的英语口头表达能力。

为了便于读者阅读和口语练习，本版做了如下修改：

- 单词部分提供国际音标，并增加了数学符号表示法的读法
- 注释部分增加专业知识的诠释
- 练习部分提供了英语口语练习的题目
- 提供更多的参考译文

为反映计算机科学的当前发展，在内容上也进行了补充和调整：

- 把第 1 课扩充成两课：硬件Ⅰ和硬件Ⅱ，内容包括闪存、USB 接口、总线和 IC 等
- 网络增加了无线网
- 数据库部分增加了数据挖掘
- 其他调整，例如补充了作为近世代数基本内容的半群与群一节等

本书可读性好，内容覆盖面大，且反映了计算机科学的基础和当前发展，可供各大专院校作为计算机专业英语教材，也可作为其他广大读者的自学教材。

本书保持了前两版的编排格式和基本风格。各校教师可根据自己的具体情况，因材施教，在每一课里挑选若干篇课文进行教学。本书每一课都给出了笔译和口语两种练习题。为了加强学生的英语口语能力，可结合所列题目，组织学生进行课堂小组讨论或讲述。

本书共分 15 课，第 1、2、4、5、6、8、10、15 课由金志权编写，第 3、7、9、11、12、13、14 课由张幸儿编写。彼此进行了互审。

在此感谢对本书的编写给予帮助的南京大学陈佩佩、李存珠、陆钟楠、张福炎、李宣东、杨献春等老师，南京师范大学顾铁成老师，南京大学外国语学院王守成、杨治中、侯焕谬、张子清等老师。同时还要感谢丁正全、张万华、韩杰等提供的支持与帮助。

限于作者水平，书中难免会有不妥和错误之处，敬请读者批评指正。

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于南京大学

CONTENTS

Lesson 1 Hardware I

1.1 A Closer Look at the Processor and Primary Storage

We have learned that all computers have similar capabilities and perform essentially the same functions, although some might be faster than others. We have also learned that a computer system has input, output, storage, and processing components; that the processor is the "intelligence" of a computer system; and that a single computer system may have several processors. We have discussed how data are represented inside a computer system in electronic states called bits. We are now ready to expose the inner workings of the nucleus of the computer system—the processor.

The internal operation of a computer is interesting, but there really is no mystery to it. The mystery is in the minds of those who listen to hearsay and believe science-fiction writer. The computer is a nonthinking electronic device that has to be plugged into an electrical power source, just like a toaster or a lamp.

Literally hundreds of different types of computers are marketed by scores of manufacturers[1]. The complexity of each type may vary considerably, but in the end each processor, sometimes called the **central processing unit or CPU**, has only two fundamental sections: the control unit and the arithmetic and logic unit. Primary storage also plays an integral part in the internal operation of a processor. These three—primary storage, the control unit, and the arithmetic and logic unit—work together. Let's look at their functions and the relationships between them.

Unlike magnetic secondary storage devices, such as tape and disk, primary storage has no moving parts. With no mechanical movement, data can be accessed from primary storage at electronic speeds, or close to the speed of light. Most of today's computers use CMOS (Complementary Metal-Oxide Semiconductor) technology for primary storage. A state-of-the-art CMOS memory chip about one eighth the size of a postage stamp[2] can store about 4,000,000 bits, or over 400,000 characters of data!

Primary storage, or main memory, provides the processor with temporary storage for programs and data. All programs and data must be transferred to primary storage from an input device (such as a VDT) or from secondary storage (such as a disk) before programs can be executed or data can be processed. Primary storage space is always at a premium; therefore, after a program has been executed, the storage space it occupied is reallocated to another program awaiting execution.

Figure 1-1 illustrates how all input/output (I/O) is "read to" or "written from" primary storage. In the figure, an inquiry (input) is made on a VDT. The inquiry, in the form of a message, is routed to primary storage over a channel (such as a coaxial cable). The message is interpreted, and the processor initiates action to retrieve the appropriate program and data from secondary storage[3]. The program and data are "loaded", or moved, to primary storage from secondary storage. This is a nondestructive read process. That is, the program and data that are read reside in both primary storage (temporarily) and secondary storage (permanently). The data are manipulated according to program instructions, and a report is written from primary storage to a printer.

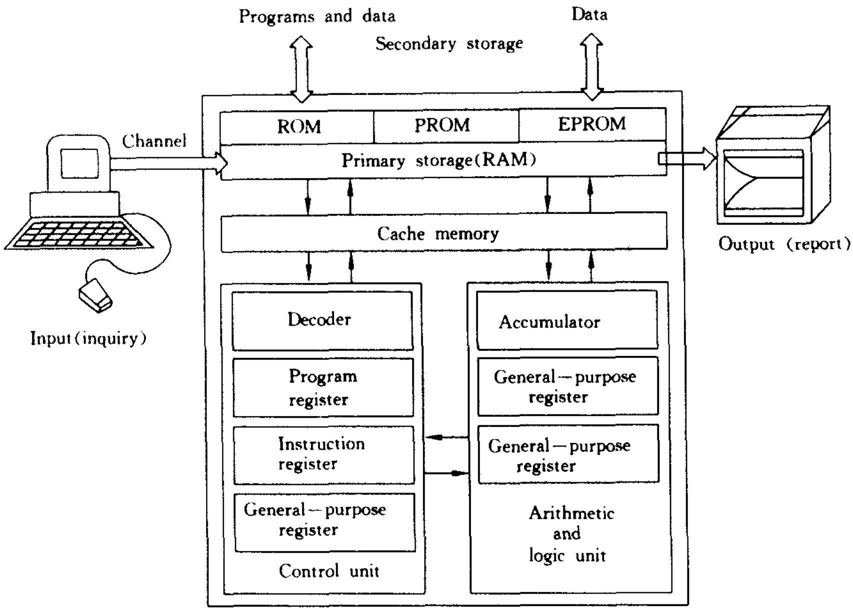

Figure 1-1 Interaction Between Primary Storage and Computer System Components
All programs and data must be transferred from an input device or from secondary storage before programs can be executed and data can be processed. During processing, instructions and data are passed between the various types of internal memories, the control unit, and the arithmetic and logic unit. Output is transferred to the printer from primary storage.

A program instruction or a piece of data is stored in a specific primary storage location called an **address**. Addresses permit program instructions and data to be located, accessed, and processed. The content of each address is constantly changing as different programs are executed and new data are processed.

Another name for primary storage is random-access memory, or RAM. A special type of primary storage, **called read-only memory (ROM)**, cannot be altered by the programmer. The contents of ROM are "hard-wired" (designed into the logic of the memory chip) by the manufacturer and can be "read only". When you turn on a microcomputer system, a program in ROM automatically readies the computer system for use. Then the ROM program produces the initial display screen prompt.

A variation of ROM is **programmable read-only memory (PROM)**. PROM is ROM into which you, the user, can load "read-only" programs and data. Once a program is loaded to PROM, it is seldom, if ever, changed[4]. However, if you need to be able to revise the contents of PROM, there is **EPROM**, erasable PROM. Before a write operation, all the storage cells must be erased to the same initial state.

A more attractive form of read-mostly memory is *electrically erasable programmable read-only memory* (EEPROM). It can be written into at any time without erasing prior contents; only the byte or bytes addressed are updated[5].

The EEPROM combines the advantage of nonvolatility with the flexibility of being updatable in place[6], using ordinary bus control, address, and data lines.

Another form of semiconductor memory is *flash memory* (so named because of the speed). Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. In addition, it is possible to erase just blocks of memory rather than an entire chip. However, flash memory does not provide byte—level erasure[7]. Like EPROM, flash memory uses only one transistor per bit, and so achieves the high density of EPROM.

Cache Memory

Program and data are loaded to RAM from secondary storage because the time required to access a program instruction or piece of data from RAM is significantly less than from secondary storage. Thousands of instructions or pieces of data can be accessed from RAM in the time it would take to access a single piece of data from disk storage[8] RAM is essentially a high-speed holding area for data and programs. In fact, nothing really happens in a computer system until the program instructions and data are moved to the processor. This transfer of instructions and data to the processor can be time-consuming, even at microsecond speeds. To facilitate an even faster transfer of instructions and data to the processor, most computers are designed with **cache memory**. Cache memory is employed by computer designers to increase the computer system **throughput** (the rate at which work is performed).

Like RAM, cache is a high-speed holding area for program instructions and data. However, cache memory uses a technology that is about 10 times faster than RAM and about 100 times more expensive. With only a fraction of the capacity of RAM, cache memory holds only those instructions and data that are likely to be needed next by the processor.

Words and Expressions

processor ['prəusesə] *n.* 处理机
primary storage 主存储器
bit [bit] *n.* 位,二进制位,比特
hearsay ['hiəsei] *n.* 传闻,谣传
scores of 许多
CPU 中央处理机
control unit 控制部件
arithmetic and logic unit 算术逻辑部件
integral parts 不可缺的部分,组成部分
tape and disk 这里指磁带和磁盘
CMOS 互补金属氧化物半导体
a state of the art (the state of the art) 目前工艺水平,最新发展水平
chip [tʃip] *n.* 芯片
VDT(Video Display Terminal) 视频显示终端
secondary storage 辅助存储器,二级存储器
at a premium 非常珍贵
reallocate [ri:'æləkeit] *v.* 重新分配
capacity [kə'pæsiti] *n.* 容量
coaxial cable *n.* 同轴电缆
program and data *n.* 程序和数据
instruction [in'strʌkʃən] *n.* 指令
location [ləu'keiʃən] *n.* 单元,位置
RAM 随机存取存储器; ROM 只读存储器
hard-wired 固化,硬件(线路)实现的
EPROM 可擦可编程只读存储器

cache [kæʃ] *n.* 高速缓存

throughput [θru(:)'put] *n.* 吞吐量，生产量，生产能力

read-mostly 以读为主的，大多数为读的

EEPROM 电可擦可编程 ROM

nonvolatility [nɔn'vɔlə'tiliti] *n.* 非易失性

updatable ['ʌpˌdeitəbl] *adj.* 可修改的

in place 在适当的地方，存在

semiconductor [semikən'dʌktə] *n.* 半导体

flash memory 闪存

functionality ['fʌŋkʃəneiliti] *n.* 功能，功能性，函数性

byte-level 字节级

Notes

1. 这里 are marketed 意为"被销售"，literally 译为"不加夸张地讲，确实地"。全句可译为：不加夸张地讲，市场上有几百种不同类型的计算机在销售。
2. about one eighth the size of a postage stamp 是介词短语，修饰前面的 CMOS memory chip，即约 1/8 邮票大小(的)。
3. retrieve the appropriate…意为"取出所需的……"，initiate 译为"启动，初始化"。本句译为：消息被解释，处理机从辅助存储器取出所需的程序和数据。
   本句的上一句中 route 译为"发送，路由"。全句译为：查询以消息的形式通过通道（像同轴电缆）发送到主存储器。
4. it is seldom, if ever, changed 中插入的 if ever 是常见用法，可译为"它简直从不改变"。
5. only the byte or bytes addressed 中 addressed 修饰前面的 the byte or bytes。本句可译为：EEPROM 在任何时候都可写入，不需擦除原先内容，且只更新寻址到的字节或多个字节。
6. being updatable in place 是 of 的介词短语。in place 是指需要更新的地方，因此短语的含义是"可更新、需要更新的字节"。本句可译为：EEPROM 把非易失性优点和可更新、需更新的地方的灵活性结合起来，修改时使用普通的总线控制线、地址线和数据线。
7. 本句说的"闪存不提供字节级的擦除"(flash memory does not provide byte－level erasure) 是针对 EEPROM 可对字节修改，即提供字节级的擦除；而 EPROM 若要修改字节，则必须先擦除整块 EPROM 的原先内容，所以三种存储的擦除单位分别是：

EPROM　　　　　整个存储器

Flash memory　　块(类似于硬盘)

EEPROM　　　　字节(可能多个字节)

目前的移动 U 盘,数码相机等的闪存卡:CF 卡(Compact Flash),Smart Media 卡,xD 卡(eXtreme Digital),记忆棒(Memory Stick),SD 卡(Secure Digital) 等都用闪存。

8. it would take to access…是定语从句,修饰前面的 the time,其前面省略了关系代词 that。it 是引导词,作形式主语,真实主语是动词不定式 to access…。access 译为“访问,存取”。全句译为:从磁盘存储器上存取单个数据所花的时间,可以从 RAM 中存取几千条指令或数据。

注:本书主要介绍计算机的 CPU 和主存,包括最近普及很快的闪存。

1.2 Bus Interconnection

A bus is a communication pathway connecting two or more devices. A key characteristic of a bus is that it is a shared transmission medium[1]. Multiple devices connect to the bus, and a signal transmitted by any one device is available for reception by all other devices attached to the bus. If two devices transmit during the same time period, their signals will overlap and become garbled. Thus, only one device at a time can successfully transmit.

Typically, a bus consists of multiple communication pathways, or lines. Each line is capable of transmitting signals representing binary 1 and binary 0. Over time, a sequence of binary digits can be transmitted across a single line. Taken together[2], several lines of a bus can be used to transmit binary digits simultaneously (in parallel). For example, an 8-bit unit of data can be transmitted over eight bus lines.

Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy[3]. A bus that connects major computer components (processor, memory, I/O) is called a *system bus*.

A system bus consists, typically, of from 50 to 100 separate lines. Each line is assigned a particular meaning or function. Although there are many different bus designs, on any bus the lines can be classified into three functional groups (Figure 1-2): data, address, and control lines. In addition, there may be power distribution lines that supply power to the attached modules[4].

The *data lines* provide a path for moving data between system modules. These lines, collectively, are called the *data bus*. The data bus typically consists of 8, 16, or

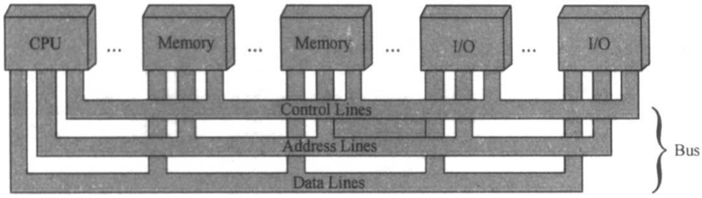

Figure 1-2 Bus Interconnection Scheme

32 separate lines, the number of lines being referred to as the *width* of the data bus [5]. Because each line can carry only 1 bit at a time, the number of lines determines how many bits can be transferred at a time. The width of the data bus is a key factor in determining overall system performance.

The address lines are used to designate the source or destination of the data on the data bus. For example, if the processor wishes to read a word of data from memory, it puts the address of the desired word on the address lines. Clearly, the width of the address bus determines the maximum possible memory capacity of the system.

The control lines are used to control the access to and the use of the data and address lines [6]. Because the data and address lines are shared by all components, there must be a means of controlling their use. Control signals transmit both command and timing information between system modules. Timing signals indicate the validity of data and address information. Command signals specify operations to be performed.

Most computer systems enjoy the use of multiple buses, generally laid out in a hierarchy[7]. A typical high-performance architecture is shown in Figure 1-3. There is a local bus that connects the processor to a cache controller, which is in turn connected to a system bus that supports main memory. The cache controller is integrated into a bridge that connects to the high-speed bus[8]. This bus supports connections to high-speed LANs, video and graphics workstation controller, as well as interface controller to local peripheral buses, including SCSI, and FireWire [9]. Lower-speed devices are still supported off an expansion bus, with an interface buffering traffic between the expansion bus and the high-speed bus [10].

PCI

The peripheral component interconnect (PCI) is a popular high-bandwidth, processor-independent bus that can function as a mezzanine or **peripheral bus** [11]. The current standard allows the use of up to 64 data lines at 66 MHz, for a raw transfer rate of 528 Mbytes/s, or 4.224 Gbps [12]. PCI is designed to support a variety of microprocessor-

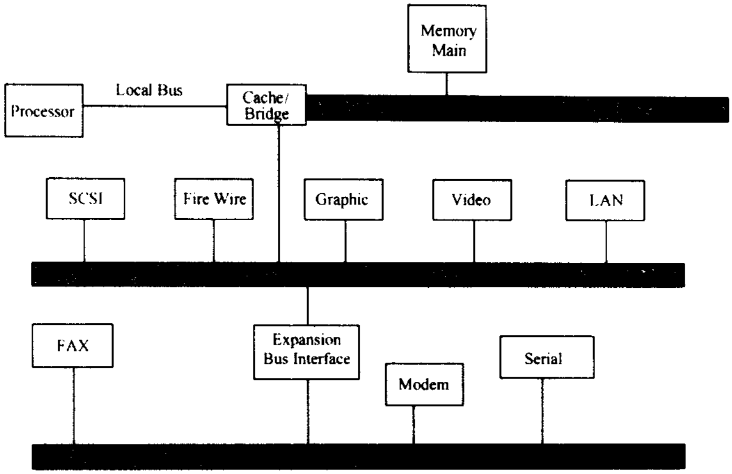

Figure 1-3 Example Bus Configuration

based configurations[13], including both single- and multiple-processor systems. Accordingly, it provides a general-purpose set of functions. It makes use of synchronous timing and a centralized arbitration scheme[14].

In a multiprocessor system (Figure 1-4), one or more PCI configurations may be connected by bridges to the processor's system bus. The system bus supports only the processor/cache units, main memory, and PCI bridges. The use of bridges keeps the PCI independent of the processor speed yet provides the ability to receive and deliver data rapidly[15].

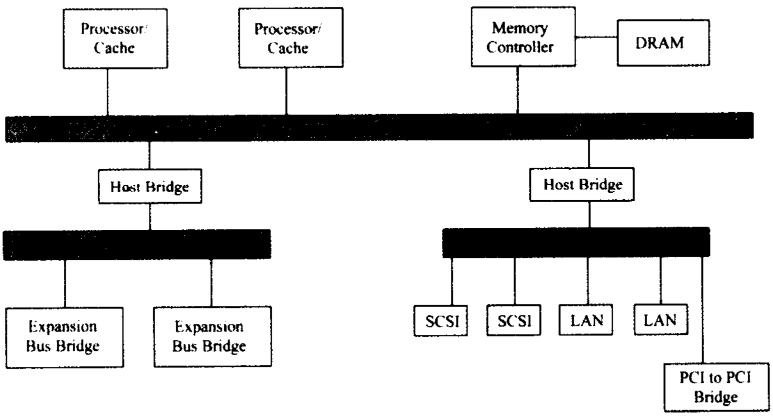

Figure 1-4 Typical Server System

Words and Expressions

bus [bʌs] *n.* 总线

pathway ['pa:θwei] *n.* 通路，路径

interconnection [intə(:)kə'neikʃən] *n.* 互连

share [ʃεə] *n.* *vt.* 共享，分享，均分

overlap [əuvə'læp] *v.* 重叠，交迭

garble ['ga:bl] *vt.* 混淆，篡改

over time　一段时间里

in parallel　并行地

hierarchy ['haiəra:ki] *n.* 分层（结构），层次

collectively [kə'lektivli] *adv.* 合在一起，集体地

overall [əuvər'ɔ:l] *adj.* 总的，总体的

timing ['taimiŋ] *n.* 时序、定时，同步

integrated ['intigreitid] *adj.* 集成

controller [kən'trəulə] *n.* 控制器

SCSI　参见 2.4

traffic ['træfik] *n.* 通信流量，信息量，交通

bandwidth ['bændwitθ] *n.* 带宽

processor-independent　独立于处理器的

mezzanine ['mezəni:n] *n.* 中间层，夹层楼面

adapter [ə'dæptə] *n.* 适配器

Mbytes (mega byte)　*n.* 兆字节，10^6 字节

Gbps (giga bit per second)　每秒千兆位

synchronous ['siŋkrənəs] *adj.* 同步

centralized arbitration　集中式仲裁

bridge [bridʒ] *n.* 桥，桥接器

Notes

1. shared transmission medium 意为"共享传输介质"。下两句解释了共享传输介质，即一个设备发出的信号可以为其他所有连接到该总线上的设备所接收。如果两个设备同时传送，则它们的信号将会重叠，引起混淆。
2. taken together 意指"（几条线被）放在一起"。全句可译为：总线的几条线放在一起能同时并行传送二进制数字。