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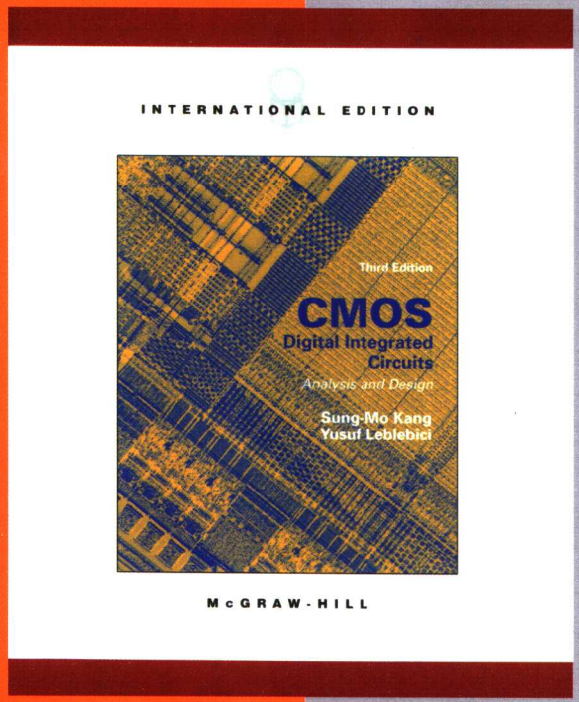
Sung-Mo Kang, Yusuf Leblebici

CMOS数字集成电路

—— 分析与设计

（第3版）



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CMOS数字集成电路

—— 分析与设计

（第3版）

CMOS Digital Integrated Circuits

Analysis and Design

(Third Edition)

Sung-Mo Kang

Yusuf Leblebici

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出 版 前 言

微电子技术是信息科学技术的核心技术之一，微电子产业是当代高新技术产业群的核心和维护国家主权、保障国家安全的战略性产业。我国在《信息产业“十五”计划纲要》中明确提出：坚持自主发展，增强创新能力和核心竞争力，掌握以集成电路和软件技术为重点的信息产业的核心技术，提高具有自主知识产权产品的比重。发展集成电路技术的关键之一是培养具有国际竞争力的专业人才。

微电子技术发展迅速，内容更新快，而我国微电子专业图书数量少，且内容和体系不能反映科技发展的水平，不能满足培养人才的需求，为此，我们系统挑选了一批国外经典教材和前沿著作，组织分批出版。图书选择的几个基本原则是：在本领域内广泛采用，有很大影响力；内容反映科技的最新发展，所述内容是本领域的研究热点；编写和体系与国内现有图书差别较大，能对我国微电子教育改革有所启示。本套丛书还侧重于微电子技术的实用性，选取了一批集成电路设计方面的工程技术用书，使读者能方便地应用于实践。本套丛书不仅能作为相关课程的教科书和教学参考书，也可作为工程技术人员的自学读物。

我们真诚地希望，这套丛书能对国内高校师生、工程技术人员以及科研人员的学习和工作有所帮助，对推动我国集成电路的发展有所促进。也衷心期望着广大读者对我们一如既往的关怀和支持，鼓励我们出版更多、更好的图书。

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CMOS Digital Integrated Circuits
Analysis and Design

影 印 版 序

《CMOS 数字集成电路——分析与设计》(CMOS Digital Integrated Circuits: Analysis and Design)一书，是美国巴斯肯工学院 Sung-Mo (Steve) Kang 教授和洛桑瑞士联邦工学院 Yusef Leblebici 教授编著的一本讨论 CMOS 数字集成电路分析与设计的教材。该书于 1995 年首版，1998 年出版第 2 版，本次由清华大学出版社引进的是 2002 年出版的第 3 版。该教材内容全面，理论阐述明晰，技术介绍详尽，被国外多所大学作为教材使用。引进该教材对推动我国集成电路设计高水平人才的培养具有积极意义。

考虑到国内教学的实际情况，在清华大学出版社的组织下，本人对该书进行了修订。修订后的学生影印版基本保持了原书的结构和内容。没有选入的只涉及原书中的 MOS 参数测试（Measurement of Parameters，原版 3.4 节中的部分内容）、电压提升（Voltage Bootstrapping，原版 9.3 节）和绝热逻辑电路（Adiabatic Logic Circuits，原版 11.6 节）等对全书完整性不产生太大影响的少量内容。可以相信，这本优秀的影印版教材对采用它进行双语教学的师生以及从事 CMOS 逻辑集成电路设计工作的工程师会提供有益的帮助。

王志功

2004 年 4 月

于东南大学

ABOUT THE AUTHORS

Sung-Mo "Steve" Kang received the Ph.D. degree in electrical engineering from the University of California at Berkeley. He has worked on CMOS VLSI design at AT&T Bell Laboratories at Murray Hill, NJ as supervisor and member of technical staff of high-end CMOS VLSI microprocessor design until 1985. Previously, he was department head and professor of electrical and computer engineering department at the University of Illinois at Urbana-Champaign. Currently, he is dean of the Baskin School of Engineering and professor of electrical engineering at the University of California at Santa Cruz. He was the founding editor-in-chief of the *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* and has served on editorial boards of several IEEE and international journals. He is Fellow of IEEE, ACM, and AAAS and recipient of IEEE Third Millennium Medal, IEEE Graduate Teaching Technical Field Award, UC Berkeley Distinguished Alumnus Award, SRC Technical Excellence Award, IEEE Circuits and Systems Society Technical Achievement Award, Alexander von Humboldt U.S. Senior Scientist Award, IEEE CAS Darlington Prize Paper Award, KBS Award, and several other best paper awards.

Yusuf Leblebici received the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign. He was a visiting assistant professor of electrical and computer engineering at the University of Illinois at Urbana-Champaign, associate professor of electrical and electronics engineering at Istanbul Technical University, and associate professor of electrical and computer engineering at Worcester Polytechnic Institute. He also served as the microelectronics program coordinator at Sabanci University. Currently, he is full (chair) professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland and director of the Microelectronic Systems Laboratory. His research interests include design of high-performance CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is a Senior Member of IEEE, and recipient of the NATO Science Fellowship Award, the Young Scientist Award of the Turkish Scientific and Technological Research Council, and the Joseph Samuel Satin Distinguished Fellow Award of the Worcester Polytechnic Institute.

PREFACE

Complementary metal oxide semiconductor (CMOS) digital integrated circuits are the enabling technology for the modern information age. Because of their intrinsic features in low-power consumption, large noise margins, and ease of design, CMOS integrated circuits have been widely used to develop random access memory (RAM) chips, microprocessor chips, digital signal processor (DSP) chips, and application-specific integrated circuit (ASIC) chips. The popular use of CMOS circuits continues to grow with the increasing demands for low-power, low-noise integrated electronic systems in the development of portable computers, personal digital assistants (PDAs), portable phones, and multimedia agents.

Since the field of CMOS integrated circuits is very broad, it is conventionally divided into digital CMOS circuits and analog CMOS circuits. This book is focused on the CMOS digital integrated circuits. However, it should be noted that the boundary between classical digital and analog CMOS design is becoming increasingly blurred, especially with the challenges presented by very deep sub-micron (VDSM) fabrication technologies, very low operating voltages, and operating frequencies extending well into the GHz range. Therefore, we attempt to present the analysis and design of digital CMOS integrated circuits from an "analog" point-of-view, i.e., taking into account the analog, non-discrete nature of the devices and circuits that are used to implement digital functions.

The origins of this textbook date back to the early 1990s when both authors were intensively involved in undergraduate and graduate level teaching of digital IC fundamentals. At the University of Illinois at Urbana-Champaign, where both of us were teaching at the time, we tried some of the available textbooks on digital MOS integrated circuits for our senior-level technical elective course, ECE382—*Large Scale Integrated Circuit Design*. Students and instructors alike realized, however, that there was a need for a new book with more comprehensive treatment of CMOS digital circuits. Thus, our textbook project was initiated several years ago by assembling our own lecture notes. Since 1993, we have used evolving versions of this material at the University of Illinois at Urbana-Champaign, at Istanbul Technical University, at Worcester Polytechnic Institute, and at the Swiss Federal Institute of Technology in Lausanne. Both authors were very much encouraged by comments from their students, colleagues, and reviewers. The first edition of *CMOS Digital Integrated Circuits: Analysis and Design* was published in late 1995.

Soon after publishing the first edition, we saw the need for updating it to reflect many constructive comments we were receiving from instructors and students who used the textbook. We intended to include and update important topics such as low-power circuit design, interconnects in high-speed circuit design, as well as the deep

sub-micron circuit design issues, and to provide more rigorous treatment of new developments in memory circuits. We also felt that in a very rapidly developing field such as CMOS digital circuits, the quality of a textbook can only be preserved by timely updates reflecting the current state-of-the-art. This realization has led us to embark on the extensive and continuous revision of our work, with the Second Edition appearing in 1998 and the Third Edition in 2002, to reflect recent advances in technology and in circuit design practices.

This book, *CMOS Digital Integrated Circuits: Analysis and Design,* is primarily intended as a comprehensive textbook at the senior level and first-year graduate level, as well as a reference for practicing engineers in the areas of integrated circuit design, digital design, and VLSI. Recognizing that the area of digital integrated circuit design is evolving at an increasingly faster pace, we have made our best effort to present up-to-date materials on all subjects covered. This book contains fifteen chapters; and we recognize that it would not be possible to cover rigorously all of this material in one semester. Thus, we would propose the following based on our teaching experience: At the undergraduate level, coverage of the first ten chapters would constitute sufficient material for a one-semester course on CMOS digital integrated circuits. Time permitting, some selected topics in Chapter 11, *Low-Power CMOS Logic Circuits,* Chapter 12, *BiCMOS Logic Circuits,* and Chapter 13, *Chip Input and Output (I/O) Circuits* can also be covered. Alternatively, this book can be used for a two-semester course, allowing a more detailed treatment of advanced issues, which are presented in the later chapters. At the graduate level, selected topics from the first ten chapters plus the last five chapters can be covered in one semester.

The first eight chapters of this book are devoted to a detailed treatment of the MOS transistor with all its relevant aspects; to the static and dynamic operation principles, analysis, and design of basic inverter circuits; and to the structure and operation of combinational and sequential logic gates. Note that the introduction chapter has been significantly expanded to include a detailed presentation of VLSI design methodologies. Since the digital IC design techniques discussed in the first half of this book are directly relevant for digital VLSI and ASIC design, we felt that the context should be presented at the very beginning of the book. The issues of on-chip interconnect modeling and interconnect delay calculation are covered extensively in Chapter 6, which provides a complete view of switching characteristics in digital integrated circuits. A separate chapter (Chapter 9) has been reserved for the treatment of *dynamic* logic circuits, which are used in state-of-the-art VLSI chips. Chapter 10 has been completely revised in both content and presentation; it offers an in-depth presentation of many state-of-the-art semiconductor memory circuits.

Recognizing the increasing importance of low-power circuit design, we dedicate one chapter (Chapter 11) to low-power CMOS logic circuits, which provides a comprehensive coverage of methodologies and design practices that are used to reduce the power dissipation of large-scale digital integrated circuits. BiCMOS digital circuit design is examined in Chapter 12, with a thorough coverage of bipolar transistor basics. In view of the continuing use of bipolar and BiCMOS circuits in very high-speed designs, we believe that at least one chapter should be allocated to cover the basics of bipolar transistors. Next, Chapter 13 provides a clear insight into the important

subject of chip I/O design. Critical issues such as ESD protection, clock distribution, clock buffering, and latch-up phenomena are discussed in detail. Finally, the more advanced but very important topics of design for manufacturability and design for testability are covered in Chapters 14 and 15, respectively.

The authors have long debated the coverage of nMOS circuits in this book. We have concluded that some coverage should be provided for pedagogical reasons. Studying nMOS circuits will better prepare readers for analysis of other field effect transistor (FET) circuits such as GaAs circuits, the topology of which is quite similar to that of depletion-load nMOS circuits. Thus, to emphasize the *load* concept, which is still widely used in many areas in digital circuit design, we present basic depletion-load nMOS circuits along with their CMOS counterparts in several places throughout the book.

Although an immense amount of effort and attention to detail were expended to prepare the camera-ready manuscript, this book may still have some flaws and mistakes due to erring human nature. The authors would welcome and greatly appreciate suggestions and corrections from the readers, for the improvement of technical content as well as the presentation style.

ACKNOWLEDGMENTS FOR THE FIRST EDITION

Our colleagues have provided many constructive comments and encouragement for the completion of the first edition. Professor Timothy N. Trick, former head of the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign, has strongly supported our efforts from the very beginning. The appointment of Sung-Mo Kang as an associate in the Center for Advanced Study at the University of Illinois at Urbana-Champaign helped to start the process.

Yusuf Leblebici acknowledges the full support and encouragement from the department of electrical and electronics engineering at Istanbul Technical University, where he introduced a new digital integrated circuits course based on the early version of this book and received very valuable feedback from his students. Yusuf Leblebici also thanks the ETA advanced Electronics Technologies Research and Development Foundation at Istanbul Technical University for their generous support.

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The authors would like to express sincere gratitude to Professor Janak Patel of the University of Illinois at Urbana-Champaign for generously mentoring the authors in writing Chapter 16, *Design for Testability*. Professor Patel has provided many constructive comments and many of his expert views on the subject are reflected in this chapter. Professor Prith Banerjee of Northwestern University and Professor Farid Najm of the University of Illinois at Urbana-Champaign also provided many good comments. We would also like to thank Dr. Abhijit Dharchoudhury for his invaluable contribution to Chapter 15, *Design for Manufacturability*.

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Many of the authors' former and current students at the University of Illinois at Urbana-Champaign also helped in the preparation of figures and verification of circuits using SPICE simulations. In particular, Dr. James Morikuni, Dr. Weishi Sun, Dr. Pablo Mena, Dr. Jaewon Kim, Mr. Steve Ho, and Mr. Sueng-Yong Park deserve recognition. Ms. Lilian Beck and the staff members of the Publications Office in the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign read the entire manuscript and provided excellent editorial comments.

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The authors are truly indebted to many individuals who, with their efforts and their help, made the second edition possible. We would like to thank Dr. Wolfgang Fichtner, President and CEO of ISE Integrated Systems Engineering, Inc., and the technical staff of ISE in Zurich, Switzerland for providing computer-generated cross-sectional color graphics of MOS transistors and CMOS inverters, which are featured in the color plates. The first author acknowledges the support provided by the U.S. Senior Scientist Research Award from the Alexander von Humbold Stiftung in Germany, which was very helpful for the second edition. The appointments of the

second author as Associate Professor at Worcester Polytechnic Institute and as Visiting Professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland have provided excellent environments for the completion of the revision project. The second author also thanks Professor Daniel Mlynek of the Swiss Federal Institute of Technology in Lausanne for his continuous encouragement and support. Many of the authors' former and current students at the University of Illinois at Urbana-Champaign, at the Swiss Federal Institute of Technology in Lausanne, and at Worcester Polytechnic Institute also helped in the preparation of figures and verification of circuits using SPICE simulations. In particular, Dr. James Stroming and Mr. Frank K. G rkaynak deserve special recognition for their extensive and valuable efforts.

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Several individuals have contributed with their time and their efforts to the third edition of our textbook. The authors would like to acknowledge the invaluable contribution of Dr. Seung-Moon Yoo who was instrumental in the extensive revision of the Memory chapter (Chapter 10). His technical insight, his meticulous attention to detail, and his very productive work are truly appreciated. The first author acknowledges the University of California at Santa Cruz for valuable support in his new position as Dean of the School of Engineering, and for enabling him to concentrate on the revision of the manuscript. The appointment of the second author as Full Professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland has also provided an excellent environment for the completion of the project. The second author gratefully acknowledges Mme. S verine Eggli for her valuable assistance in revisions, and for typing sections of the text. The authors thank Mr. Tom Vernier and the technical staff of the MOSIS organization for generously providing the SPICE BSIM parameters for TSMC 0.18 μm process that were extracted by MOSIS. The authors also acknowledge Dr. Michael W. Davidson of the Florida State University

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Finally, we would like to acknowledge the support from our families, Myoung-A (Mia), Jennifer, and Jeffrey Kang, and Anıl and Ebru Leblebici, for tolerating many of our physical and mental absences while we worked on the third edition of this book, and for providing us invaluable encouragement throughout the project.

Sung-Mo (Steve) Kang
Santa Cruz, California
August 2002

Yusuf Leblebici
Lausanne, Switzerland
August 2002

CONTENTS

CHAPTER 1

Introduction

1.1 Historical Perspective

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. Typically, the required computational and information processing power of these applications is the driving force for the fast development of this field. Figure 1.1 gives an overview of the prominent trends in information technologies over the next decade. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications for VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend to become more personalized, which means that the information processing devices must be more intelligent and also be portable to allow more mobility. This trend towards portable, distributed system architectures is one of the main driving forces for system integration, even though it does not preclude a concurrent and equally important trend towards centralized, highly powerful information systems such as those required for network computing (NC) and video services.

As more and more complex functions are required in various data processing and telecommunications devices, the need to integrate these functions in a small package is also increasing. The level of integration as measured by the number of logic gates in a monolithic chip has been steadily rising for almost three decades, mainly due to the rapid progress in processing technology and interconnect technology. Table 1.1 shows the evolution of logic complexity in integrated circuits over the last three decades, and marks the *milestones* of each era. Here, the numbers for circuit complexity should be viewed only as representative measures to indicate the order-of-magnitude. A logic block can contain anywhere from 10 to 100 transistors,

Table 1.1 Evolution of logic complexity in integrated circuits

Era	Date	Complexity (# of logic blocks per chip)
Single transistor	1958	<1
Unit logic (one gate)	1960	1
Multi-function	1962	2–4
Complex function	1964	5–20
Medium Scale Integration (MSI)	1967	20–200
Large Scale Integration (LSI)	1972	200–2,000
Very Large Scale Integration (VLSI)	1978	2,000–20,000
Ultra Large Scale Integration (ULSI)	1989	20,000–?

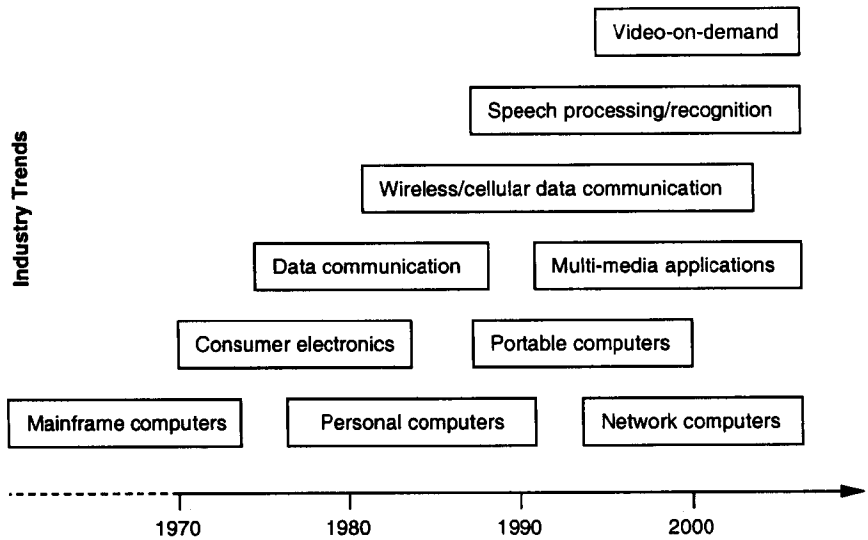

Figure 1.1 Prominent "driving" trends in information service technologies.

depending on the function. State-of-the-art ULSI chips, such as the *DEC Alpha* or the *INTEL Pentium,* contain 10 to 100 million transistors. Note that the term VLSI has been used continuously even for chips in the ULSI (Ultra Large Scale Integration) category, not necessarily abiding by the distinction in Table 1.1.

The monolithic integration of a large number of functions on a single chip usually provides:

- Less area/volume and therefore, compactness
- Less power consumption
- Less testing requirements at system level
- Higher reliability, mainly due to improved on-chip interconnects
- Higher speed, due to significantly reduced interconnection length
- Significant cost savings