



信息科学技术学术著作丛书

Modern ASIC Design

现代应用集成电路设计

Zhou Dian



科学出版社

国家科学技术学术著作出版基金资助出版

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周 电 著

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北 京

内 容 简 介

本书基于作者在美国大学十几年教授“现代应用集成电路设计”课程的手稿整理而成,主要内容包括应用集成电路设计流程、设计指标定义和规范、逻辑电路设计、物理设计、时间功耗性能分析及验证测试。读者需要有数字集成电路和硬件描述语言(VHDL)的基础知识。按照具体课程设置的要求,本书可用于一个学期的教学内容,包括应用集成电路设计流程、设计指标定义和规范、逻辑电路设计及物理设计。关于集成电路发展的前沿问题,本书在第7章和第8章中以研究课题为背影介绍了基础知识。

本书可作为电子和计算机工作专业的大学四年级或硕士研究生教材,也适于集成电路设计的专业人员参考阅读。

图书在版编目(CIP)数据

现代应用集成电路设计=Modern ASIC Design:英文/周电著. —北京:科学出版社, 2011.7

(信息科学技术学术著作丛书)

ISBN 978-7-03-031766-7

I. ①现… II. ①周… III. ①集成电路-电路设计-英文 IV. ①TN402

中国版本图书馆 CIP 数据核字(2011) 第 125149 号

责任编辑:孙 芳 / 责任校对:张凤琴

责任印制:赵 博 / 封面设计:鑫联必升

科学出版社 出版

北京东黄城根北街 16 号

邮政编码: 100717

<http://www.sciencep.com>

双青印刷厂印刷

科学出版社发行 各地新华书店经销

*

2011 年 7 月第 一 版 开本: B5 (720 × 1000)

2011 年 7 月第一次印刷 印张: 25 1/2 彩插: 2

印数: 1—2 500 字数: 496 000

定价: 120.00 元

(如有印装质量问题, 我社负责调换)

Preface

An application-specific integrated circuit (ASIC) is an integrated circuit customized for a particular application, rather than intended for general-purpose use. In the past decade, ASIC has become more mature in terms of both high design efficiency and low manufacture cost, as compared to many other available technologies. ASICs have penetrated almost every corner of our lives, from traditional computing, telecommunication, and office information processes to medical systems, automobiles, and entertainment.

ASIC design has becoming a major subject in electric and computer engineering due to its importance in modern information industries. This book is written based on the author's teaching experience and class notes on ASIC design. The intention of this book is to provide a textbook for senior level undergraduate or master level graduate students in electric and computer engineering majors. The book addresses practical issues that occur in the entire ASIC design flow, and presents the design from a system development perspective. The book can also be used as training material for engineers who would like to gain the special knowledge in this area.

Many people, especially students who attended the class in the past decade, have contributed to this book, either in shaping the content or in developing the design projects. Some of their contributions have been adopted in this book. Mr. Sagar Patel and David Hernandez-Garduno's project report is used in the Appendix. Mr. Guan-min Huang and Wei Li prepared the drafts of Chapter 5 and 8, respectively. Ms. Cathy Zhou, Belinda Zhou, Sally Liu and Mr. Dennis Liu proofread the book.

Finally, I want to thank my parents Ms. Xin-min Liu and Mr. Guang-fu Zhou for bring me up with a love for science and technology. Most importantly, I want to thank my wife Ms. Anne Y. Zhang for her persistent support of my work for more than two decades.

Zhou Dian
Dallas, Texas, USA
April 3, 2011

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Chapter 1

Introduction

Chapter Objectives

In this chapter, you will be introduced to:

- History and roadmap of IC
- ASIC
- Design flow and tasks
- Electric design automation tools
- An ASIC design project MSDAP
- About this book

1.1 History of Integrated Circuits

In 1951, William Shockley developed the world first junction transistor, and one year later, Geoffrey W. A. Dummer published the concept of the integrated circuits (IC): “Solid block (with) layers of insulating materials”. Then in 1958 Jack Kilby (Figure 1-1) at Texas Instruments suggested the integration of circuit elements such as resistors, capacitors, and transistors into a single chip made of the same material. By September 12th of the same year, Kilby had built a simple oscillator IC with five integrated components as shown in Figure 1-2. This marked the beginning of the modern IC industry.



Figure 1-1 Jack St. Clair Kilby (November 8, 1923–June 20, 2005)

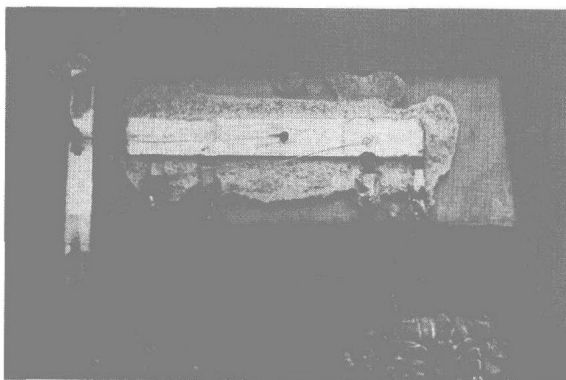


Figure 1-2 Kilby's original integrated circuits

Robert Norton Noyce (Figure 1-3) is also credited for the invention of the integrated circuits. In 1957, Noyce and several other engineers founded Fairchild Semiconductor,

where in 1959 he developed the integrated circuit. His invention was six months late, and Kilby's invention was not shared publicly at the time. In 1968, Noyce and his two Fairchild colleagues founded Intel, with Noyce as president and chief executive officer.

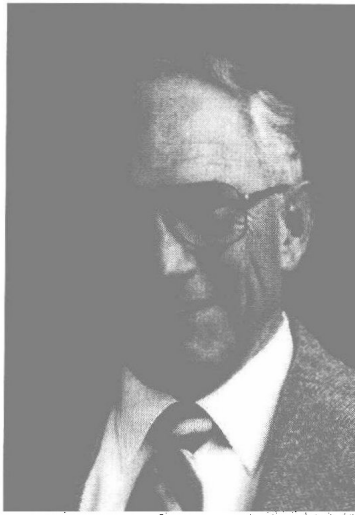


Figure 1-3 Robert Norton Noyce (December 12, 1927–June 3, 1990)

The first single chip microprocessor, based on the silicon IC, was then invented by Intel engineers Federico Faggin, Ted Hoff, and Stan Mazor in 1971. Ever since, the microprocessor has been the heart of modern electronics (Figure 1-4) (Intel 4004, 2010). Today, it can be found in almost all products, ranging from more traditional computers and cell phones, to medical equipment and automobile electronics, to name a few (ARM architecture, 2010).

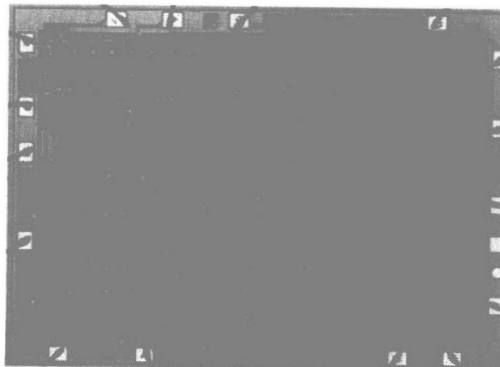


Figure 1-4 Intel 4004 microprocessor

Integrated circuits outperform vacuum tubes in most application areas in terms of size, speed and power consumption. This is attributable to the development of semicon-

ductor physics as well as twentieth century technological advancements in semiconductor device fabrication (Veendrick, 2000; Chang et al., 1996). The integration of large numbers of semiconductor transistors into a small silicon chip was an enormous improvement over the manually assembled circuits, which used discrete electronic components. The integrated circuits' mass production capability, reliability, and computer-aided design tools propelled the rapid adoption of ICs in replacing designs using discrete transistors (Rabeay et al., 2003).

Planar technology and epitaxial deposition have also helped ICs evolve. Metal-oxide-semiconductor field-effect transistors (MOSFET), transistor-transistor logic (TTL), and complementary metal-oxide-semiconductors (CMOS) were invented along the way (Sze, 1988). Today, CMOS contributes to the vast majority of all high density ICs manufactured (Weste et al., 2004; Wolf, 2002).

The advantages of ICs over discrete circuits are primarily cost and performance. Cost is low because the chips, with all of their components, are printed via a photolithography process, and millions of transistors can be manufactured and connected at the same time. Smaller feature size leads to a high performance because the components switch quicker and consume less power, due to the fact that the components are small and close together (Yeap, 1998).

The earliest version of IC, as shown in Figure 1-2, has evolved into a technological wonder. A Pentium 4 microprocessor (Figure 1-5) made in 2000 by Intel had already integrated 42 million transistors and used circuit lines of 0.18 micron feature size, a measurement of how fine we can control a line width in an IC fabrication process (Pentium 4, 2010; Rabeay et al., 2003). As of this writing, a 22nm feature size is available.



Figure 1-5 Pentium 4 microprocessor

In 2000, the importance of the IC was recognized when Kilby shared the Nobel Prize in physics with Zhores I. Alferov and Herbert Kroemer. Kilby was cited by the Nobel committee “for his part in the invention of the integrated circuit”.

The first generation of integrated circuits, called small-scale integration (SSI) circuits, contained only a few transistors. These were normally used for circuits consisting of tens of transistors. The next generation of integrated circuits, called medium-scale integration (MSI) circuits, integrated hundreds of transistors in each chip. MSI extended the integrated logic availability to counters and larger scale logic functions. Further development led to large-scale integration (LSI) in the mid 1970s, with tens of thousands of transistors per chip. LSI allowed for even larger logic functions, such as the first microprocessors Intel 4004 (containing 2000 transistors), to be consolidated into a single silicon chip (Intel 4004, 2010).

Among the most advanced integrated circuits are the microprocessors, which control everything from computers and cellular phones to digital microwave ovens (Microprocessor, 2010). In the last decade, 32-bit and 64-bit microprocessors with cache memory, floating-point arithmetic units, and multi-million transistors on a single piece of silicon have been made popular, marking the era of very large-scale integration (VLSI).

As mentioned before, integrated circuit process technology has consistently improved through smaller feature sizes over the years, allowing more circuitry to be packed into a single chip. As the feature size shrinks, almost everything improves, with cost per unit and the switching power consumption dropping, while speed increases. Small feature size improves the performance of ICs because it allows short traces, which in turn allows low power logic (such as CMOS) to be used at faster switching speed. Historically, people questioned if CMOS could compete with bipolar technology in terms of switching speed. In actuality, continuous feature size shrinking and resulting shorter channel width help maintain CMOS speed and consequently its position as the dominant technology in IC industry (Rabeay et al., 2003; Sze, 1988).

The speed and power consumption gains achieved by narrowing feature size are apparent in almost all applications. As a result, there has been fierce competition among manufacturers to use finer geometries. As a result, state-of-the-art technology for the massive production has reached feature sizes as fine as 22nm and below (ITRS, 2009).

In 1965, Gordon Moore, a director of research and development at Fairchild Semiconductor observed that “the complexity for minimum component cost has increased at a rate of roughly a factor of two per year” (Moore's law, 2010). This observation became the well-known Moore's law: The number of components per IC doubles every year. Moore's law was later amended to: The number of components per IC doubles every 18 months. Figure 1-6 shows the historic data of the real development of IC industry from 1970 to 2002 as a witness of Moor's law (ITRS, 2009). Although

there have been great concerns on the limit of ever increasing system complexity and of the accuracy of lithography, which will eventually put a stop to Moore's law, it is amazing that this rule still holds true currently.

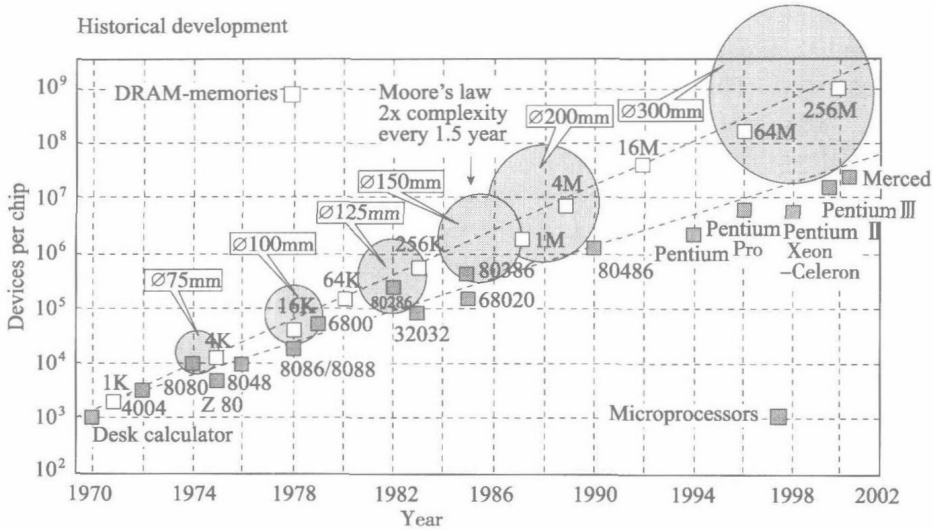


Figure 1-6 Historical development of ICs during the period from 1970 to 2002

In the figure, Ø is the wafer's diameter, and M is the unit for million. The density of DRAM represents the level of integration measured by process improvement, and the generation of microprocessors represents the complexity of the system.

1.2 Roadmap of IC Technology

We have seen the historic development of the IC industry. To predict and plan for the future, the International Technology Roadmap for Semiconductors, known throughout the world as the ITRS, collects and analyses the information from major IC companies,

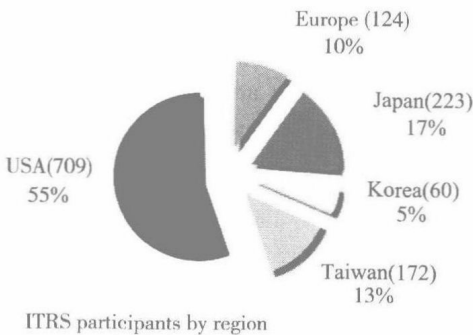


Figure 1-7 ITRS sponsors' contribution distribution

and provides a roadmap of technology milestone targets for the years to come (ITRS, 2009). The ITRS is sponsored by five leading chip manufacturing regions in the world: Europe, Japan, Korea, Taiwan, and USA as shown in Figure 1-7. Specifically, the sponsoring organizations are the European Semiconductor Industry Association (ESIA), the Japan Electronics and Information Technology Industries Association (JEITA), the Korean Semiconductor Industry Association (KSIA), the Taiwan Semiconductor Industry Association

(TSIA), and the United States Semiconductor Industry Association (SIA).

The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuits and the products that employ such devices, thereby continuing the health and success of this industry (ITRS, 2009). Through the cooperative efforts of the global chip manufacturers and equipment suppliers, research communities, and consortia, the roadmap teams identify critical challenges, encourage innovative solutions, and welcome participation from the semiconductor community. These teams are joining with other strategic roadmap efforts, such as electronics and nanotechnology, so that the roadmap effort spans the spectrum of needs from basic research capabilities to product potentials.

The ITRS roadmap has been a major guide for the IC R&D objectives and an information resource (Figure 1-8). For example, the following roadmap from ITRS provides data on half-pitch and gate length (a measurement similar to feature size) for the past twenty years, and prediction of the next fifteen years.

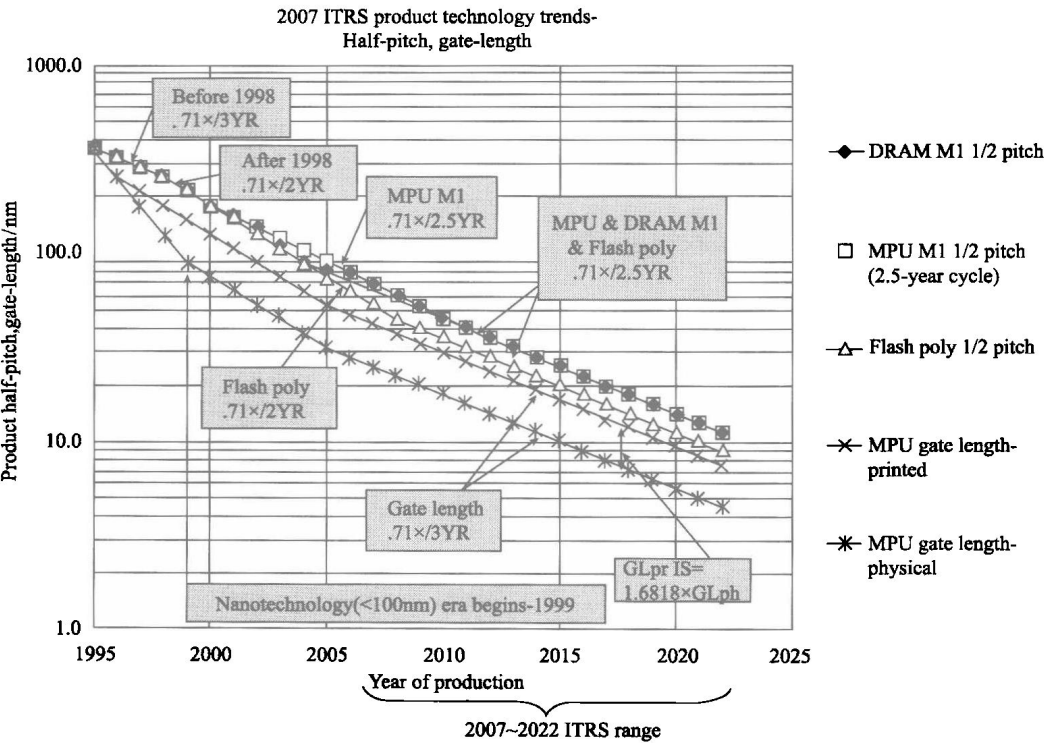


Figure 1-8 Roadmap of product half-pitch and gate length (ITRS, 2009)

To see how accurate the ITRS roadmap is, the following table compares the real historical data and that predicted by the road map. The Table 1-1 shows the historical data of the half-pitch against the ITRS prediction for DRAM products. One can see that the roadmap has predicted this technological trend fairly accurately.

Table 1-1 Roadmap versus actual trend numbers (DRAM product trend example)

Year of production	1995	1998	2000	2002	2003	2004	2006	2007	2009
Calculated trend numbers/nm	360	255	180	127.3	101	90	71.4	63.3	50.5
ITRS rounded numbers/nm	350	250	180	130	100	90	70	65	50
Year of production	2010	2012	2013	2015	2016	2018	2019	2022	
Calculated trend numbers/nm	45	35.7	31.8	25.3	22.5	17.9	15.9	11.3	
ITRS rounded numbers/nm	45	36	32	25	22	18	16	11	

ITRS also provides much more detailed information for specific classes of IC products. As mentioned above such information is very important not only for an IC company, but also for setting up research objectives. For instance, the ITRS roadmap for DRAM is shown in the following Table 1-2.

Table 1-2 DRAM introduction product generations and chip size model

Year of production	2007	2008	2009	2010	2011
DRAM 1/2 pitch (contacted)/nm	65	57	50	45	40
MPU/ASIC metal 1(M1) 1/2 pitch (f)/nm	68	59	52	45	40
MPU physical gate length/nm	25	23	20	18	16
Cell area factor/a	6	6	6	6	6
Cell area [$C_a=af^2$]/ μm^2	0.024	0.019	0.015	0.012	0.0096
Cell array area at introduction (% of chip size) §	73.52%	73.76%	73.97%	74.16%	74.30%
Generation at introduction §	16G	16G	16G	32G	32G
Functions per chip/Gbits	17.18	17.18	34.36	34.36	34.36
Chip size at introduction/ mm^2 §	568	449	711	563	446
Gbits/ cm^2 at introduction §	3.03	3.82	4.83	6.10	7.70
Year of production	2012	2013	2014	2015	
DRAM 1/2 pitch (contacted)/nm	36	32	28	25	
MPU/ASIC metal 1(M1) 1/2 pitch (f)/nm	36	32	28	25	
MPU physical gate length/nm	14	13	11	10	
Cell area factor/a	6	6	6	6	
Cell area [$C_a=af^2$]/ μm^2	0.0077	0.0061	0.0048	0.0038	
Cell array area at introduction (% of chip size) §	74.47%	74.61%	74.70%	74.83%	
Generation at introduction §	32G	64G	64G	64G	
Functions per chip/Gbits	68.72	68.72	68.72	68.72	
Chip size at introduction/ mm^2 §	706	560	444	351	
Gbits/ cm^2 at introduction §	9.73	12.28	15.49	19.55	

Moore's law mainly addresses the level of integration with respect to the number of transistors integrated into a chip and the complexity of the integrated systems. As IC application is extended into every corner of our life, we have begun to look beyond Moore's law. The following Figure 1-9 tries to explore the future from a more com-