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032 系

序号	姓名	职称	单位	论文题目	刊物名称	年卷期	类别
1	阮新波 李斌	教授 博士	032	Zero-Voltage and Zero-Current-Switching PWM Hybrid Full-Bridge Three-Level Converter	IEEE Transctions on Industrial Electronics	2005年52卷 1期	
2	阮新波 陈志英 陈武	教授 博士 博士	032	Zero-Voltage-Switching PWM Hybrid Full-Bridge Three-Level Converter	IEEE Transctions on Power Electronics	2005年20 卷2期	
3	金科 阮新波 刘福鑫	博士 教授 博士	032	Improved Voltage Clamping Scheme for ZVS PWM Three-Level Converter	IEEE Power Electronics Letters	2005年第3卷第1期	
4	王学华 阮新波	博士 教授	032	SPWM控制单相三电平逆变器	中国电机工程学报	2005年第25卷第1期	
5	金科 阮新波	博士 教授	032	改进型ZVS PWM三电平直流变换器	中国电机工程学报	2005年第25卷第4期	
6	旷建军 阮新波 任小永	博士 教授	032	平面变压器中并联绕组的均流设计	中国电机工程学报	2005年第25卷第14期	
7	张之梁 阮新波	硕士 教授	032	零电压开关PWM全桥三电平变换器	中国电机工程学报	2005年第25卷第16期	
8	王建冈 阮新波 吴伟 陈军艳 陈乾宏	博士 教授	032	倒装芯片集成电力电子模块	中国电机工程学报	2005年第25卷第17期	
9	张之梁 阮新波	硕士 教授	032	全桥三电平变换器的一种新型控制策略	中国电机工程学报	2005年第25卷第19期	
10	陈武、 阮新波	硕士 教授	032	加钳位二极管的ZVS PWM复合式全桥三电平变换器	中国电机工程学报	2005年第25卷第20期	
11	刘福鑫 阮新波	博士 教授	032	一种新颖的零电压开关PWM组合式三电平变换器	中国电机工程学报	2005年第25卷第22期	
12	任小永 阮新波	博士 教授	032	适用于高压输入低压输出的两级式变换器	中国电机工程学报	2005年第25卷第23期	
13	章涛 阮新波	硕士 教授	032	输入串联输出并联全桥变换器的均压均流的一种方法	中国电机工程学报	2005年第25卷第24期	
14	王建冈 阮新波 陈军艳	博士 教授	032	航空用大功率模块电源的设计及关键技术应用研究	电工技术学报	2005年第20卷第12期	
15	彭政 阮新波	硕士 教授	032	120W电源适配器的研制	电力电子技术	2005年第39卷第5期	
16	张之梁 阮新波	硕士 教授	032	A Novel Double Phase-Shift Control Scheme for Full-Bridge Three-Level Converter	国际会议 IEEE APEC 2005	2005年3月	
17	陈武 阮新波	硕士 教授	032	Zero-Voltage-Switching PWM Hybrid Full-Bridge Three-Level Converter with Clamping Diodes	国际会议 IEEE PESC 2005	2005年6月	
18	陈武 阮新波	硕士 教授	032	Current-Doubler-Rectifier ZVS PWM Hybrid Full-Bridge Three-Level converter	国际会议 IEEE PESC 2005	2005年6月	
19	金科 阮新波	博士 教授	032	Hybrid Full-Bridge Three-Level LLC Resonant Converter — A Novel DC-DC Converter Suitable for Fuel Cell Power System	国际会议 IEEE PESC 2005	2005年6月	
20	金科 阮新波	博士 教授	032	Control Strategy for Zero-Voltage-Switching Multi-Resonant Three-Level Converters	国际会议 IEEE PESC 2005	2005年6月	
21	李冬 阮新波	博士 教授	032	Comparison of Three Front-end DC-DC Converters for 1200W Server Power Supply	国际会议 IEEE PESC 2005	2005年6月	

22	刘福鑫 阮新波	博士 教授	032	ZVS Hybrid Three-Level Converter With Low Voltage Stress and Reduced Filter	国际会议 IEEE PESC 2005	2005年6月	
23	张之梁 阮新波	硕士 教授	032	Full-bridge Three-Level Converter with the Flying Capactior and Two Clampping Diodes	国际会议 IEEE PESC 2005	2005年6月	
24	王世山	副教授	032	运行中750kV悬挂式避雷器静电场计算及设计优化	南京航空航天大学学报	2005, 37(6): 801-806.	
25	王世山 刘泽远 李彦明	副教授 硕士	032	Calculation of short-circuit impedance for power transformer with coupling FEM method of magnetic field and circuit	Proceedings of the 14th International Symposium on High Voltage Engineering, Tsinghua University, Beijing, China, Aug. 25-29, 2005:20.	Aug. 25-29, 2005:20.	
26	王世山 谢建民	副教授 硕士	032	750kV避雷器阀片电压最大偏差的多变量拟合	高电压技术	2005，31(4):6-8	
27	王世山 何计谋	副教授 硕士	032	悬挂式避雷器离、在线阀片电压偏差差异及均压环优化配置	电瓷避雷器	2005(3):24-28.	
28	王世山 汲胜昌	副教授 硕士	032	计及金属塔和母线效应的悬挂式避雷器电场计算及其结构优化	电工技术学报	2005，20(6):30-34.	
29	张兰红 胡育文 黄文新	博士 教授 副教授	032	基于直接转矩控制技术的异步电机驱动系统两种容错方案研究	南京航空航天大学学报	2005 年 37卷 1 期	
30	张兰红 胡育文 黄文新	博士 教授 副教授	032	异步电机起动/发电系统起动向发电的转换研究	航空学报	2005 年 26卷 3 期	
31	刘陵顺 胡育文 黄文新	博士 教授 副教授	032	电力电子变换器控制的异步电机发电技	电工技术学报	2005 年 20卷 5 期	
32	周扬忠 胡育文 黄文新	博士 教授 副教授	032	阻尼绕组对直接转矩控制同步电机动态行为的影	航空学报	2005 年 26卷 4 期	
33	张兰红 胡育文 黄文新	博士 教授 副教授	032	采用瞬时转矩控制策略的异步发电机系统的容错研	航空学报	2005 年 26卷 5 期	
34	张兰红 胡育文 黄文新	博士 教授 副教授	032	容错型四开关三相变换器异步发电系统直接转矩控制研	中国电机工程学报	2005 年 25卷 18 期	
35	张兰红 胡育文 黄文新	博士 教授 副教授	032	Research on DTC control strategy of induction start/generation	国际会议	2005	
36	李勇 黄文新 胡育文	博士 副教授 教授	032	A low cost implementation of stator-flux-oriented induction motor	国际会议	2005	
37	刘陵顺 胡育文 黄文新	博士 教授 副教授	032	Optimal design of dual stator-winding induction generator with variable speed based on improved genetic	国际会议	2005	
38	高堃 胡育文	博士 教授	032	A newly method for parameters optimization of PMSM based on the variable speed characteristic	国际会议	2005	
39	尹玲玲 胡育文	硕士 教授	032	交流电机变速恒频风力发电技	电气传动	2005 年10卷 期	
40	张兰红 胡育文 黄文新	博士 教授 副教授	032	笼型异步发电机的Saber建	微特电机	2005 年 11卷 期	

41	叶万富 胡育文 黄文新	硕士 教授 副教授	032	基于定子双绕组感应发电机系统容量的仿真研	电机与控制学报	2005 年 19卷 5 期	
42	孙登亚 黄文新 胡育文	硕士 副教授 教授	032	基于新型可旋转变换器的感应电能传输技	电源技术应用	2005 年 18卷 10 期	
43	肖岚	副教授	032	逆变器综合课程设计教学平台的开发	电气电子教学学报	2005年2月，27卷1期	
44	肖岚 叶益青	副教授 硕士生	032	一种新的高频输出零电压开关逆变器	南京航空航天大学学报	2005年6月，37卷3期	
45	肖岚 纪峰	副教授 硕士生	032	级联型逆变器的输出电平研究	电力电子技术	2005年6月：39（3）	
46	肖岚 陈良亮 李睿 严仰光	副教授 博士生 硕士生 教授	032	基于有功和无功环流控制的DC-AC逆变器系统分析与实现	电工技术学报	2005.10，20卷10期	
47	严加根 刘闯	硕士 副教授	032	开关磁阻电机矩角特性研究与应用	电工技术学报	Vol. 20 No. 9	
48	严加根 刘闯	硕士 副教授	032	开关磁阻起动/发电机系统数字控制器的研究	电力电子技术	Vol.39 No.6	
49	刘闯 严加根	副教授 硕士生	032	Investigation and Practice for Basic Theory of Switched Reluctance Generators	ICEMS2005	2005	
50	邢岩 蔡宣三	教授 教授	032	高频功率开关变换技术	机械工业出版社	2005.5	
51	何中一 李明珠 邢岩	博士生 校外 教授	032	Core Techniques of Digital Control for UPS	IEEE International conference on Industrial Technology	2005	
52	孟丽禅 方宇 邢岩	硕士生 博士生 教授	032	Current Sharing Control for Boost PFC Converters in Parallel Operation	IEEE International conference on Industrial Technology	2005	
53	李吉 邢岩廖 颖熙	硕士生 硕士生 教授	032	Research on Variable Low Voltage High Current DC-DC Converter	The Eighth International Conference on Electrical Machines and Systems	2005	
54	孟丽禅 方宇 邢岩 付大丰	硕士生 博士生 教授 讲师	032	Novel Control for Boost PFC Modules in Parallel Operation	The Eighth International Conference on Electrical Machines and Systems	2005	
55	付大丰 邢岩 杨善水	讲师 教授 副教授	032	Electrical Power Distribution System Based on 1553B Bus for Advanced Aircraft	The Eighth International Conference on Electrical Machines and Systems	2005	
56	龚春英	教授	032	推挽式单级电流源高频链逆变拓扑研究	电工技术学报	2005年20卷10期	
57	龚春英	教授	032	单级式静止变流器研究	中国航空学会	2005年	
58	王琪 龚春英	硕士 教授	032	2kW新型推挽正激直流变换器的研制	电源技术应用	2005年8卷1期	
59	孙林 梁永春 龚春英 严仰光	硕士 博士 教授 教授	032	Research on Single-stage Flyback Inverter	36th IEEE PESC	2005年	
60	孙林 梁永春 龚春英	硕士 博士 教授	032	采用同步整流技术的反激逆变器研究	第十六届电源技术年会	2005年	

61	刘伟晗 王琪 龚春英	硕士 硕士 教授	032	双环控制型推挽正激DC-DC变换器的小信号模型	电源世界	2005年第9期	
62	李春燕 陈新 沈忠亭 严仰光	博士 讲师 博士 教授	032	最优PWM开关角的在线计算	南航学报	2005.2，Vol.37 No.1	
63	陈新 谢少军	讲师 教授	032	电力电子技术课程教学与网络建设	第三届全国高校电气工程及其自动化专业教	2005.9.22-25，郑州	
64	陈新 龚春英 谢少军	讲师 教授 教授	032	浅析电力电子技术课程网络化教学平台建设	南航学报社科版	2005.12 Vo.7 No.2	
65	肖庆恩 何礼高	硕士 高工	032	多电平变换器开关管的光纤隔离驱动保护电路	电力电子技术	2005年39卷3期	
66	陈鑫兵 何礼高	硕士 高工	032	三电平逆变器空间矢量过调制控制策略的研究	中国电源技术学术会16届年会	2005年10月深圳	
67	张卓然 陈志辉 杨善水 严仰光	讲师 副教授 副教授 教授	032	基于DSP的飞机高压直流电源数字调压器研究	电力电子技术	2005年39卷 第4期	
68	张卓然 陈志辉 杨善水 严仰光	讲师 副教授 副教授 教授	032	电励磁双凸极电机数字电压调节器的研究与实现	电气应用	2005年24卷 第10期	
69	葛红娟 张绍 周波	副教授 硕士 教授	032	变速恒频电源系统的交-交矩阵变换器闭环控制	南京航空航空大学学报	2005，vol.37,No.3	
70	葛红娟 穆新华 张绍 周波	副教授 副教授 硕士 教授	032	基于矩阵变换器的永磁同步电机矢量控制模型及仿真分析	中国矿业大学学报	2005，vol.34,No.3	
71	葛红娟 穆新华 周波 张绍	副教授 副教授 硕士 教授	032	用于永磁同步电机矢量控制的矩阵变换器新型离散控制技术	电工技术学报	2005，vol.20,No.4	
72	葛红娟	副教授	032	DIGITAL PWM OF AC-AC MATRIX CONVERTER BASED ON OUTPUT-VOLTAGE ERROR FUNCTION	南京航空航空大学学报英文版	2005，vol.22,No.4	
73	Ge-hongjuan Mu-xinhua Zhou-bo Zhang-shao	associate professor	032	A Novel Discrete Control Technique of Matrix Converter for the Vector Control of Permanent Magnet Synchronous Motor	International Electric Machines and Drives Conference（IEMDC 2005）	2005.05.15-18（美国San Antonio）	
74	Ge-hongjuan Mu-xinhua Zhou-bo Zhang-shao	associate professor	032	Implementation of DSP-Based Matrix Converter Permanent Magnetic Synchronous Motor Closed-loop Control System	International Conference on Electrical Machines and Systems（ICEMS 2005）	2005.09.27-29（中国Nanjing）	

75	Zhang-shao Ge-hongjuan Mu-xinhua	Graduated student	032	System Implementation of Voltage-Current Dual Closed loop Control Method of AC-AC Matrix Converter	International Conference on Electrical Machines and Systems（ICEMS 2005）	2005.09.26-29（中国 Nanjing)	
76	林聪智 穆新华	研究生 副教授	032	直升机旋翼试验塔电力拖动系统特性分析与计算	南京航空航空大学	2005，vol. 37, No. 3	
77	穆新华 葛红娟	副教授	032	基于重复控制技术的单相航空静止变流器的研究	航空学报	2005，vol. 26, No. 4	
78	Liao-yingxi Mu-xinhua Ge-hongjuan	Graduated student	032	Stabililty Study and Simulation Analysis on Aircraft Transformer Rectifier Unit (TRU) with Constant Power Load (CPL)	International Conference on Electrical Machines and Systems（ICEMS 2005）	2005.09.27-29（中国 Nanjing)	
79	张方华 严仰光	讲师 教授	032	双向DC-DC变换器的控制模型	中国电机工程学报	2005， 25(11)	
80	张方华 严仰光	讲师 教授	032	高频耦合AC-AC变压器的研究	中国电机工程学报	2005, 25(12)	
81	张方华 严仰光	讲师 教授	032	变压器匝比不同的正反激组合式双向DC-DC变换器	中国电机工程学报	2005, 25(14)	
82	张方华 严仰光	讲师 教授	032	推挽正激移相式双向DC-DC变换器	电工技术学报	2004， 19(12)	
83	张方华 严仰光	讲师 教授	032	直流变压器的研究与实现	电工技术学报	2005,20(7)	
84	张方华 谢少军 曹志亮	讲师 教授 高工	032	电气工程与自动化专业开放实验室的的建设构想	南京航空航天大学学报（社会科学版）	2005，7（1）	
85	朱成花 张方华 严仰光	讲师 讲师 教授	032	A novel split phase dual buck half bridge inverter	Proc. of IEEE Applied Power Electronics Conference and Exposition	2005	
86	刘日宝 陈荣 邓智泉	博士 博士 教授	032	基于TMS320LF2407A的永磁同步电动机伺服系统的研究	电气传动	2005年35 卷 3 期	
87	周远平 王宇 邓智泉	博士 博士 教授	032	基于逆变器开关占空比的定子磁链估计方法	电工技术学报	2005年20卷11期	
88	陈荣 邓智泉 严仰光	学生 教授 教授	032	考虑饱和运行时永磁同步伺服系统速度调节器的设计与调整	电工技术学报	2005年20卷 5期	
89	陈荣 邓智泉 严仰光	学生 教授 教授	032	微分反馈控制在永磁伺服系统中的应用研究	电工技术学报	2005 年20 卷 9期	
90	张宏荃 由文博 邓智泉 严仰光	学生 学生 教授 教授	032	无轴承异步电机的单DSP控制	中小型电机	2005 年32卷 4 期	
91	邓智泉 仇志坚 王晓琳 严仰光	教授 学生 讲师 教授	032	无轴承永磁同步电机的转子磁场定向控制研究	中国电机工程学报	2005年 25 卷 1 期	
92	赵旭生 梅磊 邓智泉 王晓琳	学生 学生 教授 讲师	032	新型永磁偏置磁轴承的不平衡补偿研究	微特电机	2005 年 卷11 期	

93	邓智泉 杨钢 张媛 曹鑫 王晓琳	教授 学生 学生 学生 讲师	032	一种新型的无轴承开关磁阻电机数学模型	中国电机工程学报	2005年25 卷9期	
94	陈荣 邓智泉 严仰光	学生 教授 教授	032	永磁同步伺服系统低速性能研究	电气自动化	2005年27卷 2 期	
95	花燕 林英杰 王晓琳 邓智泉	学生 学生 讲师 教授	032	在电机控制领域中TMS320LF240x DSP的混合编程	电气传动	2005年35卷 6 期	
96	周波 任立立 韦海荣	教授 研究生 研究生	032	基于等效电感方法的电磁式双极电机系统简化控制模型	中国电机工程学报	2005年25卷 14 期	
97	王莉 孟小利 曹小庆 严仰光	副教授 讲师 硕士生 教授	032	气隙对双凸极电励磁发电机特性的影响分析	电工技术学报	2005年20卷 第9期	
98	王莉 孟小利 曹小庆 严仰光	副教授 讲师 硕士生 教授	032	电励磁双凸极发电机的非线性模型	中国电机工程学报	2005年25卷 第10期	
99	严杰 王莉 王志强	硕士生 副教授 硕士生	032	基于Matlab的功率MOSFET建模	电力电子技术	2005年39卷 第3期	
100	王志强 王莉	硕士生 副教授	032	一种新颖的MOSFET驱动电路	电力电子技术	2005年39卷 第1期	
101	王志强 王莉 严杰	硕士生 副教授 硕士生	032	A Soft-Starting and Soft-Off Circuit of DC Solid-State Switch	Proceedings of The Eighth International Conference Electrical Machines and System	2005年9月	
102	王莉 曹小庆 孟小利 严仰光	副教授 硕士生 讲师 教授	032	. A Novel Excitation Control Scheme for Exciting-magnetic Doubly Salient Brushless DC Generator, 2005.9, Nanjing, vol.2:911-14.	Proceedings of The Eighth International Conference Electrical Machines and System	2005, 9	
103	王莉 曹小庆 张卓然 严仰光	副教授, 硕士生, 讲师, 教授	032	. Application of Load Current Forward Compensating in Digital Voltage Regulation for Doubly Salient Brushless DC Generator	PEDS05	2005,11	

Full-bridge Three-Level Converter with the Flying Capactior and Two Clampping Diodes*

Zhiliang Zhang, *Student Member, IEEE* and Xinbo Ruan, *Senior Member, IEEE*
Aero-Power Sci-tech Center
College of Automation Engineering
Nanjing University of Aeronautics and Astronautics
Nanjing, 210016, Jiangsu Province, P. R. China
Phone: 0086-25-84892053, Fax: 0086-25-84893500
E-mail: ruanxb@nuaa.edu.cn

Abstract—This paper proposes a chopping plus phase-shift (CPS) control for the full-bridge (FB) three-level (TL) converter to obtain the following advantages: 1) the main switches suffer only the half of the input voltage; 2) zero-voltage-switching (ZVS) is achieved for the main switches; 3) the converter has two operation modes; 4) the output filter inductance is reduced; 5) the input filter can be reduced. The flying capacitor and the two clamping diodes are analyzed, which are used to avoid the unequal voltage stress of the switches due to the asymmetrical driving of the switches. The operation principle of the FB TL converter is analyzed and verified experimentally.

I. INTRODUCTION

Recently, the three-level (TL) converter has become a very important alternative in the area of high voltage and high-to-medium power conversion because the power switches' voltage stress is only half of the input dc voltage [1]. The derivation of HB TL converter is extended to all the dc-to-dc converters and a family of TL converters is proposed [2].

A zero-voltage and zero-current-switching (ZVZCS) hybrid full-bridge (H-FB) TL converter is proposed in [3]. The switches of the three-level leg sustain only the half of the input voltage, so MOSFETs are suitable for the three-level leg and they can achieve zero-voltage-switching (ZVS). The switches of the two-level leg sustain the input voltage, so IGBTs are suitable for the two-level leg and they can achieve zero-current-switching (ZCS). But the IGBTs of the two-level leg limit the converter's switching frequency, and moreover, the additional diode voltage drop in series with the IGBT results in extra conduction losses.

A ZVS H-FB TL converter is proposed in [4], in which MOSFET is used in the two-level leg to replace the IGBT and its series diode. However, the MOSFET used in the two-level leg suffers the input voltage. In order to reduce the switch's voltage stress of the two-level leg, the full-bridge (FB) TL converter is derived from the H-FB TL converter by substituting the two MOSFETs in series for the single MOSFET of the two-level leg.

The soft-switching techniques including ZVS and ZVZCS for HB TL converters are proposed systematically to reveal the relationship among the different topologies and modulation strategies in [5]. However these soft-switching techniques are based on HB TL topology and need to be extended to the FB TL converter that owns two HB TL legs.

This paper proposes a chopping plus phase-shift (CPS) control for the FB TL converter. The proposed CPS control makes the FB TL converter obtain the following advantages: 1) the main switches suffer only the half of the input voltage; 2) ZVS is achieved for the main switches; 3) the converter has two operation modes; 4) the output filter inductance is reduced; 5) the input filter can be reduced. Furthermore, this paper analyzes the flying capacitor and the two clamping diodes, which are used to avoid the unequal voltage stress of the switches due to the asymmetrical driving of the switches.

II. OPERATION PRINCIPLE

The FB TL converter is shown in Fig. 1. The two TL legs consist of eight switches Q_1-Q_8 (including their body diodes D_1-D_8 and intrinsic capacitors C_1-C_8), freewheeling diodes D_9-D_{10}, clamping diodes D_{11}-D_{12}, voltage divided capacitors C_{d1} and C_{d2}, and the flying capacitor C_{ss1} and C_{ss2}. C_{d1} and C_{d2} are equal and large enough to share the input voltage V_{in} evenly, i.e., $V_{cd1}= V_{cd2}= V_{in}/2$. The output filter inductance is large enough to be treated as a constant current source during a switching period. C_{ss1} and C_{ss2} connect the switching interval of the outer two switches and the inner two switches of the two legs respectively. L_r is the resonant inductance to achieve ZVS of Q_5, Q_6, Q_7 and Q_8.

A. Three-Level Mode (3L-mode)

The key waveforms are shown in Fig. 2. The switching stages analysis of the FB TL converter is similar to that of [4]. Q_2, Q_3, Q_5&Q_6 and Q_7&Q_8 are phase-shifted controlled, i.e., Q_2 and Q_3 are switched out of phase, Q_5, Q_6 are in phase and Q_7, Q_8 are in phase. Q_5&Q_6 are switched out of phase with

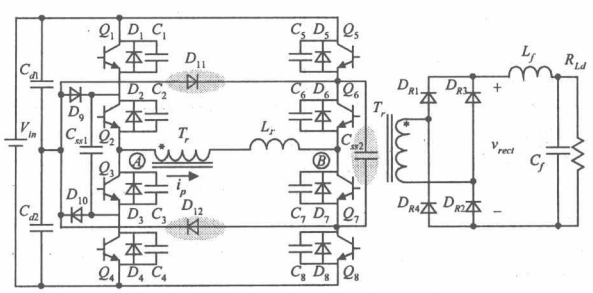

Fig. 1. Full-brdige three-level converter.

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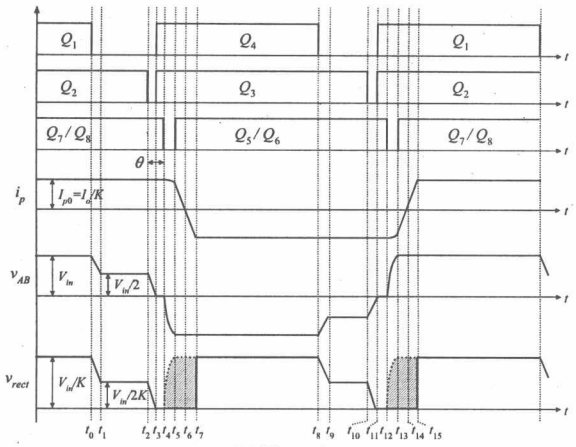
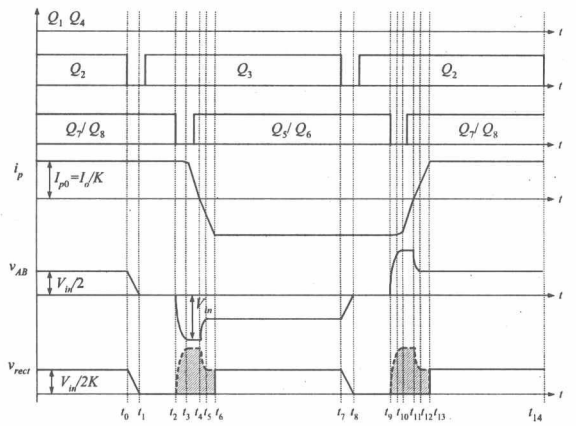


(a) 3L-mode



(b) 2L-mode

Fig. 2. Key waveforms of full-bridge three-level converter.

Q_7&Q_8. Q_2 and Q_3 are switched leading to Q_7&Q_8 and Q_5&Q_6 respectively. So Q_2 and Q_3 are called leading switches, Q_7&Q_8 and Q_5&Q_6 are called lagging switches. A small fixed phase shift θ is set between the leading switches and the lagging switches. Q_1 and Q_4 are PWM controlled corresponding to Q_2 and Q_3 respectively, therefore they are called chopping switches.

When the duty cycle of the chopping switches Q_1 and Q_4 is greater than zero, the secondary rectified voltage is a TL waveform and the output voltage is regulated by control of the duty cycle of the chopping switches, as shown in Fig. 2(a).

B. *Two-Level Mode (2L-mode)*

When the duty cycle of the chopping switches Q_1, Q_4 reduces to zero, the shift-phase between the leading switches and lagging switches will be controlled to regulate the output voltage. The secondary rectified voltage is a two-level waveform, thus the converter operates in 2L-mode as shown in Fig. 2(b).

III. FEATURES AND CHARACTERISTICS

A. *Voltage Stress of the Switches*

The voltage stress of all the main switches is only half of the input voltage under both 3L-mode and 2L-mode.

B. *Realization of ZVS for the Switches*

The energy to realize ZVS for the chopping and leading switches is provided by the output filter inductance, so they can achieve ZVS a wide load range. The energy to realize ZVS for the lagging switches is provided by the resonant inductance, so it is more difficult for the lagging switches to realize ZVS than the chopping and leading switches.

C. *Duty Cycle Loss*

The duty cycle loss D_{loss_3L} under 3L-mode and D_{loss_2L} under 2L-mode can be derived respectively[4],

$$D_{loss\_3L} = \frac{t_{47}}{T_s/2} \approx \frac{t_{57}}{T_s/2} = \frac{4 \cdot L_r \cdot I_o}{K \cdot V_{in} \cdot T_s} \tag{1}$$

$$D_{loss\_2L} = \frac{t_{26}}{T_s/2} \approx \frac{t_{34}+t_{56}}{T_s/2} = \frac{6 \cdot L_r \cdot I_o}{K \cdot V_{in} \cdot T_s} \tag{2}$$

D. *Reduction of the Output Filter Inductance*

Compared to traditional FB converter, the secondary rectified waveforms of FB TL converter have lower high-frequency content under both 3L-mode and 2L-mode. This leads to the significant reduction of the output filter inductance[4].

E. *Reduction of the Input Filter*

It can be seen in Fig. 2(a) and (b) that the rectified i_p is close to the input current of the converter, which has very little ripple. It is nearly a constant dc current source, so the input filter can be also reduced.

IV. FLYING CAPACITOR AND CLAMPING DIODES

For the CPS control, the two series switches in the lagging leg of the FB TL converter need to turn on and turn off simultaneously. However, the tiny asymmetrical driving of the two series switches cannot be avoided in the experimental circuit implementation, which may result in the voltage stress unbalance over the switches. So the flying capacitor and the two clamping diodes are introduced to the FB TL converter.

A. *Turn-Off Delay*

The four cases of turn-off delay are as follows: 1) Q_8 turns off prior to Q_7; 2) Q_7 turns off prior to Q_8; 3) Q_6 turns off prior to Q_5; 4) Q_5 turns off prior to Q_6.

Turn-off delay of Q_8 and turn-off delay of Q_7 are presented respectively. To simply the analysis, the following assumptions are made: 1) Q_5&Q_6 turn on and turn off simultaneously; 2) Q_7&Q_8 turn on simultaneously.

1) *Turn-Off Delay of Q_8*

Fig. 3 shows the waveforms of the turn-off delay of Q_8 during the first half cycle [t_0, t_8]. The equivalent circuits are shown in Fig. 4.

a) Stage 1 [t_4, t_α] [Fig. 4(a)]: At t_4, turn off Q_7, i_p charges C_7 and discharges C_6 via C_{ss2}.

b) Stage 2 [t_α, t_β] [Fig. 4(b)]: At t_α, turn off Q_8, i_p charges C_8 and discharges C_5 via C_{ss2}. Meantime, i_p charges C_7 and

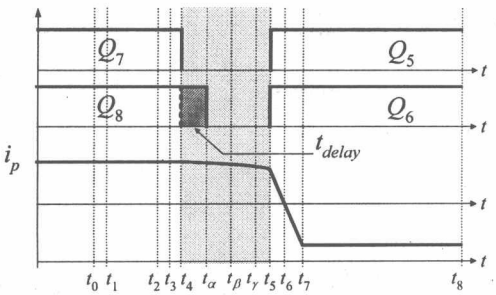
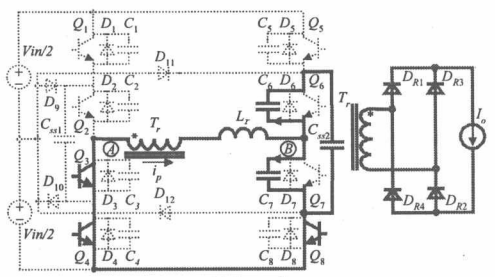
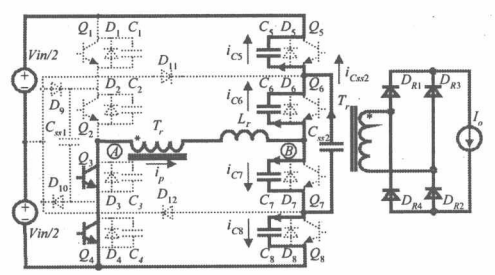


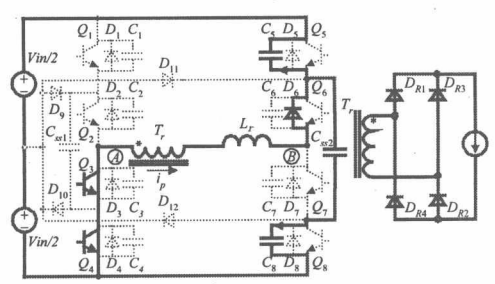
Fig. 3. Waveforms of turn-off delay of Q_8



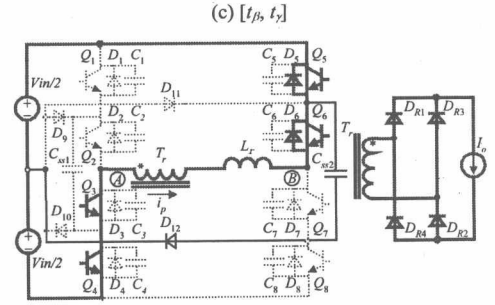
(a) $[t_4, t_\alpha]$



(b) $[t_\alpha, t_\beta]$



(c) $[t_\beta, t_\gamma]$



(d) $[t_\gamma, t_5]$

Fig.4. Equivalent circuits of switching mode of turn-off delay of Q_8

discharges C_6 via C_{ss2}. The energy of C_{ss2} is released, and v_{css2} decays.

$$i_p = i_{c6} + i_{c7} \tag{3}$$

$$i_{c5} = i_{c6} + i_{css2} \tag{4}$$

$$i_{c8} = i_{c7} - i_{css2} \tag{5}$$

From (3), (4) and (5), the following equation is derived

$$i_p = i_{c5} + i_{c8} = i_{c6} + i_{c7} \tag{6}$$

c) Stage 3 $[t_\beta, t_\gamma]$ [Fig. 4(c)]: At t_β, v_{c6} decays to zero, D_6 conducts, Q_6 can be turned on with zero-voltage. i_p continues to charges C_8 and discharges C_5 via C_{ss2}.

d) Stage 4 $[t_\gamma, t_5]$ [Fig. 4(d)]: At t_γ, v_{c5} decays to zero, D_5 conducts, Q_5 can be turned on with zero-voltage. C_{ss2} is charged though D_{12} and the voltage of C_{ss2} is clamped at $V_{in}/2$.

2). Turn-Off Delay of Q_7

Fig. 5 shows the waveforms of the turn-off delay of Q_7 during the first half cycle $[t_0, t_8]$. The equivalent circuits are shown in Fig. 6.

a) Stage 1 $[t_4, t_\alpha]$ [Fig. 6(a)]: At t_4, turn off Q_8, i_p charges C_8 and discharges C_5 via C_{ss2}.

b) Stage 2 $[t_\alpha, t_\beta]$ [Fig. 6(b)]: At t_α, turn off Q_7, i_p charges C_7 and discharges C_6 via C_{ss2}. Meantime, i_p charges C_8 and discharges C_5 via C_{ss2}. The energy of C_{ss2} is released, and v_{css2} decays.

$$i_p = i_{c6} + i_{c7} \tag{7}$$

$$i_{c5} = i_{c6} + i_{css2} \tag{8}$$

$$i_{c8} = i_{c7} - i_{css2} \tag{9}$$

From (7), (8) and (9), the following equation is derived

$$i_p = i_{c5} + i_{c8} = i_{c6} + i_{c7} \tag{10}$$

c) Stage 3 $[t_\beta, t_\gamma]$ [Fig. 6(c)]: At t_β, v_{c5} decays to zero, D_5 conducts, Q_5 can be turned on with zero-voltage. i_p continues to charges C_7 and discharges C_6 via C_{ss2}.

d) Stage 4 $[t_\gamma, t_5]$ [Fig. 6(d)]: At t_γ, v_{c6} decays to zero, D_6 conducts, Q_6 can be turned on with zero-voltage. C_{ss2} is charged though D_{12} and the voltage of C_{ss2} is clamped at $V_{in}/2$.

Other cases of switches' driving unbalance are similar to the above examples. And the voltage stress unbalance of the lagging switches can be avoided owing to the flying capacitor C_{ss2} and the clamping diodes D_{11} and D_{12}.

B. Turn-On Delay

The four cases of turn-on delay are as follows: 1) Q_8 turns on prior to Q_7; 2) Q_7 turns on prior to Q_8; 3) Q_6 turns on prior to Q_5; 4) Q_5 turns on prior to Q_6. When the lagging switches achieve ZVS, the body diodes have conducted, so the switches turn-on delay will not result in the voltage stress unbalance of the switches.

The flying capacitor decouples the charging and discharging procedure of the intrinsic capacitors of the switches. Meanwhile the voltage of the flying capacitor is clamped at half of the input voltage by the clamping diodes,

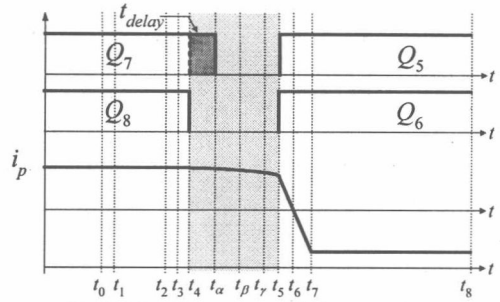
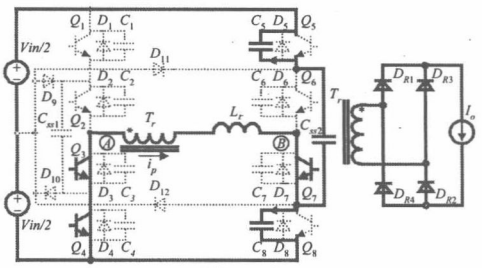
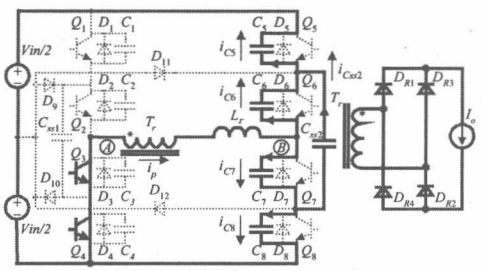


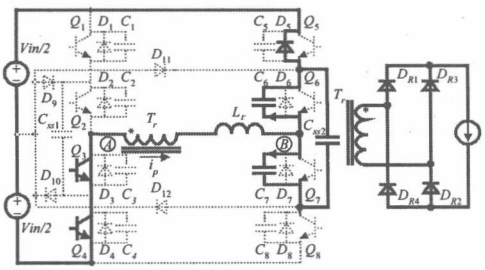
Fig. 5. Waveforms of turn-off delay of Q_7



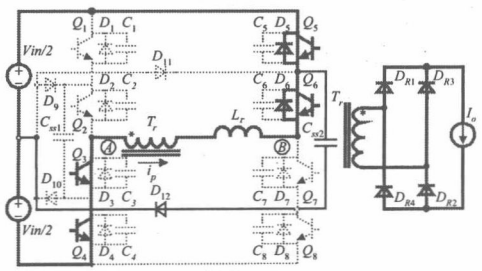
(a) $[t_4, t_\alpha]$



(b) $[t_\alpha, t_\beta]$



(c) $[t_\beta, t_7]$



(d) $[t_7, t_5]$

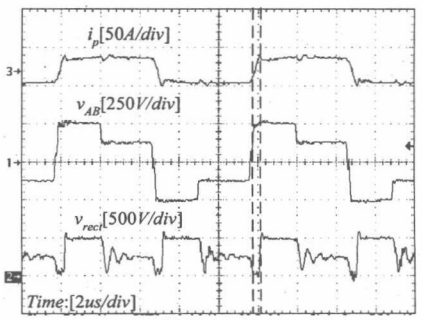
Fig.6. Equivalent circuits of switching mode of turn-off delay of Q_7

thus the unequal voltage stress of the lagging switches due to the asymmetrical driving of can be avoided.

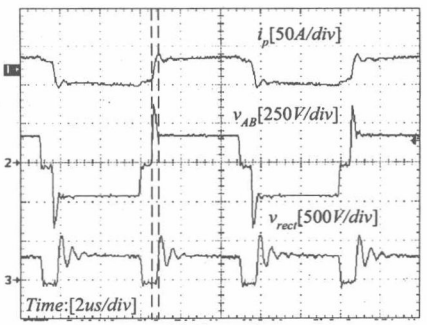
V. EXPERIMENT RESULTS AND DISSCUSSIONS

A prototype converter was built to verify the operation principle. The specifications are as follows: Input voltage: 200-400V; Output voltage: 300V; Rated load current: 10A; Switching frequency: 100kHz; $Q_1(D_1\&C_1)$ -$Q_8(D_8\&C_8)$: IXFH60N25Q; Output filter capacitor: C_f=560uF x2; Flying capacitors C_{ss1}, C_{ss2} =2.2uF; D_9-D_{12}: DSEP30-03; D_{R1}-D_{R4}: SDT12S60; Ratio of primary and secondary windings of transformer: K =7:13; Resonant inductance measured at switching frequency: L_r=1.33uH; Output filter inductance: L_f =144uH; Output filter capacitor C_f=560uFx2.

Fig. 7 shows the experimental results at full load. Fig. 7(a) and (b) show the waveforms of i_p, v_{AB}, and v_{rect} under 3L-mode at V_{in}=260V and 2L-mode at V_{in}=400V respectively. The lower high-frequency content of the rectified voltage leads to the reduction of the output filter inductance. i_p leads to little ripple in the input current, which can reduce the input filter. The duty cycle loss is shown between two dashed lines in Fig. 7(a) and (b) respectively.



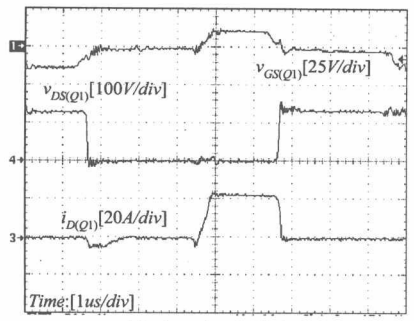
(a) 3L-mode



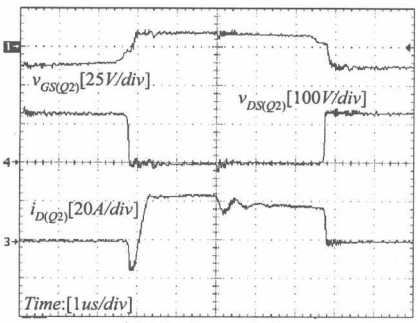
(b) 2L-mode

Fig.7. Experimental waveforms at full load.

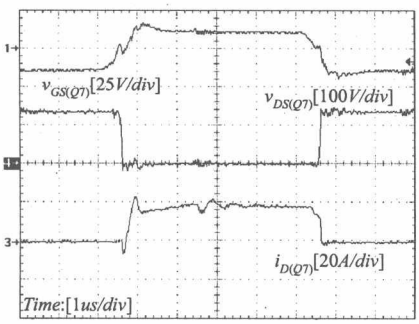
Fig. 8(a) shows the gate drive signal v_{GS}, the voltage across the drain and source v_{DS}, and the drain current i_D of the chopping switch Q_1 under 3L-mode at V_{in}=260V, which indicates that ZVS is achieved for Q_1, and its voltage stress is half of the input voltage. Similarly, ZVS is achieved for Q_2 and Q_7 and their voltage stress is half of the input voltage as shown in Fig. 8(b), (c) and Fig. 9(a), (b).



(a) chopping switch

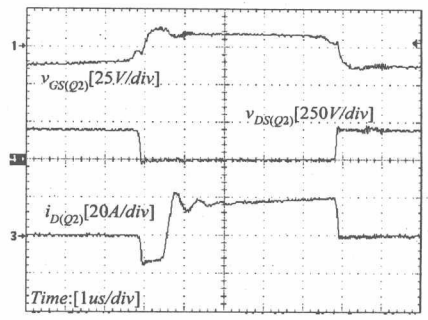


(b) leading switch

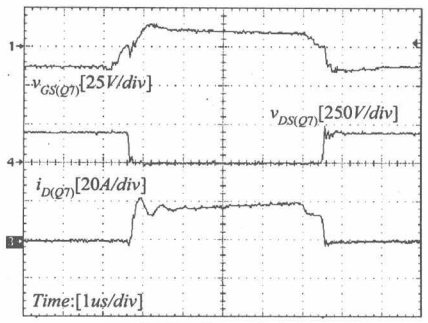


(c) lagging switch

Fig.8. Gate drive signal v_{GS}, voltage across drain and source v_{DS}, and drain current i_D at full load under @V_{in}=260V.

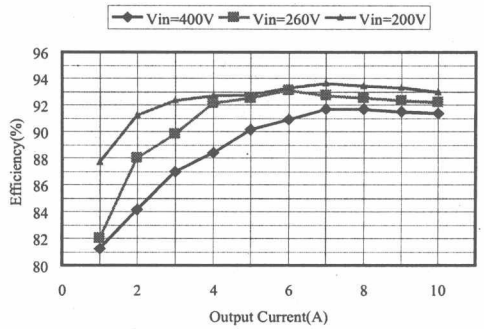


(a) leading switch

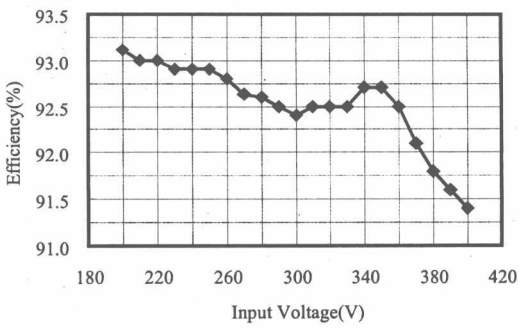


(b) lagging switch

Fig.9. Gate drive signal v_{GS}, voltage across the drain and source v_{DS}, and drain current i_D of switches at full load under 2L-mode@V_{in}=400V.



(a)



(b)

Fig. 10. Conversion efficiency of FB TL converter. (a) conversion efficiency at different load current under the nominal input voltage; (b) conversion efficiency at full load under different input voltage.

Fig. 10(a) gives the conversion efficiency at different load current at V_{in}=200V, V_{in}=260V and V_{in}=400V. Fig. 10(b) shows the efficiency at full load under different input voltage. The higher the input voltage is, the lower efficiency. Under 3L-mode, when v_{AB}= V_{in}/2, the primary current flows through freewheeling diodes D_9 and D_{10} instead of Q_1 and Q_4, which results in higher conduction loss. So when V_{in} increases, the efficiency decreases slightly. Under 2L-mode, there is idle current in the primary side during zero state (when v_{AB}=0), which results in conduction loss in the switches and the primary winding. The higher the input voltage, the longer the zero state is, thus the higher conduction loss and the lower efficiency.

VI. CONCLUSIONS

This paper proposes a CPS control for the FB TL converter, and the flying capacitor and the two clamping diodes are analyzed, which are used to avoid voltage stress unbalance of the lagging switches. The converter has the following advantages:

1) The voltage stress of all the switches is only half of the input voltage, which makes the converter very attractive in high input voltage application;

2) The chopping switches and leading switches can realize ZVS in a wide load range, and the lagging switches can realize ZVS by using of the resonant inductance;

3) The converter has two operation modes (3L-mode and 2L-mode), which makes it adaptive to wide input voltage range;

4) The reduction of the output filter inductance can be achieved due to the superior secondary rectified voltage waveform with lower high frequency content;

5) The input current has little ripple, so the input filter can be reduced.

The operation principle of the FB TL converter is analyzed and verified by a 3kW prototype converter.

REFERENCES

[1] J.R.Pinherio and I.Barbi, "The three-level zvs pwm converter - A new concept in high-voltage dc-to- dc conversion," in Proc. IEEE IECON, 1992, pp.173-178.

[2] X. Ruan, B. Li and Q.Chen, "Three-level converters - A new approach for high volttage and high power dc-to-dc conversion," in Proc. IEEE PESC, 2002, pp.663-668.

[3] X. Ruan and B. Li, "Zero-voltage and zero-current-switching pwm hybrid full-bridge three-level converter," in Proc. IEEE PESC, 2002, pp.1847-1852.

[4] X. Ruan, Z. Chen, W. Chen, "Zero-voltage-switching pwm hybrid full-bridge three-level converter," IEEE Trans. Power Electron., Vol.20, No.2, pp. 395-404, 2005.

[5] X. Ruan, L. Zhou and Y. Yan, "Soft-swithing pwm three-level converters," IEEE Trans. on Power Electron., Vol.16, No.5, 2001, pp.612-622.

Zero-Voltage and Zero-Current-Switching PWM Hybrid Full-Bridge Three-Level Converter

Xinbo Ruan, *Senior Member, IEEE,* and Bin Li

***Abstract*—This paper proposes a zero-voltage and zero-current-switching pulsewidth modulation hybrid full-bridge three-level (ZVZCS PWM H-FB TL) converter, which has a TL leg and a two-level leg. The voltage stress of the switches of the TL leg is half of the input voltage, and the switches can realize ZVS, so MOSFETs can be adopted; the voltage stress of the switches of the two-level leg is the input voltage, and the switches can realize ZCS, so IGBT can be adopted. The secondary rectified voltage is a TL waveform having lower high-frequency content compared with that of the traditional FB converters, which leads to the reduction of the output filter inductance. The input current of the converter has quite little ripple, so the input filter can also be significantly reduced. The operation principle of the proposed converter is analyzed and verified by the experimental results. Several ZVZCS PWM H-FB TL converters are also proposed in this paper.**

***Index Terms*—Full-bridge converter, pulsewidth modulation (PWM), soft-switching, three-level converter.**

I. Introduction

POWER-FACTOR correction (PFC) techniques should be adopted in order to meet the requirements of IEC61000-3-2 class A standard. The output voltage of the three-phase PFC converter is 760–800 V, which raises the stress of the switches of the downstream dc–dc converter. In order to reduce the voltage stress of the switches, a three-level (TL) converter was proposed, where the voltage stress of the switches is half of the input voltage [1]. The soft-switching pulsewidth modulation (PWM) techniques for TL converters are systematically researched in [5]. The concept of leading switches and lagging switches are introduced, and the soft-switching PWM TL converters are classified into two kinds: zero-voltage-switching (ZVS) PWM TL converters and zero-voltage and zero-current-switching (ZVZCS) PWM TL converters.

ZVS PWM TL converters realize ZVS for all switches with the use of the leakage inductance of the transformer and the intrinsic capacitors of the switches. However, the lagging switches will lose ZVS at light load, and the leakage inductance results in duty cycle loss [1]–[3], [6]. ZVZCS PWM TL converters realize ZVS for the leading switches and ZCS for the lagging switches in a wide load range [4], [5]. MOSFETs are used as the leading switches, and insulated gate bipolar transistors (IGBTs) are used as the lagging switches. However, IGBTs with high voltage rating (e.g., 1200 V) are available; their voltage potential could not be exploited enough because the lagging switches (using IGBT) only suffer half of the input voltage.

The above-mentioned TL converter is essentially a half-bridge (HB) converter, and the secondary rectified voltage is a two-level waveform. The converter should be exactly called an HB TL converter.

This paper proposes a ZVZCS PWM hybrid full-bridge (H-FB) TL converter, in which one phase leg is a TL leg and the other is a two-level leg. The switches of TL leg suffer only half of the input voltage, and they can realize ZVS in a wide load range, so metal–oxide–semiconductor field-effect transistors (MOSFETs) can be used. The switches of the two-level leg suffer the input voltage; however, they can realize ZCS in a wide load range, so IGBTs can be used. The characteristics of MOSFETs and IGBTs are sufficiently exploited. Furthermore, the secondary rectified voltage is a TL waveform, which has lower high-frequency content compared with the two-level waveform, and as a result, the output filter inductance can be reduced. The input current of the proposed converter has little ripple, so the input filter can be significantly reduced. The operation principle and parameter design of the proposed converter are analyzed in detail and verified experimentally.

II. Operation Principle

Fig. 1 shows the main circuit and key waveforms of the proposed converter. The TL leg consists of four switches Q_1–Q_4 (including their body diodes D_1–D_4 and intrinsic capacitors C_1–C_4), freewheeling diodes D_7 and D_8, voltage divided capacitors C_{d1} and C_{d2}, and the flying capacitor C_{ss}. C_{d1} and C_{d2} are equal and large enough to share the input voltage $V_{\rm in}$ evenly, i.e., $V_{cd1} = V_{cd2} = V_{\rm in}/2$. C_{ss} connects the switching interval of the outer two switches and the inner two switches respectively. The two-level leg consists of two switches Q_5 and Q_6 and their series diodes D_5 and D_6. D_5 and D_6 make Q_5 and Q_6 only conduct in the positive direction, respectively. $L_{\rm lk}$ is the leakage inductance of the transformer. C_b is the blocking capacitor to make the primary current reduce to zero to achieve ZCS for Q_5 and Q_6.

Q_2, Q_3, Q_5, and Q_6 are phase-shifted controlled, i.e., Q_2 and Q_3 are switched out of phase and Q_5 and Q_6 are switched out of phase, and Q_2 and Q_3 are switched leading to Q_6 and Q_5, respectively. So Q_2 and Q_3 are called leading switches and Q_5

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X. Ruan is with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: ruanxb@nuaa.edu.cn).

B. Li is with the Bel Power (Hangzhou) Company, Ltd., Hangzhou 310053, China (e-mail: bli@belfuse.com).

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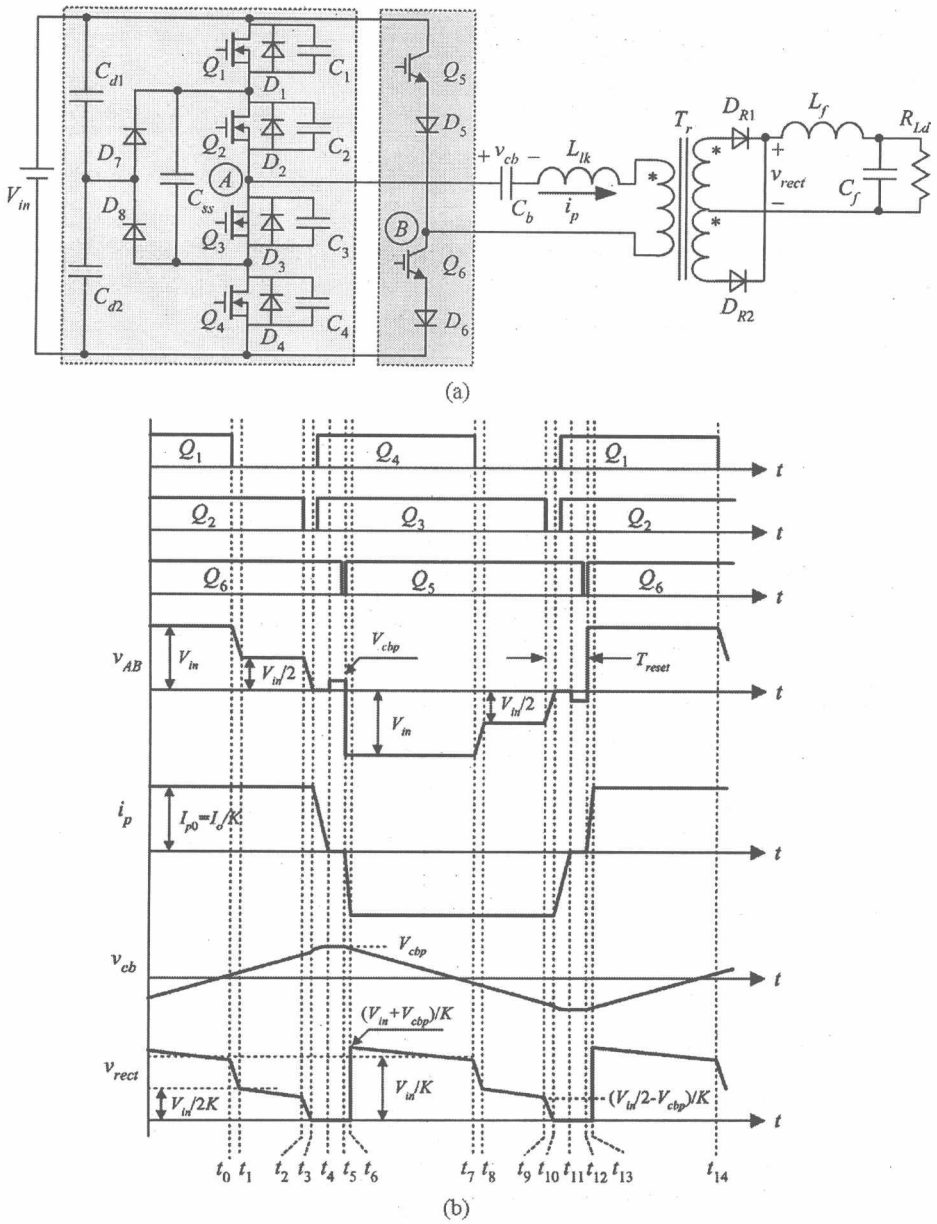

Fig. 1. ZVZCS PWM hybrid full-bridge TL converter. (a) Main circuit. (b) Key waveforms.

and Q_6 are called lagging switches as well. Q_1 and Q_4 are PWM controlled corresponding to Q_2 and Q_3, respectively, so they are called chopping switches. When the duty cycle of the chopping switches is greater than zero, the shift-phase between the leading switches and lagging switches is set at a minimum value to make the primary current reset to ensure ZCS for the lagging switches. Once the duty cycle of the chopping switches reduces to zero, the shift-phase will be regulated to regulate the output voltage.

There are 14 switching modes in a switching period. The equivalent circuits are shown in Fig. 2. Before the analysis, we make the following assumptions.

1) All power devices and diodes are ideal.
2) All capacitors and inductances are ideal.
3) $C_1 = C_2 = C_3 = C_4 = C_r$.
4) The divided capacitors C_{d1} and C_{d2} are large enough to be treated as two voltage sources with value of $V_{\rm in}/2$.
5) The flying capacitor C_{ss} is large enough to be treated as a voltage source with value of $V_{\rm in}/2$.
6) The output filter inductance is large enough to be treated as a constant current source during a switching period.

A. Mode 0 [at t_0] [Fig. 2(a)]

At t_0, Q_1, Q_2, and Q_6 are conducting and $v_{AB} = V_{\rm in}$. D_{R1} is conducting and D_{R2} is off. The primary current i_p charges the blocking capacitor C_b. The primary current is $I_{p0} = I_o/K$, where I_o is the output current and K is the ratio of the primary and secondary windings of the transformer. The voltage of C_b is $V_{cb}(t_0)$.

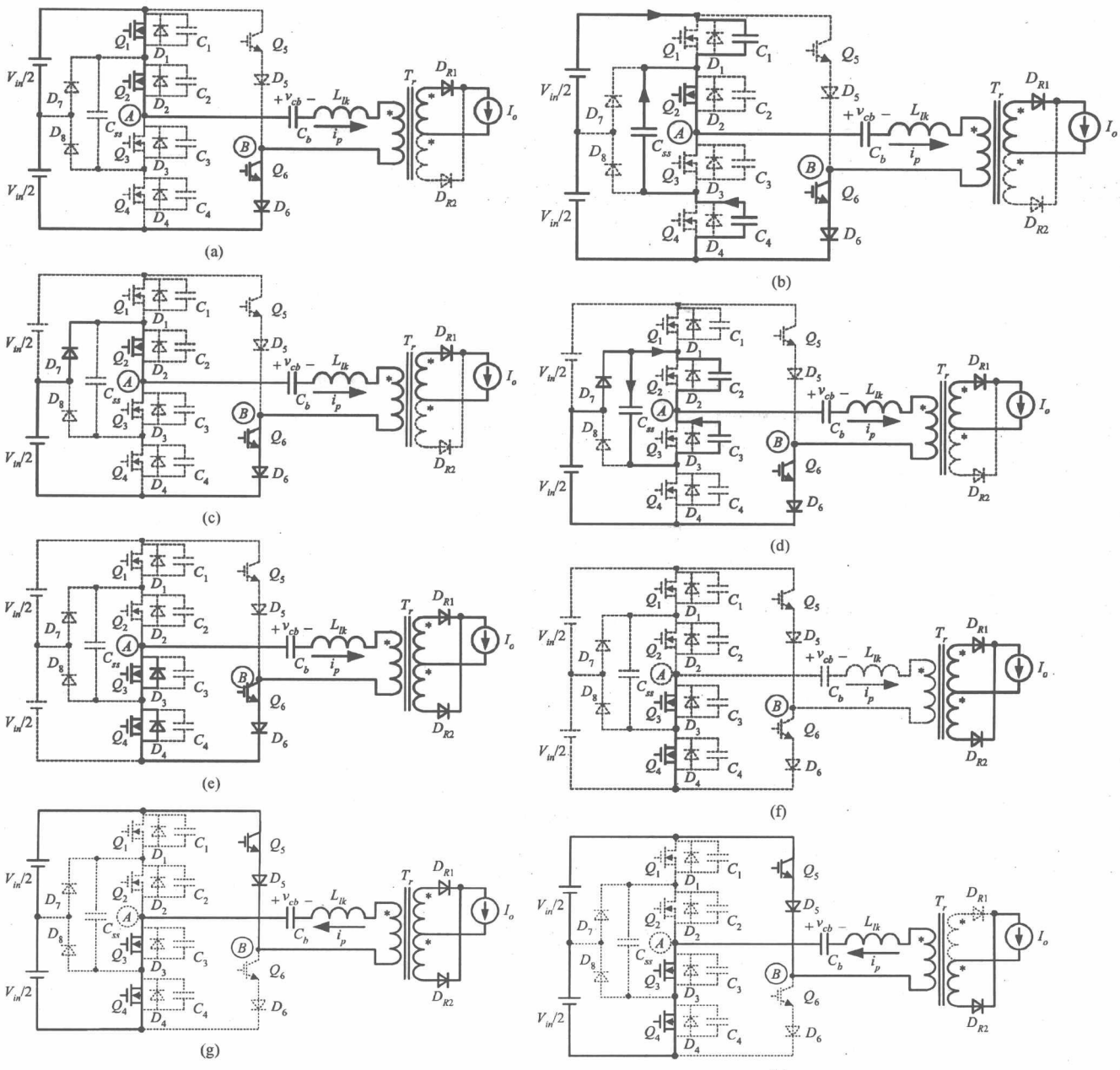

Fig. 2. Equivalent circuits of the switching modes at (a) t_0, (b) $[t_0, t_1]$, (c) $[t_1, t_2]$, (d) $[t_2, t_3]$, (e) $[t_3, t_4]$, (f) $[t_4, t_5]$, (g) $[t_5, t_6]$, and (h) $[t_6, t_7]$.

B. Mode 1 $[t_0, t_1]$ [Fig. 2(b)]

At t_0, turn off Q_1, i_p charges C_1 and discharges C_4 via C_{ss}. As C_1 and C_4 limit the rise rate of the voltage of C_1, Q_1 is zero-voltage turnoff. During this mode L_{lk} is in series with L_f. L_f is large enough to be treated as a constant current source so that i_p keeps the value $I_{p0} = I_o/K$. i_p continues charging C_b. The voltage C_1 rises linearly and the voltage of C_4 decays linearly

$$v_{c1}(t) = \frac{I_{p0}}{2C_r}(t - t_0) \tag{1}$$

$$v_{c4}(t) = \frac{V_{\text{in}}}{2} - \frac{I_{p0}}{2C_r}(t - t_0). \tag{2}$$

At t_1, v_{c1} rises to $V_{\text{in}}/2$ and v_{c4} decays to zero, the voltage potential of A is $V_{\text{in}}/2$, and D_7 conducts naturally. The interval of mode 1 is

$$t_{01} = \frac{C_r V_{\text{in}}}{I_{p0}}. \tag{3}$$

C. Mode 2 $[t_1, t_2]$ [Fig. 2(c)]

D_7 conducts, $v_{AB} = V_{\text{in}}/2$, and i_p continues charging C_b. As the voltage of C_{ss} is $V_{\text{in}}/2$, the voltage across Q_4 is clamped at zero.