国外电子与通信教材系列

PEARSON

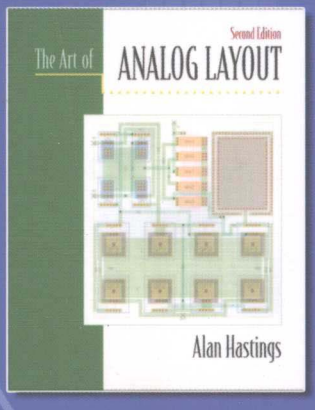
英文版

模拟电路版图的艺术

（第二版）

The Art of Analog Layout

Second Edition



[美] Alan Hastings 著

電子工業出版社
PUBLISHING HOUSE OF ELECTRONICS INDUSTRY
http://www.phei.com.cn

国外电子与通信教材系列

模拟电路版图的艺术

（第二版）

（英文版）

The Art of Analog Layout

Second Edition

［美］Alan Hastings 著

電子工業出版社
Publishing House of Electronics Industry
北京 · BEIJING

内容简介

作者Alan Hastings具有渊博的集成电路版图设计知识和丰富的实践经验。本书以实用和权威性的观点全面论述了模拟集成电路版图设计中所涉及的各种问题及目前的最新研究成果。书中介绍了半导体器件物理与工艺、失效机理等内容；基于模拟集成电路设计所采用的3种基本工艺：标准双极工艺、多晶硅栅CMOS工艺和模拟BiCMOS工艺，重点探讨了无源器件的设计与匹配性问题，二极管设计，双极型晶体管和场效应晶体管的设计与应用，以及某些专门领域的内容，包括器件合并、保护环、焊盘制作、单层连接、ESD结构等；最后介绍了有关芯片版图的布局布线知识。本书可作为相关专业高年级本科生和研究生教材，对于专业版图设计人员也是一本极具价值的参考书。

图书在版编目（CIP）数据

模拟电路版图的艺术：第2版：英文/（美）黑斯廷斯（Hastings, A.）著；
北京：电子工业出版社，2013.1
国外电子与通信教材系列
书名原文：The Art of Analog Layout, Second Edition
ISBN 978-7-121-18674-5
Ⅰ.①模… ·Ⅱ.①黑… Ⅲ.①模拟电路－电路设计－高等学校－教材－英文 Ⅳ.①TN710.02

中国版本图书馆CIP数据核字（2012）第238113号

策划编辑：马　岚
责任编辑：马　岚
印　　刷：三河市鑫金马印装有限公司
装　　订：三河市鑫金马印装有限公司
出版发行：电子工业出版社
　　北京市海淀区万寿路173信箱　邮编：100036
开　　本：787 × 1092　1/16　　印张：41.25　　字数：1373千字
印　　次：2013年1月第1次印刷
定　　价：79.00元

凡所购买电子工业出版社的图书有缺损问题，请向购买书店调换；若书店售缺，请与本社发行部联系。联系及邮购电话：（010）88254888。
质量投诉请发邮件至zlts@phei.com.cn，盗版侵权举报请发邮件至dbqq@phei.com.cn。
服务热线：（010）88258888。

Preface to the Second Edition

I originally wrote *The Art of Analog Layout* as a companion volume to a series of lectures. Many people encouraged me to publish it. At first I was reluctant to do so, for I thought that it would find a rather limited audience. Publication has proven my concerns quite unfounded. To my astonishment, *The Art of Analog Layout* has even been translated into Chinese!

The passage of several years has alerted me to the limitations of the first edition and prompted an extensive revision. Every chapter has been examined and corrected. Many new passages have been added, along with some 50 new illustrations to accompany them. New topics introduced in the second edition include the following:

- Advanced metallization systems
- Dielectric isolation
- Failure mechanisms of MOS transistors
- Integrated inductors
- MOS safe operating area
- Nonvolatile memory

In preparing this edition, I have drawn extensively upon the experience and wisdom of my colleagues at Texas Instruments. I have also made constant reference to the resources available upon the IEEE Xplore website, most particularly those contained in the *IEEE Journal of Electron Devices*. I thank all the many people who have contributed to my own understanding or who have corrected my many mistakes. A work of this length and magnitude will never prove perfect, but the second edition greatly improves upon the first.

ALAN HASTINGS

Acknowledgments

The information contained in this text has been gathered through the hard work of many scientists, engineers, and technicians, the vast majority of whom must remain unacknowledged because their work has not been published. I have included references to as many fundamental discoveries and principles as I could, but in many cases I have been unable to determine original sources.

I thank my colleagues at Texas Instruments for numerous suggestions. I am especially grateful to Ken Bell, Walter Bucksch, Taylor Efland, Lou Hutter, Clif Jones, Alec Morton, Jeff Smith, Fred Trafton, and Joe Trogolo, all of whom have provided important information for this text. I am also grateful for the encouragement of Bob Borden, Nicolas Salamina, and Ming Chiang, without which this book would never have been written.

Preface to the First Edition

An integrated circuit reveals its true appearance only under high magnification. The intricate tangle of microscopic wires covering its surface and the equally intricate patterns of doped silicon beneath it, all follow a set of blueprints called a *layout*. The process of constructing layouts for analog and mixed-signal integrated circuits has stubbornly defied all attempts at automation. The shape and placement of every polygon requires a thorough understanding of the principles of device physics, semiconductor fabrication, and circuit theory. Despite 30 years of research, much remains uncertain. What information there is lies buried in obscure journal articles and unpublished manuscripts. This textbook assembles that information between a single set of covers. While primarily intended for use by practicing layout designers, it should also prove valuable to circuit designers who desire a better understanding of the relationship between circuits and layouts.

The text has been written for a broad audience, some of whom have had only limited exposure to higher mathematics and solid-state physics. The amount of mathematics has been kept to an absolute minimum, and care has been taken to identify all variables and to use the most accessible units. The reader need only have a familiarity with basic algebra and elementary electronics. Many of the exercises assume that the reader also has access to layout editing software; but those who lack such resources can complete many of the exercises with pencil and paper.

The text consists of 14 chapters and five appendices. The first two chapters provide an overview of device physics and semiconductor processing. These chapters avoid mathematical derivations and instead emphasize simple verbal explanations and visual models. The third chapter presents three archetypal processes: standard bipolar, silicon-gate CMOS, and analog BiCMOS. The presentation focuses upon development of cross sections and the correlation of these cross sections to conventional layout views of sample devices. The fourth chapter covers common failure mechanisms and emphasizes the role of layout in determining reliability. Chapters 5 and 6 cover the layout of resistors and capacitors. Chapter 7 presents the principles of matching, using resistors and capacitors as examples. Chapters 8 through 10 cover the layout of bipolar devices, while Chapters 11 and 12 cover the layout and matching of field-effect transistors. Chapters 13 and 14 cover a variety of advanced topics, including device mergers, guard rings, ESD protection structures, and floorplanning. The appendices include a list of acronyms, a discussion of Miller indices, sample layout rules for use in working the exercises, and the derivation of formulas used in the text.

ALAN HASTINGS

Contents

1 *Device Physics 1*

1.1 Semiconductors 1
- 1.1.1. Generation and Recombination 4
- 1.1.2. Extrinsic Semiconductors 6
- 1.1.3. Diffusion and Drift 9

1.2 PN Junctions 11
- 1.2.1. Depletion Regions 11
- 1.2.2. PN Diodes 13
- 1.2.3. Schottky Diodes 16
- 1.2.4. Zener Diodes 18
- 1.2.5. Ohmic Contacts 19

1.3 Bipolar Junction Transistors 21
- 1.3.1. Beta 23
- 1.3.2. I-V Characteristics 24

1.4 MOS Transistors 25
- 1.4.1. Threshold Voltage 27
- 1.4.2. I-V Characteristics 29

1.5 JFET Transistors 32

1.6 Summary 34

1.7 Exercises 35

2 *Semiconductor Fabrication 37*

2.1 Silicon Manufacture 37
- 2.1.1. Crystal Growth 38
- 2.1.2. Wafer Manufacturing 39
- 2.1.3. The Crystal Structure of Silicon 39

2.2 Photolithography 41
- 2.2.1. Photoresists 41
- 2.2.2. Photomasks and Reticles 42
- 2.2.3. Patterning 43

2.3 Oxide Growth and Removal 43
- 2.3.1. Oxide Growth and Deposition 44
- 2.3.2. Oxide Removal 45
- 2.3.3. Other Effects of Oxide Growth and Removal 47
- 2.3.4. Local Oxidation of Silicon (LOCOS) 49

2.4 Diffusion and Ion Implantation 50
- 2.4.1. Diffusion 51
- 2.4.2. Other Effects of Diffusion 53
- 2.4.3. Ion Implantation 55

2.5 Silicon Deposition and Etching 57
- 2.5.1. Epitaxy 57
- 2.5.2. Polysilicon Deposition 59
- 2.5.3. Dielectric Isolation 60

2.6 Metallization 62
- 2.6.1. Deposition and Removal of Aluminum 63
- 2.6.2. Refractory Barrier Metal 65
- 2.6.3. Silicidation 67
- 2.6.4. Interlevel Oxide, Interlevel Nitride, and Protective Overcoat 69
- 2.6.5. Copper Metallization 71

2.7 Assembly 73
- 2.7.1. Mount and Bond 74
- 2.7.2. Packaging 77

2.8 Summary 78

2.9 Exercises 78

3 *Representative Processes 80*

3.1 Standard Bipolar 81
- 3.1.1. Essential Features 81

3.1.2. Fabrication Sequence 82
Starting Material 82
N-Buried Layer 82
Epitaxial Growth 83
Isolation Diffusion 83
Deep-N+ 83
Base Implant 84
Emitter Diffusion 84
Contact 85
Metallization 85
Protective Overcoat 86
3.1.3. Available Devices 86
NPN Transistors 86
PNP Transistors 88
Resistors 90
Capacitors 92
3.1.4. Process Extensions 93
Up-Down Isolation 93
Double-Level Metal 94
Schottky Diodes 94
High-Sheet Resistors 94
Super-Beta Transistors 96
3.2 Polysilicon-Gate CMOS 96
3.2.1. Essential Features 97
3.2.2. Fabrication Sequence 98
Starting Material 98
Epitaxial Growth 98
N-Well Diffusion 98
Inverse Moat 99
Channel Stop Implants 100
LOCOS Processing and Dummy Gate Oxidation 100
Threshold Adjust 101
Polysilicon Deposition and Patterning 102
Source/Drain Implants 102
Contacts 103
Metallization 103
Protective Overcoat 103
3.2.3. Available Devices 104
NMOS Transistors 104
PMOS Transistors 106
Substrate PNP Transistors 107
Resistors 107
Capacitors 109
3.2.4. Process Extensions 109
Double-Level Metal 110
Shallow Trench Isolation 110
Silicidation 111
Lightly Doped Drain (LDD) Transistors 112
Extended-Drain, High-Voltage Transistors 113
3.3 Analog BiCMOS 114
3.3.1. Essential Features 115
3.3.2. Fabrication Sequence 116
Starting Material 116
N-Buried Layer 116
Epitaxial Growth 117
N-Well Diffusion and Deep-N+ 117
Base Implant 118
Inverse Moat 118
Channel Stop Implants 119
LOCOS Processing and Dummy Gate Oxidation 119
Threshold Adjust 119
Polysilicon Deposition and Pattern 120
Source/Drain Implants 120

Metallization and Protective Overcoat 120
Process Comparison 121
3.3.3. Available Devices 121
NPN Transistors 121
PNP Transistors 123
Resistors 125
3.3.4. Process Extensions 125
Advanced Metal Systems 126
Dielectric Isolation 126
3.4 Summary 130
3.5 Exercises 131

4 *Failure Mechanisms 133*
4.1 Electrical Overstress 133
4.1.1. Electrostatic Discharge (ESD) 134
Effects 135
Preventative Measures 135
4.1.2. Electromigration 136
Effects 136
Preventative Measures 137
4.1.3. Dielectric Breakdown 138
Effects 138
Preventative Measures 139
4.1.4. The Antenna Effect 141
Effects 141
Preventative Measures 142
4.2 Contamination 143
4.2.1. Dry Corrosion 144
Effects 144
Preventative Measures 145
4.2.2. Mobile Ion Contamination 145
Effects 145
Preventative Measures 146
4.3 Surface Effects 148
4.3.1. Hot Carrier Injection 148
Effects 148
Preventative Measures 150
4.3.2. Zener Walkout 151
Effects 151
Preventative Measures 152
4.3.3. Avalanche-Induced Beta Degradation 153
Effects 153
Preventative Measures 154
4.3.4. Negative Bias Temperature Instability 154
Effects 155
Preventative Measures 155
4.3.5. Parasitic Channels and Charge Spreading 156
Effects 156
Preventative Measures (Standard Bipolar) 159
Preventative Measures (CMOS and BiCMOS) 162
4.4 Parasitics 164
4.4.1. Substrate Debiasing 165
Effects 166
Preventative Measures 167
4.4.2. Minority-Carrier Injection 169
Effects 169
Preventative Measures (Substrate Injection) 172
Preventative Measures (Cross-Injection) 178
4.4.3. Substrate Influence 180
Effects 180
Preventative Measures 180

4.5 Summary 183
4.6 Exercises 183

5 *Resistors 185*
5.1 Resistivity and Sheet Resistance 185
5.2 Resistor Layout 187
5.3 Resistor Variability 191
5.3.1. Process Variation 191
5.3.2. Temperature Variation 192
5.3.3. Nonlinearity 193
5.3.4. Contact Resistance 196
5.4 Resistor Parasitics 197
5.5 Comparison of Available Resistors 200
5.5.1. Base Resistors 200
5.5.2. Emitter Resistors 201
5.5.3. Base Pinch Resistors 202
5.5.4. High-Sheet Resistors 202
5.5.5. Epi Pinch Resistors 205
5.5.6. Metal Resistors 206
5.5.7. Poly Resistors 208
5.5.8. NSD and PSD Resistors 211
5.5.9. N-Well Resistors 211
5.5.10. Thin-Film Resistors 212
5.6 Adjusting Resistor Values 213
5.6.1. Tweaking Resistors 213
Sliding Contacts 214
Sliding Heads 215
Trombone Slides 215
Metal Options 215
5.6.2. Trimming Resistors 216
Fuses 216
Zener Zaps 219
EPROM Trims 221
Laser Trims 222
5.7 Summary 223
5.8 Exercises 224

6 *Capacitors and Inductors 226*
6.1 Capacitance 226
6.1.1. Capacitor Variability 232
Process Variation 232
Voltage Modulation and Temperature Variation 233
6.1.2. Capacitor Parasitics 235
6.1.3. Comparison of Available Capacitors 237
Base-Emitter Junction Capacitors 237
MOS Capacitors 239
Poly-Poly Capacitors 241
Stack Capacitors 243
Lateral Flux Capacitors 245
High-Permittivity Capacitors 246
6.2 Inductance 246
6.2.1. Inductor Parasitics 248
6.2.2. Inductor Construction 250
Guidelines for Integrating Inductors 251
6.3 Summary 252
6.4 Exercises 253

7 *Matching of Resistors and Capacitors 254*
7.1 Measuring Mismatch 254

7.2 Causes of Mismatch 257
7.2.1. Random *Variation* 257
Capacitors 258
Resistors 258
7.2.2. Process Biases 260
7.2.3. Interconnection Parasitics 261
7.2.4. Pattern Shift 263
7.2.5. Etch Rate Variations 265
7.2.6. Photolithographic Effects 267
7.2.7. Diffusion Interactions 268
7.2.8. Hydrogenation 270
7.2.9. Mechanical Stress and Package Shift 271
7.2.10. Stress Gradients 274
Piezoresistivity 274
Gradients and Centroids 275
Common-Centroid Layout 277
Location and Orientation 281
7.2.11. Temperature Gradients and Thermoelectrics 283
Thermal Gradients 285
Thermoelectric Effects 287
7.2.12. Electrostatic Interactions 288
Voltage Modulation 288
Charge Spreading 292
Dielectric Polarization 293
Dielectric Relaxation 294
7.3 Rules for Device Matching 295
7.3.1. Rules for Resistor Matching 296
7.3.2. Rules for Capacitor Matching 300
7.4 Summary 303
7.5 Exercises 304

8 *Bipolar Transistors 306*
8.1 Topics in Bipolar Transistor Operation 306
8.1.1. Beta Rolloff 308
8.1.2. Avalanche Breakdown 308
8.1.3. Thermal Runaway and Secondary Breakdown 310
8.1.4. Saturation in NPN Transistors 312
8.1.5. Saturation in Lateral PNP Transistors 315
8.1.6. Parasitics of Bipolar Transistors 318
8.2 Standard Bipolar Small-Signal Transistors 320
8.2.1. The Standard Bipolar NPN Transistor 320
Construction of Small-Signal NPN Transistors 322
8.2.2. The Standard Bipolar Substrate PNP Transistor 326
Construction of Small-Signal Substrate PNP Transistors 328
8.2.3. The Standard Bipolar Lateral PNP Transistor 330
Construction of Small-Signal Lateral PNP Transistors 332
8.2.4. High-Voltage Bipolar Transistors 337
8.2.5. Super-Beta NPN Transistors 340
8.3 CMOS and BiCMOS Small-Signal Bipolar Transistors 341
8.3.1. CMOS PNP Transistors 341
8.3.2. Shallow-Well Transistors 345
8.3.3. Analog BiCMOS Bipolar Transistors 347
8.3.4. Fast Bipolar Transistors 349
8.3.5. Polysilicon-Emitter Transistors 351
8.3.6. Oxide-Isolated Transistors 354
8.3.7. Silicon-Germanium Transistors 356
8.4 Summary 358
8.5 Exercises 358

9 *Applications of Bipolar Transistors 360*
9.1 Power Bipolar Transistors 361

9.1.1. Failure Mechanisms of NPN Power Transistors 362
Emitter Debiasing 362
Thermal Runaway and Secondary Breakdown 364
Kirk Effect 366
9.1.2. Layout of Power NPN Transistors 368
The Interdigitated-Emitter Transistor 369
The Wide-Emitter Narrow-Contact Transistor 371
The Christmas-Tree Device 372
The Cruciform-Emitter Transistor 373
Power Transistor Layout in Analog BiCMOS 374
Selecting a Power Transistor Layout 376
9.1.3. Power PNP Transistors 376
9.1.4. Saturation Detection and Limiting 378
9.2 Matching Bipolar Transistors 381
9.2.1. Random Variations 382
9.2.2. Emitter Degeneration 384
9.2.3. NBL Shadow 386
9.2.4. Thermal Gradients 387
9.2.5. Stress Gradients 391
9.2.6. Filler-Induced Stress 393
9.2.7. Other Causes of Systomatic Mismatch 395
9.3 Rules for Bipolar Transistor Matching 396
9.3.1. Rules for Matching Vertical Transistors 397
9.3.2. Rules for Matching Lateral Transistors 402
9.4 Summary 402
9.5 Exercises 403

10 *Diodes 406*
10.1 Diodes in Standard Bipolar 406
10.1.1. Diode-Connected Transistors 406
10.1.2. Zener Diodes 409
Surface Zener Diodes 410
Buried Zeners 412
10.1.3. Schottky Diodes 415
10.1.4. Power Diodes 420
10.2 Diodes in CMOS and BiCMOS Processes 422
10.2.1. CMOS Junction Diodes 422
10.2.2. CMOS and BiCMOS Schottky Diodes 423
10.3 Matching Diodes 425
10.3.1. Matching PN Junction Diodes 425
10.3.2. Matching Zener Diodes 426
10.3.3. Matching Schottky Diodes 428
10.4 Summary 428
10.5 Exercises 429

11 *Field-Effect Transistors 430*
11.1 Topics in MOS Transistor Operation 431
11.1.1. Modeling the MOS Transistor 431
Device Transconductance 432
Threshold Voltage 434
11.1.2. Parasitics of MOS Transistors 438
Breakdown Mechanisms 440
CMOS Latchup 442
Leakage Mechanisms 443
11.2 Constructing CMOS Transistors 446
11.2.1. Coding the MOS Transistor 447
Width and Length 448
11.2.2. N-Well and P-Well Processes 449
11.2.3. Channel Stop Implants 452
11.2.4. Threshold Adjust Implants 453
11.2.5. Scaling the Transistor 456

11.2.6. Variant Structures 459
Serpentine Transistors 461
Annular Transistors 462
11.2.7. Backgate Contacts 464
11.3 Floating-Gate Transistors 467
11.3.1. Principles of Floating-Gate Transistor Operation 469
11.3.2. Single-Poly EEPROM Memory 472
11.4 The JFET Transistor 474
11.4.1. Modeling the JFET 474
11.4.2. JFET Layout 476
11.5 Summary 479
11.6 Exercises 479

12 *Applications of MOS Transistors 482*
12.1 Extended-Voltage Transistors 482
12.1.1. LDD and DDD Transistors 483
12.1.2. Extended-Drain Transistors 486
Extended-Drain NMOS Transistors 487
Extended-Drain PMOS Transistors 488
12.1.3. Multiple Gate Oxides 489
12.2 Power MOS Transistors 491
12.2.1. MOS Safe Operating Area 492
Electrical SOA 493
Electrothermal SOA 496
Rapid Transient Overload 497
12.2.2. Conventional MOS Power Transistors 498
The Rectangular Device 499
The Diagonal Device 500
Computation of R_M 501
Other Considerations 502
Nonconventional Structures 503
12.2.3. DMOS Transistors 505
The Lateral DMOS Transistor 506
RESURF Transistors 508
The DMOS NPN 510
12.3 MOS Transistor Matching 511
12.3.1. Geometric Effects 513
Gate Area 513
Gate Oxide Thickness 514
Channel Length Modulation 515
Orientation 515
12.3.2. Diffusion and Etch Effects 516
Polysilicon Etch Rate Variations 516
Diffusion Penetration of Polysilicon 517
Contacts Over Active Gate 518
Diffusions Near the Channel 518
PMOS versus NMOS Transistors 519
12.3.3. Hydrogenation 520
Fill Metal and MOS Matching 521
12.3.4. Thermal and Stress Effects 521
Oxide Thickness Gradients 522
Stress Gradients 522
Thermal Gradients 522
12.3.5. Common-Centroid Layout of MOS Transistors 523
12.4 Rules for MOS Transistor Matching 528
12.5 Summary 531
12.6 Exercises 531

13 *Special Topics 534*
13.1 Merged Devices 534
13.1.1. Flawed Device Mergers 535

13.1.2. Successful Device Mergers 539
13.1.3. Low-Risk Merged Devices 541
13.1.4. Medium-Risk Merged Devices 542
13.1.5. Devising New Merged Devices 544
13.1.6. The Role of Merged Devices in Analog BiCMOS 544
13.2 Guard Rings 545
13.2.1. Standard Bipolar Electron Guard Rings 546
13.2.2. Standard Bipolar Hole Guard Rings 547
13.2.3. Guard Rings in CMOS and BiCMOS Designs 548
13.3 Single-level Interconnection 551
13.3.1. Mock Layouts and Stick Diagrams 551
13.3.2. Techniques for Crossing Leads 553
13.3.3. Types of Tunnels 555
13.4 Constructing the Padring 557
13.4.1. Scribe Streets and Alignment Markers 557
13.4.2. Bondpads, Trimpads, and Testpads 558
13.5 ESD Structures 562
13.5.1. Zener Clamp 563
13.5.2. Two-Stage Zener Clamps 565
13.5.3. Buffered Zener Clamp 566
13.5.4. V_{CES} Clamp 568
13.5.5. V_{ECS} Clamp 569
13.5.6. Antiparallel Diode Clamps 570
13.5.7. Grounded-Gate NMOS Clamps 570
13.5.8. CDM Clamps 572
13.5.9. Lateral SCR Clamps 573
13.5.10. Selecting ESD Structures 575
13.6 Exercises 578

14 *Assembling the Die 581*
14.1 Die Planning 581
14.1.1. Cell Area Estimation 582
Resistors 582
Capacitors 582
Vertical Bipolar Transistors 583
Lateral PNP Transistors 583
MOS Transistors 583
MOS Power Transistors 584
Computing Cell Area 584
14.1.2. Die Area Estimation 584
14.1.3. Gross Profit Margin 587
14.2 Floorplanning 588
14.3 Top-Level Interconnection 594
14.3.1. Principles of Channel Routing 594
14.3.2. Special Routing Techniques 596
Kelvin Connections 597
Noisy Signals and Sensitive Signals 598
14.3.3. Electromigration 600
14.3.4. Minimizing Stress Effects 603
14.4 Conclusion 604
14.5 Exercises 605

Appendices
A. Table of Acronyms Used in the Text 607
B. The Miller Indices of a Cubic Crystal 611
C. Sample Layout Rules 614
D. Mathematical Derivations 622
E. Sources for Layout Editor Software 627

Index 628

1 Device Physics

Before 1960, most electronic circuits depended upon vacuum tubes to perform the critical tasks of amplification and rectification. An ordinary mass-produced AM radio required five tubes, while a color television needed no fewer than twenty. Vacuum tubes were large, fragile, and expensive. They dissipated a lot of heat and were not very reliable. So long as electronics depended upon them, it was nearly impossible to construct systems requiring thousands or millions of active devices.

The appearance of the bipolar junction transistor in 1947 marked the beginning of the solid-state revolution. These new devices were small, cheap, rugged, and reliable. Solid-state circuitry made possible the development of pocket transistor radios and hearing aids, quartz watches and touch-tone phones, compact disc players and personal computers.

A *solid-state device* consists of a crystal with regions of impurities incorporated into its surface. These impurities modify the electrical properties of the crystal, allowing it to amplify or modulate electrical signals. A working knowledge of device physics is necessary to understand how this occurs. This chapter covers not only elementary device physics but also the operation of three of the most important solid-state devices: the junction diode, the bipolar transistor, and the field-effect transistor. Chapter 2 explains the manufacturing processes used to construct these and other solid-state devices.

1.1 SEMICONDUCTORS

The inside front cover of the book depicts a long-form periodic table. The elements are arranged so those with similar properties group together to form rows and columns. The elements on the left-hand side of the periodic table are called *metals*, while those on the right-hand side are called *nonmetals*. Metals are usually good conductors of heat and electricity. They are also malleable and display a characteristic metallic luster. Nonmetals are poor conductors of heat and electricity, and those that are solid are brittle and lack the shiny luster of metals. A few elements in the middle of the periodic table, such as silicon and germanium, have electrical

properties that lie midway between those of metals and nonmetals. These elements are called *semiconductors*. The differences between metals, semiconductors, and nonmetals result from differences in the electronic structure of their respective atoms.

Every atom consists of a positively charged nucleus surrounded by a cloud of electrons. The number of electrons in this cloud equals the number of protons in the nucleus, which also equals the atomic number of the element. Therefore, a carbon atom has six electrons, because carbon has an atomic number of six. These electrons occupy a series of *shells* that are somewhat analogous to the layers of an onion. As electrons are added, the shells fill in order from innermost outward. The outermost or *valence* shell may remain unfilled. The electrons occupying this outermost shell are called *valence electrons*. The number of valence electrons possessed by an element determines most of its chemical and electronic properties.

Each row of the periodic table corresponds to the filling of one shell. The leftmost element in the row has one valence electron, while the rightmost element has a full valence shell. Atoms with filled valence shells possess a particularly favored configuration. Those with unfilled valence shells will trade or share electrons so that each can claim a full shell. Electrostatic attraction forms a chemical bond between atoms that trade or share electrons. Depending upon the strategy adopted to fill the valence shell, one of three types of bonding will occur.

Metallic bonding occurs between atoms of metallic elements, such as sodium. Consider a group of sodium atoms in close proximity. Each atom has one valence electron orbiting around a filled inner shell. Imagine that the sodium atoms all discard their valence electrons. The discarded electrons are still attracted to the positively charged sodium atoms, but, since each atom now has a full valence shell, none accepts them. Figure 1.1A shows a simplified representation of a sodium crystal. Electrostatic forces hold the sodium atoms in a regular lattice. The discarded valence electrons wander freely through the resulting crystal. Sodium metal is an excellent electrical conductor due to the presence of numerous free electrons. These same electrons are also responsible for the metallic luster of the element and its high thermal conductivity. Other metals form similar crystal structures, all of which are held together by metallic bonding between a sea of free valence electrons and a rigid lattice of charged atomic cores.[1]

Ionic bonding occurs between atoms of metals and nonmetals. Consider a sodium atom in close proximity to a chlorine atom. The sodium atom has one valence electron, while the chlorine atom is one electron short of a full valence shell. The sodium atom can donate an electron to the chlorine atom, and by this means both can achieve filled outer shells. After the exchange, the sodium atom has a net positive

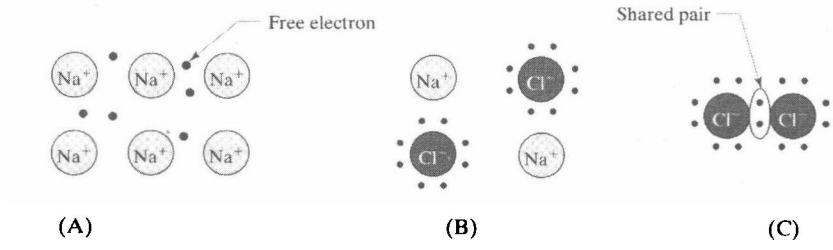


FIGURE 1.1 Simplified illustrations of various types of chemical bonding: a small part of a metallically bonded sodium crystal (A), a small part of an ionically bonded sodium chloride crystal (B), and a covalently bonded chlorine molecule (C).

[1] Some metals conduct by means of holes rather than electrons, but the general observations made here still apply.

charge and the chlorine atom, a net negative charge. The two charged atoms (or *ions*) attract one another. Solid sodium chloride thus consists of sodium and chlorine ions arranged in a regular lattice, forming a crystal (Figure 1.1B). Crystalline sodium chloride is a poor conductor of electricity, since all of its electrons are held in the shells of the various atoms.

Covalent bonding occurs between atoms of nonmetals. Consider two chlorine atoms in close proximity. Each atom has only seven valence electrons, while each needs eight to fill its valence shell. Suppose that each of the two atoms contributes one valence electron to a common pair shared by both. Now each chlorine atom can claim eight valence electrons: six of its own, plus the two shared electrons. The two chlorine atoms link to form a molecule that is held together by the electron pair shared between them (Figure 1.1C). The shared pair of electrons forms a *covalent bond*. The lack of free valence electrons explains why nonmetallic elements do not conduct electricity and why they lack metallic luster. Many nonmetals are gases at room temperature because the electrically neutral molecules exhibit no strong attraction to one another and thus do not condense to form a liquid or a solid.

The atoms of a semiconductor also form covalent bonds. Consider atoms of silicon, a representative semiconductor. Each atom has four valence electrons and needs four more to complete its valence shell. Two silicon atoms could theoretically attempt to pool their valence electrons to achieve filled shells. In practice this does not occur because eight electrons packed tightly together strongly repel one another. Instead, each silicon atom shares one electron pair with each of four surrounding atoms. In this way, the valence electrons are spread around to four separate locations and their mutual repulsion is minimized.

Figure 1.2 shows a simplified two-dimensional representation of a silicon crystal. Each of the small circles represents a silicon atom. Each of the lines between the circles represents a covalent bond consisting of a shared pair of valence electrons. Each silicon atom can claim eight electrons (four shared electron pairs), so all of the atoms have full valence shells. These atoms are linked together in a molecular network by the covalent bonds formed between them. This infinite lattice represents the structure of the silicon crystal. The entire crystal is literally a single molecule, so crystalline silicon is strong and hard, and it melts at a very high temperature. Silicon is a poor conductor of electricity because all of its valence electrons are used to form the crystal lattice.

A similar macromolecular crystal can theoretically be formed by any group-IV element,[2] including carbon, silicon, germanium, tin, and lead. Carbon, in the form of

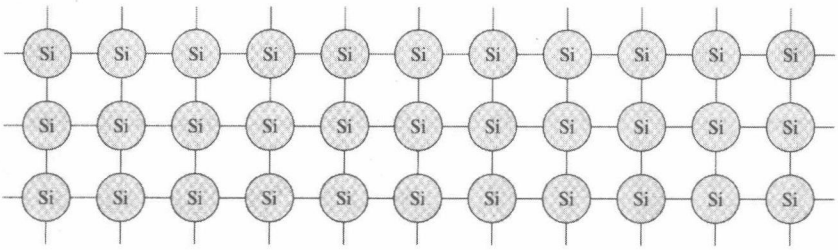


FIGURE 1.2 Simplified two-dimensional representation of a silicon crystal lattice.

[2] The group-III, IV, V, and VI elements reside in columns III-B, IV-B, V-B, and VI-B of the long-form periodic table. The group-II elements may fall into either columns II-A or II-B. The A/B numbering system is a historical curiosity and the International Union of Pure and Applied Chemists (IUPAC) has recommended its abandonment; see J. Hudson, *The History of Chemistry* (New York: Chapman and Hall, 1992), pp. 122–137.

diamond, has the strongest bonds of any group-IV element. Diamond crystals are justly famed for their strength and hardness. Silicon and germanium have somewhat weaker bonds due to the presence of filled inner shells that partially shield the valence electrons from the nucleus. Tin and lead have weak bonds because of numerous inner shells; they typically form metallically bonded crystals instead of covalently bonded macromolecules. Of the group-IV elements, only silicon and germanium have bonds of an intermediate degree of strength. These two elements act as true semiconductors, while carbon is a nonmetal, and tin and lead are both metals.

1.1.1. Generation and Recombination

The electrical conductivity of group-IV elements increases with atomic number. Carbon, in the form of diamond, is a true insulator. Silicon and germanium have much higher conductivities, but these are still far less than those of metals such as tin and lead. Because of their intermediate conductivities, silicon and germanium are termed *semiconductors*.

Conduction implies the presence of free electrons. At least a few of the valence electrons of a semiconductor must somehow escape the lattice to support conduction. Experiments do indeed detect small but measurable concentrations of free electrons in pure silicon and germanium. The presence of these free electrons implies that some mechanism provides the energy needed to break the covalent bonds. The statistical theory of thermodynamics suggests that the source of this energy lies in the random thermal vibrations that agitate the crystal lattice. Even though the average thermal energy of an electron is relatively small (roughly 0.04 electron-volt at 25°C), these energies are randomly distributed, and a few electrons possess much larger energies. The energy required to free a valence electron from the crystal lattice is called the *bandgap energy*. A material with a large bandgap energy possesses strong covalent bonds and therefore contains few free electrons. Materials with lower bandgap energies contain more free electrons and possess correspondingly greater conductivities (Table 1.1).

TABLE 1.1 Selected properties

Element	Atomic Number	Melting Point, °C	Electrical Conductivity, $(\Omega \cdot cm)^{-1}$	Bandgap Energy, eV
Carbon (diamond)	6	3550	$\sim 10^{-16}$	5.2
Silicon	14	1410	$4 \cdot 10^{-6}$	1.1
Germanium	32	937	0.02	0.7
White tin	50	232	$9 \cdot 10^{4}$	0.1

A vacancy occurs whenever an electron leaves the lattice. One of the atoms that formerly possessed a full outer shell now lacks a valence electron and therefore has a net positive charge. This situation is depicted in a simplified fashion in Figure 1.3. The ionized atom can regain a full valence shell if it appropriates an electron from a neighboring atom. This is easily accomplished since it still shares electrons with three adjacent atoms. The electron vacancy is not eliminated; it merely shifts to the

[3] Bandgap energies for Si, Ge: B. G. Streetman, *Solid State Electronic Devices*, 2d ed. (Englewood Cliffs, NJ: Prentice-Hall, 1980), p. 443. Bandgap for C: N. B. Hanny, ed., *Semiconductors* (New York: Reinhold Publishing, 1959), p. 52. Conductivity for Sn: R. C. Weast, ed., *CRC Handbook of Chemistry and Physics*, 62d ed. (Boca Raton, FL: CRC Press, 1981), pp. F135–F136. Other values computed. Melting points: Weast, pp. B4–B48.