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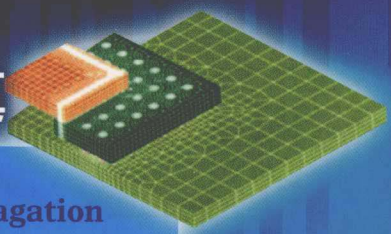
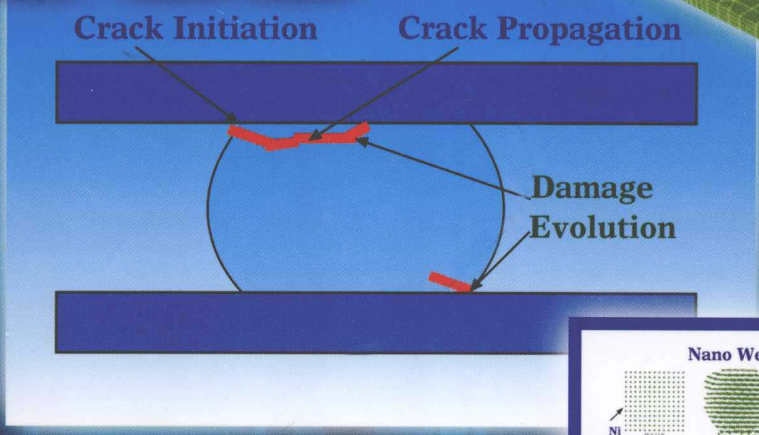
Modeling and Simulation for Microelectronic Packaging Assembly

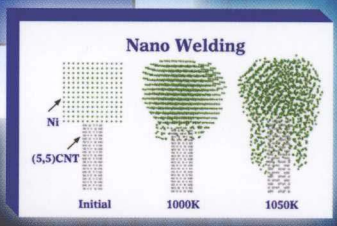
Manufacturing, Reliability and Testing

微电子封装组件的建模和仿真

——制造、可靠性与测试







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·北京·

随着电子封装的发展，电子封装已从传统的四个主要功能（电源系统、信号分布及传递、散热及机械保护）扩展为六个功能，即增加了 DFX 及系统测试两个新的功能。其中 DFX 是为“X”而设计，X 包括：可制造性、可靠性、可维护性、成本，甚至六西格玛。DFX 有望在产品设计阶段实现工艺窗口的确定、可靠性评估和测试结构及参数的设计等功能，真正做到“第一次就能成功”，从而将计算机辅助工程（CAE）变为计算机主导工程（CE），以大大加速产品的上市速度。本书是全面介绍 DFX 在封装中应用的图书。作为封装工艺过程和快速可靠性评估及测试建模仿真的第一本专著，书中包含两位作者在工业界二十多年的丰富经验，以及在 MEMS、IC 和 LED 封装部分成功的实例，希望能给国内同行起到抛砖引玉的作用。同时，读者将会从书中的先进工程设计和微电子产品的并行工程和协同设计方法中受益。

本书主要读者对象为学习 DFX（制造工艺设计、测试设计、可靠性设计等）的研究人员、工程师和学生等。

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Foreword

By C. P. Wong

Modeling and simulation of microelectronic packaging and assembly is a multi-disciplinary activity that relies on the expertise of sequence dependant complex processes, almost all the material types, and detailed process windows; a very challenging task for both academic people and practicing engineers. Modeling and simulation has been classified in the ITRS Roadmap in the past years as being one of the cross cutting technologies that must be mastered to enable rapid progress in this first industry. The importance of modeling and simulation has been witnessed by the increasing number of design engineers in each corporation from 20% in the early 1980s to 80% in the late 2000s in terms of recruited engineers, as it is essential to design and make the product the first time right.

The most popular methodology of design and manufacturing is called Design for X (DFX, here X refers to manufacturing, assembly, testing, reliability, maintenance, environment, and even cost), which has been widely adopted by those multinational and small high tech start-up companies. The design methodology is being adjusted to meet the requirements of a full-life cycle, the so called "concept/ cradle-to-grave" product responsibility, coined by Dr. Walter L. Winterbottom of Ford Science Lab.

A packaging module and related application systems, like any other electronic systems, involve a lot of manufacturing processes from film deposition, etching, chip to wafer and wafer to wafer bonding, dicing/ sigulation, and extensive reliability testing for extended-life goals of many critical products such as those used for automobile electronics, avionics, portable electronics, and so on. The defects in terms of voids, cracks, delaminations, and microstructure changes, can be induced in any step and may interact and grow in subsequent steps, imposing extreme demands on the fundamental understanding of stressing and physics of failures. Currently, the testing programs have been extensive to assure reliability during product development. An iterative, build-test-fix-later process has long been used in new product development, significant concerns are being addressed as cost effective and fast time-to-market needs may not be achievable with such an approach. In the sense of high reliability, system hardware design and manufacturing and testing are costly and time consuming, and severely limit the number of design choices within the short time frame, and do not allow enough time to explore the optimal design. With the current situation of three to six months for each generation of IC chip, it is challenging to achieve truly optimal and innovative products with so many constraints in design. Design procedure must be modified and DFX must be used so as to achieve prevention with integrated consideration of manufacturing processes, testing, and operation.

Although there is still a long way to go to enable virtual manufacturing, virtual reliability and virtual testing due to the many difficulties involved, pioneering efforts have been made since the early 1990s by outstanding professionals to shorten the gap significantly, and Professor Sheng Liu and Dr. Yong Liu are two of those brave individuals. Professor Sheng Liu and Dr. Yong Liu have been promoting the new design method in the past years to help assist engineers in material selection, manufacturing yield enhancement, appropriate rapid reliability assessment, and testing when the packaging module and system are subjected to uncertainties of material selection, process windows, and various service loadings. All these issues must be addressed prior to hardware build-up and test.

A lot of processes were first time modeled and simulated by the two authors, addressing the critical importance of modeling in manufacturing, reliability, and testing. Many books about packaging have been written. Some books have been written in which mechanics has been applied to reliability issues only. This is the first book focusing on the many detailed processes in front end, back end, even probing, wire bonding, bonding, and so on. It is the first book to cover the broad aspects from manufacturing to reliability, and to testing, with many examples of their pioneering efforts. The authors describe their contributions in detail and provide guidance to those in the field and present a design approach that must ultimately replace the build-test-fix-later process if the efficiencies and potential cost benefits of the microelectronic packaging systems are to be fully realized.

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Foreword

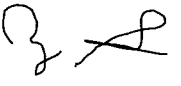
By Zhigang Suo

The dramatic rise of the semiconductor industry is fundamentally changing our lives. Memory devices store all human experience, or at least the part that can be digitized. Solid-state lighting saves energy. Biochips detect cancers early and at low cost. Our brains are being scanned to unravel the molecular basis of happiness and despair. The world has become a giant computer, connecting people to people, and to a multitude of devices that extend our senses. The distinction between the computer and the human may one day become a matter of choice.

The exciting future aside, the semiconductor industry is facing major challenges. As the features on chips shrink, approaching the nanoscale, the cost for chip-making equipment has been increasing. Diverse functions are being packaged, as represented by cell phones, power electronics, MEMS, solar cells, and deformable electronics. Complex manufacturing processes inevitably generate defects, which may lower the yield or result in low returns. For an industry particularly sensitive to cost and time-to-market, it has become increasingly difficult to create technologies and design products by using the trial-and-error approach.

Simulation based on mechanics has long been important for the aerospace and automobile industries, and is becoming more and more important in the semiconductor industry. The strong industrial needs have attracted many researchers to develop methods to simulate manufacturing processes and testing methods. While the dream of virtual manufacturing and virtual testing may not fully come true in the near future, simulation has already begun to reduce the amount of trial-and-error manufacturing and uncontrolled testing. The sustained effort will make the technology greener.

The authors of this book, Professor Sheng Liu and Dr. Yong Liu, are outstanding researchers and engineers. Since early 1990s, they have been intimately involved in pioneering efforts in simulating almost all the major manufacturing processes, ranging from plastic packaging to nano welding. They have devoted their careers to building material databases, developing constitutive models, finding ways to validate the models, constantly refining them, and using the models to solve practical problems. They have applied mechanics to various industry sectors, including commercial electronics, automobile electronics, powering electronics, CPUs, micro sensors, and solid-state lighting. Their experience is distilled in this book. The book is an important addition to mechanics and microelectronics, as well as to other industries that involve sophisticated manufacturing processes and testing methods.



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Preface

Over the past two decades semiconductor technology has made impressive progress, particularly in electronics, opto electronics, communications, health, automotive applications, computing, consumer electronics, security, and industrial electronics. These progresses are powered by Moore's law which is focusing on IC miniaturization down to nano dimensions and system on chip (SoC) integration. However, there are technologies based on or derived from silicon technologies but which do not simply scale with Moore's law such as the RF, power electronics, sensors, MEMS, opto/lighting and other systems in package; these technologies are called "More than Moore". Along with the technology development trends characterized by Moore's law and "More than Moore", the business trends are mainly characterized by cost reduction, shortertime-to-market, and outsourcing. The combination of these technology and business trends leads to increased design complexity, decreased design margins, increased chances and consequences of failure in reliability, decreased product development in R&D, and difficulties in assembly manufacture and qualification times. Especially in the assembly manufacturing process, quality and reliability are key technologies to ensure a successful product. In addition to the forward looking trends of technology it is important to recognize that the methods for concurrent engineering of these solutions (both the semiconductor content and high performance package capability) are becoming increasingly dependent on rigorous use of proven multi-physics/finite element analysis (FEA) tools and techniques for both new product development and its assembly processes. The correct use of the modeling tool can definitely save design time and shorten the design cycle. The challenges are along with the development of new package technology; can the modeling tools and methodologies be ready to support the new trends? Examples are various designs, reliability and assembly manufacture modeling which include electro migration simulation; diffusion along the interface of two metal materials; contamination at the interface between leadframe, multiple chips and EMC; thermal resistance definition in system in package (SiP); 3D copper stud bumping, wire bonding simulation, and so on.

Most challenges in modeling for electronic packaging today are the fundamental multiple-physics simulation which couples the electrical, thermal, and mechanical fields for various assembly manufacturing processes and for various reliability tests. Development of a highly efficient modeling algorithm for such a SiP system is critical for the virtual prototyping of the new product. In some cases, the SiP might have strong thermal mechanical performance but is weak in the electrical area, or the SiP has very good electrical performance but is weak in thermal-mechanical design. Therefore, it is necessary to establish the best solution using the modeling design of experiment (DoE) while the actual tests or actual assembly manufacturing will cost more and take much longer.

In industry, we all understand the importance of assembly manufacturing, reliability, and testing, because a lot of packaging failures are related to the assembly process. Examples include the wire bonding process, which would induce silicon cratering, bond pad peel off, and interlayer dielectric (ILD) layer under bond pad cracking; die attaching process for multiple die; the order of the die attaching process will have a big impact on the residual stress after the die bonding. When thin die (today the thinnest die thickness would be below 20 microns) is picked up from the tape, the pick-up process could crack the silicon. The molding process is also a key process which could induce later failure, such as delamination due to the voids tracked in the interface between the leadframe and encapsulate molding compound (EMC). Leadframe forming, punch/simulation, and trim may result in the die and package cracking as well. A lot of initial tiny defects are induced in first assembly manufacture process; later in the further

assembly process and reliability test, they become potential product quality and reliability concerns. An example is wafer sorting, which will induce the cratering/marks on the bond pad. When the wire bonding process is applied to the cratered/marked bond pad, it will definitely impact the adhesion strength at the interface between the wire bond and the bond pad. Product line engineers are always interested in knowing wire bonding versus wafer probing; which makes things worse? The study of assembly manufacture processes through modeling and simulation started from the beginning of the IC packaging, and today the need for modeling and simulation in this area has increased much more. However, at the present time, there is no book that has systematically described the modeling methodologies for assembly manufacturing, reliability, and testing, as well as discussing the above challenges and giving the readers some unresolved space for further exploring. This is our goal in writing this book; to share our modeling experiences and systematically introduce our modeling methodologies for electronic packaging assembly manufacturing, reliability and testing.

This book is primarily concerned with studies of electronic packaging in assembly manufacture processes and failure mechanisms in assembly manufacture processes and tests through modeling and simulation. However, the fundamental studies regarding the advanced modeling methodologies including molecular dynamics, state of the art simulation algorithms, material constitutive relations, material behavior testing, and various semiconductor reliability tests are also discussed and presented in the book. Various package layouts including the 3D/TSV/Stacking/SiP, carbon nano-tube and interconnects technology, opto packaging, and MEMS are discussed and presented in the book as well. A lot of case studies provide the most advanced research progress and the topics that industry is interested in. The basic framework of this book is arranged in four parts, the first part (Part I) includes eight chapters that introduce the fundamental mechanics concepts, material constitutive models, basic modeling methodologies such as finite element, and the concurrent engineering background for microelectronics. This part is to provide readers with the background knowledge for modeling and simulation, mechanics, material, and the engineering. The next part (Part II) is concerned with the modeling in microelectronic packaging and the assembly manufacturing process which includes five chapters. Major topics include the electronic packaging front of line (which involves key processes such as wafer sorting, die picking up, die attach process, wire bonding); end of line (which includes molding, leadframe clamping, forming, and singulation); Opto packaging assembly; MEMS packaging assembly; system in packaging stack/3D assembly and the Nano interconnects and packaging assembly. Part III describes the modeling in reliability and testing which includes the wafer probing test and typical package reliability tests such as the temperature cycle test, power cycle test, drop test, electro-migration test, precondition test with reflow which includes moisture sensitivity test, vapor pressure at reflow with the popcorning failure mechanisms. The advanced simulation algorithm will be presented especially in the wafer level CSP solder joint reliability in drop test, temperature cycling, and the mass migration induced failure which includes electro migration, thermal migration, stress migration, and the atomic density gradient induced migration. The final part will introduce the modern modeling and simulation methodologies which include the classical molecular dynamics, advanced molecular dynamics, and coupling with continuum modeling methods. This part will disclose how the modern modeling and simulation methodologies will impact the assembly manufacturing, reliability and the testing for today and future advanced package development. An appendix is available on the book companion web site for those who like to know more detail about finite element.

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The materials in this book have clearly been derived mainly from previous papers and research notes by the two authors and some works of their friends which are mainly from both the research community and industry, such as Dr. Gary Li of Freescale, Dr. Yifan Guo of Skyworks, and Professor Zhigang Suo from Harvard University. It would be quite impossible for us to express our appreciation to everyone concerned for their collaboration in the production of this book, but we would like to extend our gratitude. In particular, we would like to thank several professional societies in which we have previously published some of our materials included in this book. They are the American Society of American Engineers (ASME) and the Institute of Electrical and Electronic Engineers (IEEE) for their conferences, proceedings, and journals, including *ASME Transactions on Journal of Electronic Packaging, IEEE Transactions on Advanced Packaging, IEEE Transactions on Components and Packaging Technology* and *IEEE Transactions on Electronics Packaging Manufacturing*. Many important conferences such as the Electronic Components and Technology Conference (ECTC), and International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT–HDP), EuroSime are also appreciated for the reproduction of some of their publication materials.

We would like to acknowledge those colleagues who helped review some chapters and manuscript. They are Dr. YiHsin Pao of Foxcom, Professor Biao Wang of SunYiSan University, Professor Kikuo Kishimoto at Tokyo Institute of Technology, and Professor Ricky Lee at Hong Kong University of Science and Technology. We would like to thank them for many suggestions and comments which added a lot to this book. Their depth of knowledge and their dedication have been demonstrated throughout the process of reviewing this book and its chapters.

We would like to thank Huazhong University of Science and Technology (HUST), Wuhan National Laboratory for Optoelectronics, the School of Mechanical Science and Engineering, and Fairchild Semiconductor Corporation for providing us with excellent working environment to make this book possible. We also appreciate those places where we have previously studied and worked, such as Stanford University, Florida Institute of Technology, and Wayne State University, where we conducted quite a significant part of our research results in the book. We would like to express our appreciation to those who have worked in microelectronic packaging and assembly for many years, such as those SRC mentors in the first author's research. The first author felt honored to have worked with Dr. William Chen and Dr. T. Y. Wu at ASE (formerly at IBM), Dr. YiFan Guo at Skyworks (formerly at IBM and Freescale), Dr. J. Benson at Harris, Dr. T.D. Dudderar at Bell Labs, Dr. L. Li at Cisco (formerly at IBM), Dr. M.J. Lii at Intel, Dr. Z. Mei at HP, Dr. S. Sidharth at AMD, Dr. L. Stark at TI, and Dr. J. Xie at Cisco (formerly at Motorola), Dr. S. Wu at Motorola, and Dr. Luu T. Nguyen at National. We would also like to thank several outstanding scholars and leaders who once worked or who are still working at HUST, who have been providing us with

About the Authors

Sheng Liu is a Changjiang scholar Professor of Mechanical Engineering at Huazhong University of Science and Technology and he has a dual appointment at Wuhan National Laboratory for Optoelectronics. He was once a tenured faculty at Wayne State University. He has over 18 years experience in LED/MEMS/IC packaging. He has extensive experience in consulting with many leading multinational and Chinese companies. He won the prestigious White House/NSF Presidential Faculty Fellow Award in 1995, the ASME Young Engineer Award in 1996, the NSFC Overseas Young Scientist Award in 1999 in China, the IEEE CPMT Exceptional Technical Achievement Award in 2009, and the Chinese Electronic Manufacturing and Packaging Technology Society Special Achievement Award in 2009. He has been an associate editor of *IEEE Transactions on Electronic Packaging Manufacturing* since 1999 and an associate editor of *Frontiers of Optoelectronics in China* since 2007. Since 2006, he has been one of the 11 National Committee Members in LED at the Ministry of Science and Technology of China. He obtained his PhD from Stanford University in 1992, his MS and BS degrees from Nanjing University of Aeronautics and Astronautics in 1986 and 1983 respectively. He was an aircraft designer at the Chengdu Aircraft Company for two years. He is also currently an ASME Fellow. He has filed and owned more than 140 patents in China and in the USA, has published more than 500 technical articles, given more than 100 keynotes and invited talks, and edited more than nine proceedings in English for the ASME and IEEE.

Yong Liu has been with Fairchild Semiconductor Corporation in South Portland, Maine since 2001; as a Senior Member of the Technical Staff from 2008, a Member of the Technical Staff from 2004–2007, and a Principal Engineer from 2001–2004. He is now a Fairchild global team leader of electrical, thermal-mechanical modeling and analysis. His main area of interest is advanced IC packaging, modeling and simulation, reliability and assembly process. In the last few years he and his team have been working on advanced IC package modeling and simulation, which includes pioneering work on the assembly manufacture process, the electromigration induced failures for chip scale wafer level packages, and co-design automation. He has been invited to give keynotes talks and presentations at international conferences such as Eurosime, ICEPT–HDP, and EPTC and at universities in the USA, Europe, and China. He has co-authored over 140 papers in journals and conferences and has filed over 40 USA patents in the area of 3D/Stack/TSV IC packaging and power devices. Dr. Liu obtained his BS, Masters, and PhD degrees at the Nanjing Univeristy of Science and Technology in 1983, 1987, and 1990 respectively. He was once promoted, in a ground-breaking way, as a full professor at Zhejiang University of Technology in 1994. Dr. Liu was awarded an Alexander von Humboldt Fellowship and studied as a Humboldt fellow at Tech University of Braunschweig, Germany in 1995. In 1997, he was awarded an Alexander von Humboldt European Fellowship and studied as a Humboldt European fellow at the University of Cambridge, England. In 1998, he worked as a post-doctor at Semiconductor Focus Center and Computational Mechanics Center,

Rensselaer Polytechnic Institute (RPI). In 2000, he worked as a staff opto package engineer at Nortel Networks in Boston. Since he joined Fairchild in 2001, he was awarded the first Fairchild President Award in 2008, the Fairchild Key Technologist in 2006 and 2009, the Fairchild BIQ award in product innovation in 2005, and the Fairchild award for Power of the Pen first place in 2004. Yong Liu is currently an IEEE Senior member and has been actively involved in technical committees of the IEEE ECTC, EuroSime, ESREF, ESTC, EPTC, and ICEPT.

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