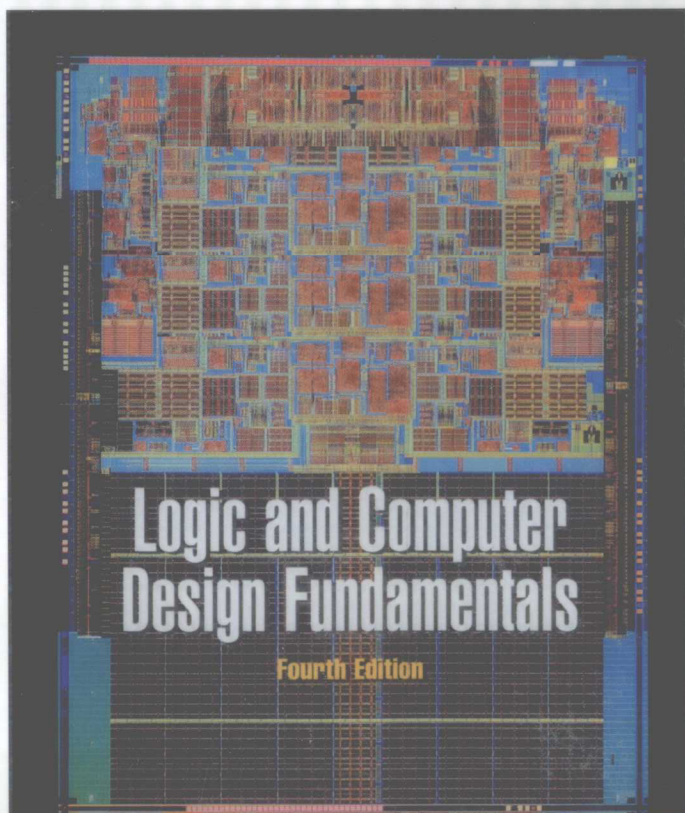


逻辑与计算机设计基础

(英文版·第4版)



M. Morris Mano

加州大学洛杉矶分校

(美)

Charles R. Kime

威斯康星大学麦迪逊分校

著



机械工业出版社
China Machine Press

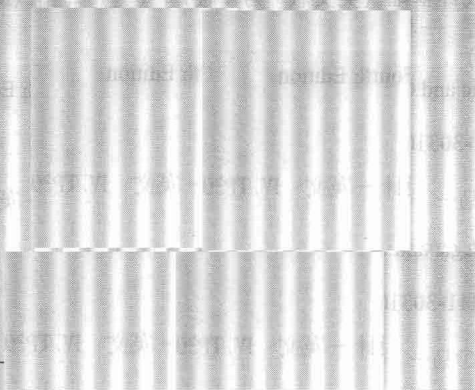
经典原版书库

逻辑与计算机设计基础

(英文版·第4版)

Logic and Computer Design Fundamentals

(Fourth Edition)



机械工业出版社
China Machine Press

English reprint edition copyright © 2010 by Pearson Education Asia Limited and China Machine Press.

Original English language title: *Logic and Computer Design Fundamentals, Fourth Edition* (ISBN 978-0-13-198926-9) by M. Morris Mano and Charles R. Kime, Copyright © 2008.

All rights reserved.

Published by arrangement with the original publisher, Pearson Education, Inc., publishing as Prentice Hall.

For sale and distribution in the People's Republic of China exclusively (except Taiwan, Hong Kong SAR and Macau SAR).

本书英文影印版由 Pearson Education Asia Ltd. 授权机械工业出版社独家出版。未经出版者书面许可, 不得以任何方式复制或抄袭本书内容。

仅限于中华人民共和国境内(不包括中国香港、澳门特别行政区和中国台湾地区)销售发行。

本书封面贴有 Pearson Education (培生教育出版集团) 激光防伪标签, 无标签者不得销售。

封底无防伪标均为盗版

版权所有, 侵权必究

本书法律顾问 北京市展达律师事务所

本书版权登记号: 图字: 01-2009-6762

图书在版编目(CIP)数据

逻辑与计算机设计基础(英文版·第4版)/(美)马诺(Mano, M.M.), 凯姆(Kime, C.R.)著. —北京: 机械工业出版社, 2010.4

(经典原版书库)

书名原文: *Logic and Computer Design Fundamentals, Fourth Edition*

ISBN 978-7-111-30310-7

I. 逻… II. ①马… ②凯… III. 电子计算机—逻辑设计—英文 IV. TP302.2

中国版本图书馆 CIP 数据核字(2010)第 057164 号

机械工业出版社(北京市西城区百万庄大街 22 号 邮政编码 100037)

责任编辑: 李俊竹

北京京师印务有限公司印刷

2010 年 4 月第 1 版第 1 次印刷

150mm × 214mm · 21.875 印张

标准书号: ISBN 978-7-111-30310-7

定价: 58.00 元

凡购本书, 如有缺页、倒页、脱页, 由本社发行部调换

客服热线: (010) 88379210; 88361066

购书热线: (010) 68326294; 88379649; 68995259

投稿热线: (010) 88379604

读者信箱: hzjsj@hzbook.com

PREFACE

The objective of this text is to serve as a cornerstone for the learning of logic design, digital system design, and computer design by a broad audience of readers. This fourth edition marks the decade point in the evolution of the text contents. Beginning as an adaptation of a previous book by the first author in 1997, it continues to offer a unique combination of logic design and computer design principles with a strong hardware emphasis. Over the years, the text has followed industry trends by adding new material such as hardware description languages, removing or de-emphasizing material of declining importance, and revising material to track changes in computer technology and computer-aided design.

In the fourth edition, revisions address pedagogical considerations as well as industrial trends. Sixty “real world” examples and problems, most drawn from design problems for products encountered in contemporary day-to-day life, motivate interest and provide practice in solution formulation. Changes in chapter organization permit instructors to more easily tailor the degree of technology coverage, accommodating both electrical and computer engineering and computer science audiences.

The organizational changes begin with the combining of the introduction to design from Chapter 3 and the functional block material from Chapter 4 into a new Chapter 3. The design science content from the old Chapter 3 is now distributed over multiple chapters on an “as needed” basis and is accompanied by illustrations. Hardware description language coverage for combinational circuits has been combined in Chapter 4 with that for arithmetic circuits to balance chapter size. Material on technology from the old Chapter 3, including timing and programmable logic, appears in a new Chapter 6 and can be selectively covered and scheduled by the instructor as appropriate for the course syllabus. The placement of this material in Chapter 6 permits earlier coverage of sequential circuits for those with lesser technology-related needs and provides the more extensive background needed for some of the topics covered. Further, technology topics fit better within digital system design rather than within basic logic design material presented earlier in the text. Chapter 6 also contains new information on CMOS circuits and asynchronous interaction between systems including synchronization of inputs and metastability.

Chapter 8 has been eliminated along with the algorithmic state machine (ASM) to streamline the treatment of design of complex sequential circuits and control units. Concepts from Chapter 8 are split between Chapter 5 (Sequential Circuits) and Chapter 7 (Registers and Register Transfers). A new state machine

diagram notation replaces the ASM. The state machine diagram is modeled after the traditional state diagram and graphically represents much of the modeling flexibility inherent in hardware description languages. Further, in Chapter 7, the design procedure for doing combined datapath and control unit design is formalized and illustrated.

Offering integrated coverage of both digital and computer design, this edition of *Logic and Computer Design Fundamentals* features a strong emphasis on fundamentals underlying contemporary design. Understanding of the material is supported by clear explanations and a progressive development of examples ranging from simple combinational applications to a CISC architecture built upon a RISC core. A thorough coverage of traditional topics is combined with attention to computer-aided design, problem formulation, solution verification, and the building of problem-solving skills. Flexibility is provided for selective coverage of logic design, digital system design, and computer design topics, and for coverage of hardware description languages (none, VHDL, or Verilog®). Aside from the organizational and content changes describe thus far, other updates in the Fourth Edition include: (1) a brief introduction to embedded systems, (2) illustration of practical computer-aided logic optimization methods as used in Espresso, (3) replacement of a CRT display example with an LCD screen example, and (4) an updated Architectural Innovations section including multiple CPU microprocessors.

With these revisions, chapters 1 through 5 of the book treat logic design, chapters 6 through 8 deal with digital systems design and chapters 9 through 13 focus on computer design. This arrangement provides solid digital system design fundamentals while accomplishing a gradual, bottom-up development of fundamentals for use in top-down computer design in later chapters. Summaries of the topics covered in each chapter follow.

Chapter 1—Digital Systems and Information This chapter introduces digital computers, embedded systems, and information representation including number systems, arithmetic, and codes.

Chapter 2—Combinational Logic Circuits This chapter deals with gate circuits and their types and basic ideas for their design and cost optimization. Concepts include Boolean algebra, algebraic and Karnaugh map optimization, the Espresso algorithm as a pragmatic CAD optimization tool, and multilevel optimization.

Chapter 3—Combinational Logic Design This chapter begins with an overview of a contemporary logic design process. The details of steps of the design process including problem formulation, logic optimization, technology mapping to NAND and NOR gates, and verification are covered for combinational logic design examples. In addition, the chapter covers the functions and building blocks of combinational design including enabling and input-fixing, decoding, encoding, code conversion, selecting, and distributing, and their implementations.

Chapter 4—Arithmetic Functions and HDLs This chapter deals with arithmetic functions and their implementations. Beyond number representation for arithmetic, addition, subtraction, and incrementing, decrementing, filling, extension and shifting are described and implemented. Synthesis and hardware description languages (HDLs) are introduced and Verilog and VHDL are presented for

describing of combinational logic from Chapter 3 and arithmetic logic from this chapter.

Chapter 5—Sequential Circuits This chapter covers sequential circuit analysis and design. Latches, master-slave flip-flops and edge-triggered flip-flops are covered with emphasis on the D type. Other types of flip-flops (S-R, J-K and T), which are used less frequently in modern designs, are covered briefly. Emphasis is placed on state machine diagram and state table formulation. A complete design process for sequential circuits including specification, formulation, state assignment, flip-flop input and output equation determination, optimization, technology mapping, and verification is developed. A graphical state machine diagram model that represents sequential circuits too complex to model with a conventional state diagram is presented and illustrated by two real world examples. The chapter concludes with VHDL and Verilog descriptions of a flip-flop and a sequential circuit.

Chapter 6—Selected Design Topics This chapter presents topics focusing on various aspects of underlying technology including the MOS transistor and CMOS circuits, delay and timing for gates, combinational and sequential circuits, asynchronous interactions between circuits, and programmable logic technologies. The asynchronous interactions section includes coverage of synchronization of asynchronous inputs and metastability. Programmable logic covers read-only memories, programmable logic arrays and programmable array logic.

Chapter 7—Registers and Register Transfers This chapter covers registers and their applications. Shift register and counter design are based on the combination of flip-flops with functions and implementations introduced in the Chapters 3 and 4. Only the ripple counter is introduced as a totally new concept. Register transfers are considered for both parallel and serial designs and time-space trade-offs are discussed. A section focuses on register cell design for multi-function registers that performing multiple operations. A process for the integrated design of datapaths and control units using register transfer statements and state machine diagrams is introduced and illustrated by two real world examples. Verilog and VHDL descriptions of selected register types are introduced.

Chapter 8—Memory Basics This chapter introduces static random access memory (SRAM) and dynamic random access memory (DRAM), and basic memory systems. It also describes briefly various distinct types of SRAMs.

Chapter 9—Computer Design Basics This chapter covers register files, function units, datapaths, and two simple computers: a single-cycle computer and a multiple-cycle computer. The focus is on datapath and control unit design formulation concepts applied to implementing specified instructions and instruction sets in single-cycle and multiple-cycle designs.

Chapter 10—Instruction Set Architecture introduces many facets of instruction set architecture. It deals with address count, addressing modes, architectures, and the types of instructions and presents floating-point number representation and operations. Program control architecture is presented including procedure calls and interrupts.

Chapter 11—RISC and CISC Processors This chapter covers high-performance processor concepts including a pipelined RISC processor, and a CISC processor. The

CISC processor, by using microcoded hardware added to a modification of the RISC processor, permits execution of the CISC instruction set using the RISC pipeline, an approach used in contemporary CISC processors. Also, sections describe high-performance CPU concepts and architecture innovations including two examples of multiple CPU microprocessors.

Chapter 12—Input-Output and Communication This chapter deals with data transfer between the CPU and memory, input-output interfaces and peripheral devices. Discussions of a keyboard, a Liquid Crystal Display (LCD) screen, and a hard drive as peripherals are included, and a keyboard interface is illustrated. Other topics range from serial communication, including the Universal Serial Bus (USB), to interrupt system implementation.

Chapter 13—Memory Systems has a particular focus on memory hierarchies. The concept of locality of reference is introduced and illustrated by consideration of the cache/main memory and main memory/hard drive relationships. An overview of cache design parameters is provided. The treatment of memory management focuses on paging and a translation lookaside buffer supporting virtual memory.

In addition to the text itself, a Companion Website and an Instructor's Manual are provided. Companion Website (<http://www.prenhall.com/mano>) content includes the following: 1) reading supplements including new material and material deleted from prior editions, 2) VHDL and Verilog source files for all examples, 3) links to computer-aided design tools for FPGA design and HDL simulation, 4) solutions for about one-third of all text Chapter problems, 5) errata, 6) PowerPoint® slides for Chapters 1 through 9, 7) projection originals for complex figures and tables from the text, and 8) site news sections for students and instructors pointing out new material, updates, and corrections. Instructors are encouraged to periodically check the instructor's site news so that they are aware of site changes. **Instructor's Manual** content includes suggestions for use of the book and all problem solutions. On-line access to this manual is available from Prentice Hall to instructors at academic institutions who adopt the book for classroom use. The suggestions for use provide important detailed information for navigating the text to fit with various course syllabi.

Because of its broad coverage of both logic and computer design, this book serves several different objectives in sophomore through junior level courses. Chapters 1 through 10 with selected sections omitted, provide an overview of hardware for computer science, computer engineering, electrical engineering or engineering students in general in a single semester course. Chapters 1 through 5 possibly with selected parts of 6 through 8 give a basic introduction to logic design, which can be completed in a single quarter for electrical and computer engineering students. Coverage of Chapters 1 through 8 in a semester, provides a stronger, more contemporary logic design treatment. The entire book, covered in two quarters, provides the basics of logic and computer design for computer engineering and science students. Coverage of the entire book with appropriate supplementary material or a laboratory component can fill a two-semester sequence in logic design and computer architecture. Due to its moderately paced treatment of a wide range of topics, the book is ideal for self-study by engineers and computer scientists. Finally, all of these

various objectives can also benefit from use of reading supplements provided on the Companion Website.

During the preparation of the fourth edition, we have sought out the views of many instructors using prior editions of this text. Over 50 instructors completed an extensive survey on the third edition content and their uses of it. In addition, Professor Bharat Bhuvra, Vanderbilt University, and Professor Donald Hung, San Jose State University, provided useful feedback through written reviews of the third edition. We are very grateful to all of these instructors for their participation and their thoughtful input in guiding the preparation of the fourth edition. Particular thanks goes to Professors Katherine Compton, Mikko Lipasti, Kewal Saluja, and Leon Shohet, and Faculty Associate Michael Morrow, ECE, University of Wisconsin–Madison. Via focused discussions with the second author, they provided extensive comments and suggestions that greatly influenced the fourth edition content. We appreciate corrections to the third edition provided by both instructors and students, most notably, those from Professor Douglas De Boer of Dordt College. A special thanks goes to Divya Jhalani from the University of Wisconsin–Madison for her preparation of solutions to new problems in the Instructor’s Manual and on the website. Our appreciation goes to all of those at Prentice Hall and elsewhere for their efforts on this edition. Notable are Editor Mike McDonald for his guidance, encouragement and support, Production Editors Dan Sandin and Irwin Zucker for their efficiency and helpfulness with text production, and Bob Lentz for his meticulous copy-editing. Finally, a very special thanks to Val Kime for her enduring patience and understanding throughout the development of the fourth edition.

M. MORRIS MANO
CHARLES R. KIME

CONTENTS

Preface	iii
□ Chapter 1 3	
DIGITAL SYSTEMS AND INFORMATION	3
1-1 Information Representation	4
The Digital Computer	6
Beyond the Computer	7
More on the Generic Computer	11
1-2 Number Systems	13
Binary Numbers	14
Octal and Hexadecimal Numbers	16
Number Ranges	17
1-3 Arithmetic Operations	18
Conversion from Decimal to Other Bases	20
1-4 Decimal Codes	23
BCD Addition	24
1-5 Alphanumeric Codes	25
ASCII Character Code	26
Parity Bit	26
1-6 Gray Codes	28
1-7 Chapter Summary	31
References	31
Problems	31
□ Chapter 2 35	
COMBINATIONAL LOGIC CIRCUITS	35
2-1 Binary Logic and Gates	35
Binary Logic	36
Logic Gates	38

2-2	Boolean Algebra	39
	Basic Identities of Boolean Algebra	42
	Algebraic Manipulation	44
	Complement of a Function	47
2-3	Standard Forms	48
	Minterms and Maxterms	49
	Sum of Products	52
	Product of Sums	54
2-4	Two-Level Circuit Optimization	54
	Cost Criteria	55
	Map Structures	56
	Two-Variable Maps	59
	Three-Variable Maps	61
2-5	Map Manipulation	65
	Essential Prime Implicants	65
	Nonessential Prime Implicants	67
	Product-of-Sums Optimization	68
	Don't-Care Conditions	70
2-6	Pragmatic Two-Level Optimization	72
2-7	Multiple-Level Circuit Optimization	76
2-8	Other Gate Types	81
2-9	Exclusive-OR Operator and Gates	85
	Odd Function	86
2-10	High-Impedance Outputs	88
2-11	Chapter Summary	90
	References	90
	Problems	91

□ Chapter 3 **97**

	COMBINATIONAL LOGIC DESIGN	97
3-1	Design Procedure	97
3-2	Beginning Hierarchical Design	104
3-3	Technology Mapping	107
3-4	Verification	111
	Manual Logic Analysis	111
	Simulation	113
3-5	Combinational Functional Blocks	113
3-6	Rudimentary Logic Functions	115
	Value-Fixing, Transferring, and Inverting	115
	Multiple-Bit Functions	116
	Enabling	119

3-7	Decoding	121
	Decoder and Enabling Combinations	124
	Decoder-Based Combinational Circuits	126
3-8	Encoding	127
	Priority Encoder	129
	Encoder Expansion	130
3-9	Selecting	131
	Multiplexers	131
	Multiplexer-Based Combinational Circuits	136
3-10	Chapter Summary	138
	References	140
	Problems	140

□ Chapter 4 **149**

ARITHMETIC FUNCTIONS AND HDLS		149
4-1	Iterative Combinational Circuits	150
4-2	Binary Adders	151
	Half Adder	151
	Full Adder	152
	Binary Ripple Carry Adder	153
4-3	Binary Subtraction	155
	Complements	157
	Subtraction Using 2s Complement	158
4-4	Binary Adder-Subtractors	159
	Signed Binary Numbers	161
	Signed Binary Addition and Subtraction	163
	Overflow	165
4-5	Other Arithmetic Functions	167
	Contraction	167
	Incrementing	169
	Decrementing	170
	Multiplication by Constants	170
	Division by Constants	172
	Zero Fill and Extension	172
4-6	Hardware Description Languages	173
	Hardware Description Languages	173
	Logic Synthesis	175
4-7	HDL Representations—VHDL	176
	Behavioral Description	186

4-8	HDL Representations—Verilog	187
	Behavioral Description	195
4-9	Chapter Summary	196
	References	196
	Problems	197

□ Chapter 5 **207**

SEQUENTIAL CIRCUITS	207
5-1 Sequential Circuit Definitions	208
5-2 Latches	210
SR and $\overline{S}\overline{R}$ Latches	211
D Latch	214
5-3 Flip-Flops	215
Master–Slave Flip-Flops	216
Edge-Triggered Flip-Flop	218
Standard Graphics Symbols	219
Direct Inputs	221
5-4 Sequential Circuit Analysis	222
Input Equations	223
State Table	224
State Diagram	227
Sequential Circuit Simulation	229
5-5 Sequential Circuit Design	230
Design Procedure	231
Finding State Diagrams and State Tables	231
State Assignment	238
Designing with D Flip-Flops	240
Designing with Unused States	243
Verification	245
5-6 Other Flip-Flop Types	247
JK and T Flip-Flops	247
5-7 State-Machine Diagrams and Applications	250
State-Machine Diagram Model	250
Constraints on Input Conditions	253
Design Applications Using State-Machine Diagrams	256
5-8 HDL Representation for Sequential Circuits—VHDL	264
5-9 HDL Representation for Sequential Circuits—Verilog	272
5-10 Chapter Summary	278
References	279
Problems	280

□ Chapter 6 **295**

SELECTED DESIGN TOPICS		295
6-1	The Design Space	295
	Integrated Circuits	296
	CMOS Circuit Technology	296
	Technology Parameters	302
6-2	Gate Propagation Delay	304
6-3	Flip-Flop Timing	306
6-4	Sequential Circuit Timing	308
6-5	Asynchronous Interactions	310
6-6	Synchronization and Metastability	312
6-7	Synchronous Circuit Pitfalls	318
6-8	Programmable Implementation Technologies	319
	Read-Only Memory	322
	Programmable Logic Array	323
	Programmable Array Logic Devices	327
6-9	Chapter Summary	329
	References	329
	Problems	330

□ Chapter 7 **335**

REGISTERS AND REGISTER TRANSFERS		335
7-1	Registers and Load Enable	336
	Register with Parallel Load	337
7-2	Register Transfers	339
7-3	Register Transfer Operations	341
7-4	A Note for VHDL and Verilog Users Only	344
7-5	Microoperations	344
	Arithmetic Microoperations	345
	Logic Microoperations	347
	Shift Microoperations	349
7-6	Microoperations on a Single Register	350
	Multiplexer-Based Transfers	350
	Shift Registers	353
	Ripple Counter	357
	Synchronous Binary Counters	359
	Other Counters	363

7-7	Register-Cell Design	366
7-8	Multiplexer and Bus-Based Transfers for Multiple Registers	372
	Three-State Bus	374
7-9	Serial Transfer and Microoperations	375
	Serial Addition	377
7-10	Control of Register Transfers	378
	Design Procedure	380
7-11	HDL Representation for Shift Registers and Counters—VHDL	395
7-12	HDL Representation for Shift Registers and Counters—Verilog	398
7-13	Microprogrammed Control	399
7-14	Chapter Summary	402
	References	402
	Problems	402

□ Chapter 8 **413**

MEMORY BASICS		413
8-1	Memory Definitions	413
8-2	Random-Access Memory	414
	Write and Read Operations	416
	Timing Waveforms	417
	Properties of Memory	419
8-3	SRAM Integrated Circuits	419
	Coincident Selection	422
8-4	Array of SRAM ICs	425
8-5	DRAM ICs	429
	DRAM Cell	429
	DRAM Bit Slice	431
8-6	DRAM Types	435
	Synchronous DRAM (SDRAM)	436
	Double-Data-Rate SDRAM (DDR SDRAM)	439
	RAMBUS® DRAM (RDRAM)	439
8-7	Arrays of Dynamic RAM ICs	440
8-8	Chapter Summary	441
	References	441
	Problems	441

□ Chapter 9 **443**

COMPUTER DESIGN BASICS	443
9-1 Introduction	444
9-2 Datapaths	444
9-3 The Arithmetic/Logic Unit	447
Arithmetic Circuit	448
Logic Circuit	450
Arithmetic/Logic Unit	451
9-4 The Shifter	453
Barrel Shifter	454
9-5 Datapath Representation	455
9-6 The Control Word	458
9-7 A Simple Computer Architecture	464
Instruction Set Architecture	464
Storage Resources	465
Instruction Formats	466
Instruction Specifications	468
9-8 Single-Cycle Hardwired Control	471
Instruction Decoder	472
Sample Instructions and Program	474
Single-Cycle Computer Issues	477
9-9 Multiple-Cycle Hardwired Control	478
Sequential Control Design	482
9-10 Chapter Summary	489
References	490
Problems	490

□ Chapter 10 **497**

INSTRUCTION SET ARCHITECTURE	497
10-1 Computer Architecture Concepts	497
Basic Computer Operation Cycle	498
Register Set	499
10-2 Operand Addressing	499
Three-Address Instructions	500
Two-Address Instructions	501
One-Address Instructions	501
Zero-Address Instructions	502
Addressing Architectures	503

10-3	Addressing Modes	506
	Implied Mode	507
	Immediate Mode	507
	Register and Register-Indirect Modes	508
	Direct Addressing Mode	508
	Indirect Addressing Mode	510
	Relative Addressing Mode	510
	Indexed Addressing Mode	511
	Summary of Addressing Modes	511
10-4	Instruction Set Architectures	513
10-5	Data-Transfer Instructions	514
	Stack Instructions	515
	Independent versus Memory-Mapped I/O	517
10-6	Data-Manipulation Instructions	518
	Arithmetic Instructions	518
	Logical and Bit-Manipulation Instructions	519
	Shift Instructions	520
10-7	Floating-Point Computations	522
	Arithmetic Operations	523
	Biased Exponent	524
	Standard Operand Format	525
10-8	Program Control Instructions	527
	Conditional Branch Instructions	528
	Procedure Call and Return Instructions	530
10-9	Program Interrupt	531
	Types of Interrupts	533
	Processing External Interrupts	534
10-10	Chapter Summary	535
	References	536
	Problems	537

□ Chapter 11 **543**

RISC AND CISC CENTRAL PROCESSING UNITS		543
11-1	Pipelined Datapath	544
	Execution of Pipeline Microoperations	548
11-2	Pipelined Control	549
	Pipeline Programming and Performance	551
11-3	The Reduced Instruction Set Computer	553
	Instruction Set Architecture	554
	Addressing Modes	557
	Datapath Organization	557

	Control Organization	560
	Data Hazards	563
	Control Hazards	570
11-4	The Complex Instruction Set Computer	574
	ISA Modifications	575
	Datapath Modifications	577
	Control Unit Modifications	577
	Microprogrammed Control	579
	Microprograms for Complex Instructions	582
11-5	More on Design	586
	Advanced CPU Concepts	586
	Recent Architectural Innovations	589
11-6	Chapter Summary	592
	References	593
	Problems	593

□ Chapter 12 **597**

	INPUT-OUTPUT AND COMMUNICATION	597
12-1	Computer I/O	597
12-2	Sample Peripherals	598
	Keyboard	598
	Hard Drive	599
	Liquid Crystal Display Screen	601
	I/O Transfer Rates	604
12-3	I/O Interfaces	604
	I/O Bus and Interface Unit	605
	Example of I/O Interface	606
	Strobing	608
	Handshaking	609
12-4	Serial Communication	611
	Synchronous Transmission	612
	The Keyboard Revisited	612
	A Packet-Based Serial I/O Bus	613
12-5	Modes of Transfer	617
	Example of Program-Controlled Transfer	618
	Interrupt-Initiated Transfer	620
12-6	Priority Interrupt	620
	Daisy Chain Priority	621
	Parallel Priority Hardware	623
12-7	Direct Memory Access	624
	DMA Controller	625
	DMA Transfer	627