1985年
世界集成电路大全

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上海交通大学微机研究所·南洋电脑开发总公司

1985年世界集成电路大全

2.数字器件

上海交通大学微机研究所　　南洋电脑开发总公司

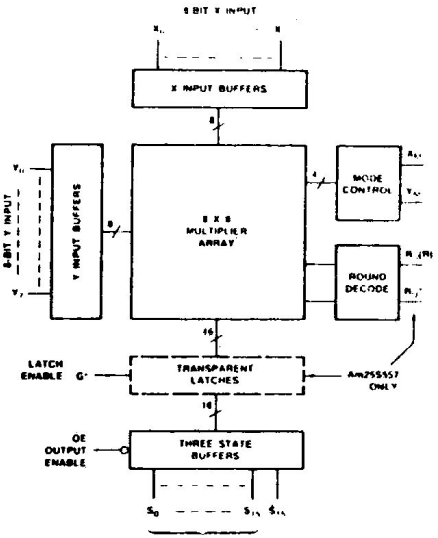
1985年10月

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
Digital Signal Processing Products

Am25S557/Am25S558 8-Bit by 8-Bit Combinatorial Multiplier

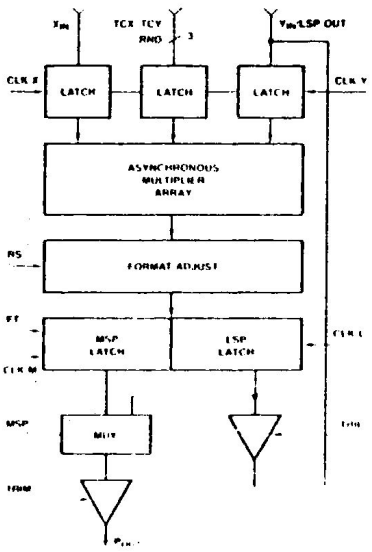
- Multiplies Two 8-Bit Numbers - 16-Bit Output
- Combinatorial - No Clocks Required
- Full 8 x 8 Multiply in 45ns (Typ)
- Cascades to 16 x 16 in 110ns (Typ)
- Expandable to Multiples of Eight Bits
- MSB and $\overline{\text{MSB}}$ Outputs for Easy Expansion
- Unsigned, Twos Complement or Mixed Operands
- Implements Common Rounding Algorithms with Additional Logic
- 3-State Outputs
- Transparent 16-Bit Latch in Am25S557
- Industry Standard Pinouts
- 40-Pin DIP



*Pin 11 is G for Am25S557 and R_U for Am25S558

Am29516/Am29517 and Am29L516/Am29L517 16 by 16 Combinatorial Multipliers

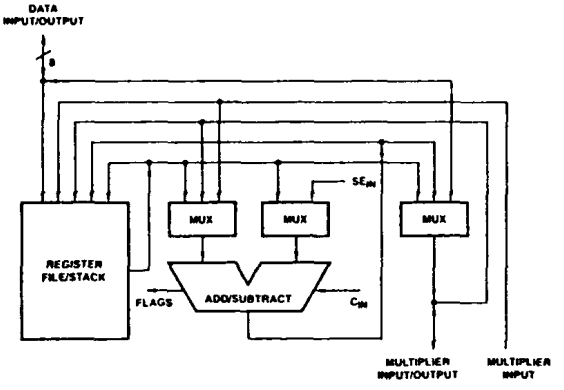
- High speed 16 x 16 parallel multiplier
- Two's complement, unsigned or mixed operands
- Full product multiplexed at output
- Am29516 pin and functionally compatible with TRW MPY-16HJ
- Am29517 optimized for microprogramming, single clock with register enables
- IMOX™ oxide isolated process
- Improved speed: 50ns clock multiply (1 devices)
- Reduced power dissipation 2W (L devices)
- TTL I/O, single +5V supply
- 64-pin package



SUPPORT PRODUCTS

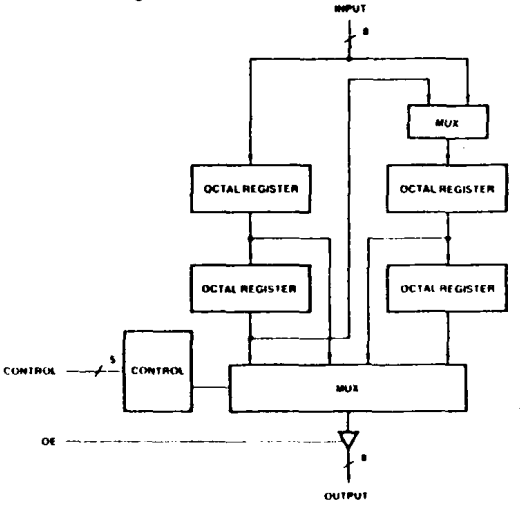
Am29501 Programmable Signal Processor

- 8-Bit Slice
- 8-Bit ALU
- Six 8-Bit Register File
- Designed to Operate with Am29516/Am29517
- 29-Bit Microcode Control
- Multiple Simultaneous Data Moves
- Supports 100ns Microcycle Time
- 64-Pin DIP



Am29520/Am29521 Multilevel Pipeline Register

- Four 8-Bit Vipeline Registers
- *All Registers Mux to Output*
- Programmable Pipeline – Dual 2-Stage or Single 4-Stage
- Am29520 Has Separate Load and Shift
- 24-Pin 0.3" Wide DIP

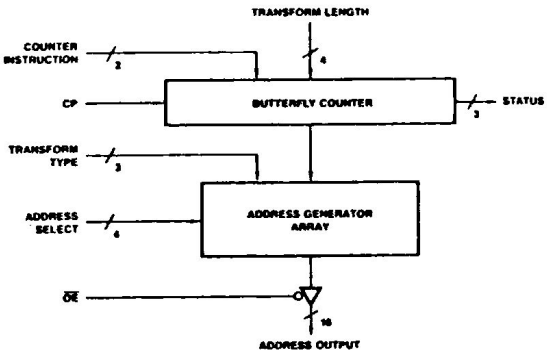


Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
Digital Signal Processing Products

Am29540 Programmable FFT Address Sequencer

- Generates Data/Coefficient Addresses
- Programmable Length – 2 to 65536 Point Transforms
- DIF or DIT Algorithms
- Bit-Reversed I or O (In-Place)
- Radix-2 or -4 Address Sequence
- Radix-2 RVI Transforms
- 40-Pin DIP



Advanced Micro Devices

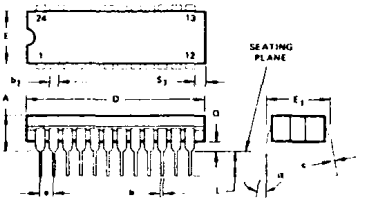
BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

DISTINCTIVE CHARACTERISTICS

- Standard I/O pin-out organization
- 48mA Commercial I_{OL}
- 32mA Mil I_{OL}
- Standard clock and output enable pin-outs
- 24-pin slim 0.3 inch wide *DIP* package
- IMOX Speed
  - 7.5ns typical CP to Y for registers
  - 4.0ns typical D to Y for buffers
- Wide data paths and flexible control
  - 10 bits for video or wide addresses
  - 9 bits for byte plus parity buses
  - 8-bit with multiple enables
- 100% Product assurance screening to MIL-STD-883 requirements

PHYSICAL DIMENSIONS
Dual-In-Line

D-24-SLIM



HERMETIC DUAL IN-LINE PACKAGE

AMD Pkg	D-24-Slim	
Common Name	SLIM CERDIP	
JEDEC Appendix C	-	
Parameters	Min	Max
A	140	220
b	018	020
b_1	045	065
c	009	011
D	1.270	1.285
E	245	285
E_1	290	320
e	090	110
L	120	150
Q	015	060
S_1	010	
α	3°	13°

FUNCTIONAL DESCRIPTION

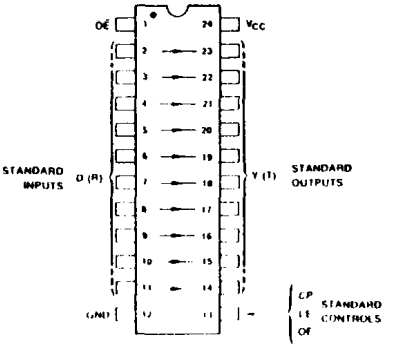
The Am29800 Family provides a completely standardized functional family of registers, latches, buffers, transceivers and parity check-and-regenerate functions optimized for bus interface applications. Each is packaged in the standard 24-pin x 0.3" wide *DIP package to allow LSI functionality in the minimum board area.* Board layout is eased by the standardization of inputs on the left and outputs on the right, directly across from each other. Output drive levels are standardized at 48mA Commercial and 32mA Military.

All functions are implemented in AMD's new proprietary IMOX™ (Implanted Micro OXide) process to provide the optimum in speed power product. Typical benchmark speeds are 7.5ns typical CP-to-Y for registers, and 4.0ns typical D-to-Y for buffers.

The basic 29800 Family functions are available in 10-bit, 9-bit and *8-bit configurations with broad control flexibility aimed at* minimizing the SSI/MSI content of LSI systems. The 10-bit devices make it easy to interface data plus controls or for 2 parts to interface 20-bit address lines. The 9 bits function are ideal for byte plus parity bus structures. The parity check-and-regenerate functions are designed for interfacing non-parity peripherals to parity organized buses.

All of the functional types have the pin-out format shown below.

STANDARDIZED PIN-OUTS FOR EASY BOARD LAYOUT



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Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29821/822/823/824/825/826

- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Noninverting CP-Y t_{PD} 7.5ns typ
  - Inverting CP-Y t_{PD} 7.5ns typ
- Buffered common Clock Enable ($\overline{EN}$)
- Buffered common asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24 pin 0.3" space saving package

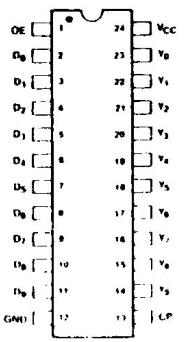
FUNCTIONAL DESCRIPTION

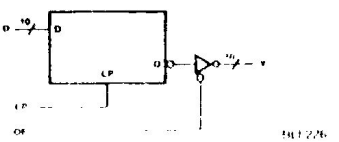
The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered 10-bit wide version of the popular 374 function. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the 823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

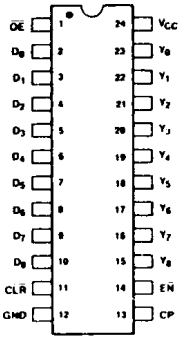
Am29821/Am29822
10-BIT REGISTERS



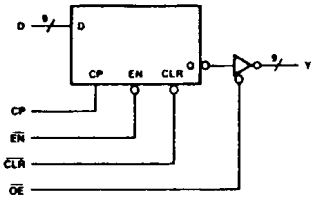


BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29823/Am29824
9-BIT REGISTERS

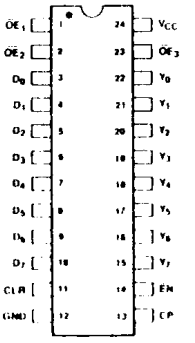


BLI-227

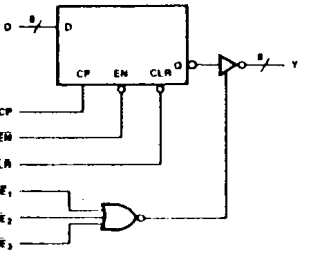


BLI-228

Am29825/Am29826
8-BIT REGISTERS



BLI-229



BLI-230

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29827/828,
Am29861/862/863/864

- High-speed symmetrical bidirectional transceivers
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- High speed buffers and inverters
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

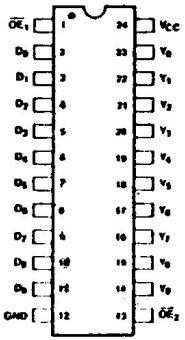
FUNCTIONAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers and Am29860 Series bus transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers and 9-bit transceivers have NOR ed output enables for maximum control flexibility. All buffer and transceiver data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

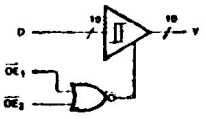
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit Buffers	10-Bit Transceivers	9-Bit Transceivers
Noninverting	Am29827	Am29861	Am29863
Inverting	Am29828	Am29862	Am29864

Am29827/Am29828
10-BIT BUS DRIVERS



BLI-237

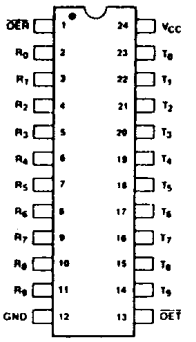


BLI-238

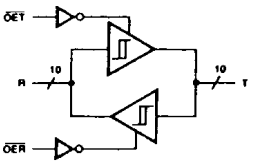
DIGITAL

Advanced Micro Devices

Am29861/Am29862
10-BIT TRANSCEIVERS

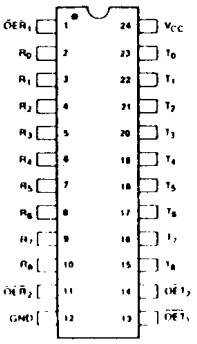


BLI-239

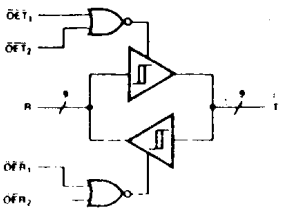


BLI-240

Am29863/Am29864
9-BIT TRANSCEIVERS



BLI-241



BLI-242

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29833/834

- High speed bidirectional transceivers for 8-bit non-parity to 9-bit with parity ports
  - Noninverting data t_{PD} = 6.0ns typ
  - Inverting data t_{PD} = 6.0ns typ
  - Parity generate t_{PD} = 9.0ns typ
- High speed parity generation for Transmit mode
- High speed parity fault detection for Receive mode
- Clearable, open-collector output, Fault Flag register
- 200mV minimum input hysteresis
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA Mil. I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

FUNCTIONAL DESCRIPTION

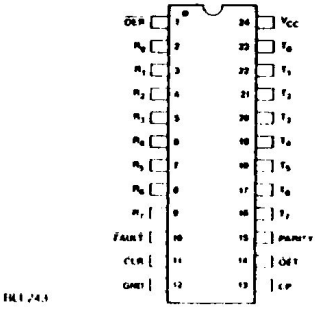
The Am29833 and Am29834 bidirectional transceivers are designed to interface an 8-bit data path without parity to a byte-parity 9-bit data path. All outputs – R_i, T_i and PARITY – have high I_{OL} drive capability and are ideal for device-to-bus or bus-to-bus interfacing.

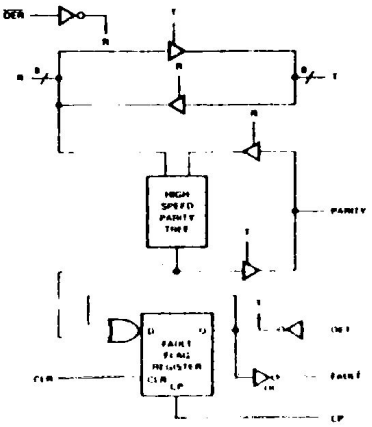
The internal $\overline{\text{FAULT}}$ flag register is configured as a "one's catcher" to capture and hold any odd parity fault occurring at the rising edge of the clock, CP. A registered $\overline{\text{FAULT}}$ output remains LOW until cleared. Also, the $\overline{\text{FAULT}}$ output is an open-collector output for wired-OR configurations where byte-parity is used for 16-bit or wider data buses or where multiple port flags are wired-OR tied together.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device
Noninverting	Am29833
Inverting	Am29834

Am29833/Am29834
8-BIT TO 9-BIT PARITY TRANSCEIVERS





BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29841/842/843/844/845/846

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 4.5ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable input
- Buffered common clear input
- Buffered common preset input
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

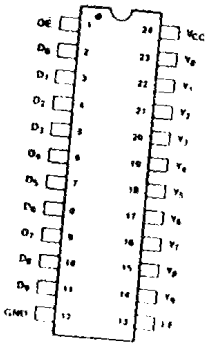
FUNCTIONAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide version of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

Am29841/Am29842
10-BIT LATCHES



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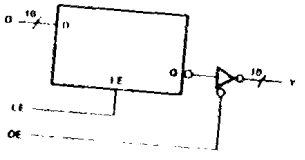
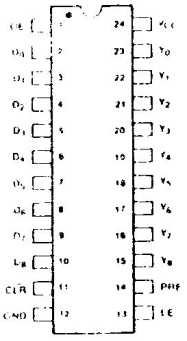


BLI 232

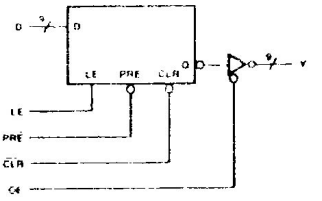
Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29843/Am29844
9 BIT LATCHES

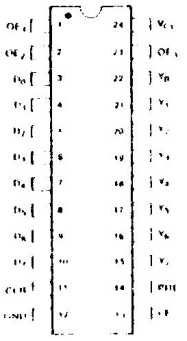


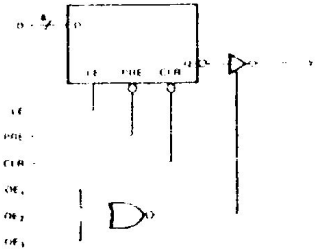
BLI 213



BLI 234

Am29845/Am29846
8-BIT LATCHES





BLI 236

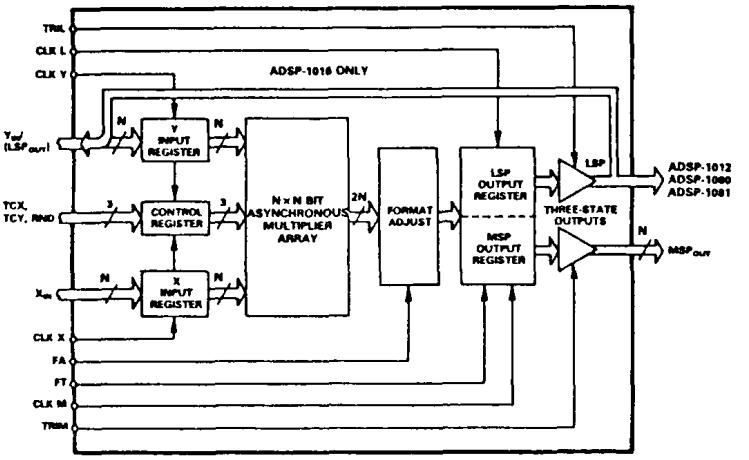
ANALOG DEVICES

CMOS MULTIPLIERS

Analog Devices offers a full line of high-speed CMOS digital multipliers for use in high-performance digital signal/array processors. The 8-, 12-, and 16-bit devices are fully compatible with industry standard units; also, a proprietary 24-bit multiplier is available. Alternative speed grades are offered, as well as a variety of package types. Full 883B processing is supported.

8-, 12-, and 24-bit devices are in production in a five micron CMOS process. In addition, Analog Devices is currently producing 16-bit multipliers in a 1.5 micron CMOS process (denoted the ADSP-1016A), allowing blazing speed to be combined with ultra low power. During the coming year, other models will be introduced in this 1.5 micron process.

ADSP-1016 FUNCTIONAL BLOCK DIAGRAM



Model	Bit Size	Multiply Time (ns) +25°C/Over T_{amb}	Power Dissipation	Package	Temp. Range[1]	Notes
ADSP-1080JD[2]	8 × 8	100/115	75mW	40-Pin DIP	C	Two's Complement Only
ADSP-1080KD	8 × 8	85/100	75mW	"	C	Two's Complement Only
ADSP-1080SD/883B	8 × 8	100/130	100mW	"	E	Two's Complement Only
ADSP-1080TD/883B	8 × 8	85/115	100mW	"	E	Two's Complement Only
ADSP-1081JD	8 × 8	100/105	75mW	40-Pin DIP	C	Unsigned Magnitude Only
ADSP-1081KD	8 × 8	85/100	75mW	"	C	Unsigned Magnitude Only
ADSP-1081SD/883B	8 × 8	100/130	100mW	"	E	Unsigned Magnitude Only
ADSP-1081TD/883B	8 × 8	85/115	100mW	"	E	Unsigned Magnitude Only
ADSP-1012JD[2]	12 × 12	140/165	125mW	64-Pin DIP[3]	C	
ADSP-1012KD	12 × 12	110/130	125mW	"	C	
ADSP-1012SD/883B	12 × 12	140/195	150mW	"	E	
ADSP-1012TD/883B	12 × 12	110/150	150mW	"	E	
ADSP-1016AJD	16 × 16	75/90	175mW	64-Pin DIP[3]	C	
ADSP-1016AKD	16 × 16	65/75	175mW	"	C	
ADSP-1016ASD/883B	16 × 16	75/105	200mW	"	E	
ADSP-1016ATD/883B	16 × 16	65/90	200mW	"	E	
ADSP-1024KD	24 × 24	145/200	200mW	84-PGA	C	
ADSP-1024JD	24 × 24	185/250	200mW	"	C	

NOTES
[1]C = Commercial (0 to +70°C), E = Extended (−55°C to +125°C ambient
[2]"A" versions of the ADSP-1080 and ADSP-1012 will be available 1Q85
[3]ADSP-1012 and ADSP-1016 are also available in 68 Terminal Ceramic Leadless Chip Carrier and 68 Pin Grid Array

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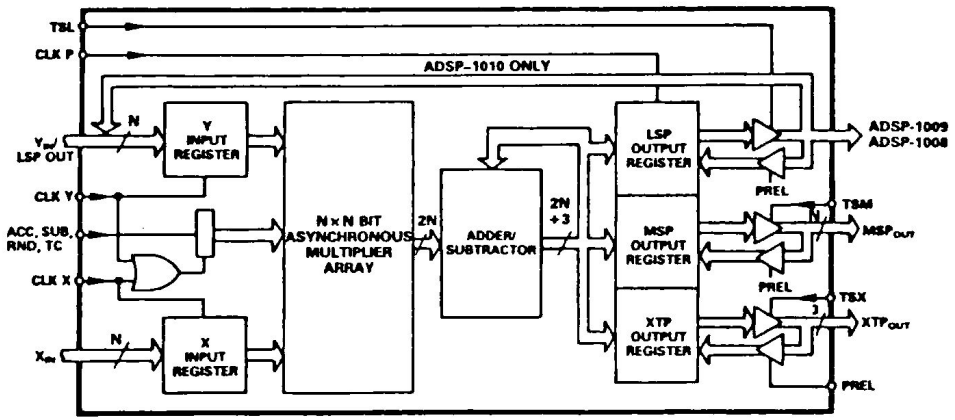
ANALOG DEVICES

CMOS MULTIPLIER/ACCUMULATORS

Analog Devices offers a full line of high-speed CMOS digital multiplier/accumulators for use in high-performance digital signal/array processors. These 8-, 12-, and 16-bit devices are fully compatible with industray standard units, while consuming 1/20th the power. Alternative speed grades are offered as well as a variety of package types. Full 883B processing is supported.

As the table below indicates, the 8 × 8 and 16 × 16 multiplier/accumulators are now being produced in a 1.5 micron CMOS process (denoted ADSP-1008A and ADSP-1010A), yielding extremely fast, low-power DSP devices. During the coming year, the ADSP-1009 will also be introduced in the 1.5 micron process.

ADSP-1010 FUNCTIONAL BLOCK DIAGRAM



Model	Bit Size	Multiply Accumulate Time (ns) +25°C/Over T_{amb}	Power Dissipation	Package	Temp. Range[1]
ADSP-1008AJD	8 × 8	55/65	75mW	48-Pin DIP	C
ADSP-1008AKD	8 × 8	45/55	75mW	"	C
ADSP-1008ASD/883B	8 × 8	55/80	100mW	"	E
ADSP-1008ATD/883B	8 × 8	45/65	100mW	"	E
ADSP-1009JD[2]	12 × 12	165/195	125mW	64-Pin DIP[3]	C
ADSP-1009KD	12 × 12	130/155	125mW	"	C
ADSP-1009SD/883B	12 × 12	165/225	150mW	"	E
ADSP-1009TD/883B	12 × 12	130/180	150mW	"	E
ADSP-1010AJD	16 × 16	95/115	175mW	64-Pin DIP[3]	C
ADSP-1010AKD	16 × 16	80/95	175mW	"	C
ADSP-1010ASD/883B	16 × 16	95/135	200mW	"	E
ADSP-1010ATD/883B	16 × 16	80/110	200mW	"	E

NOTES
[1]C - Commercial 0 to +70°C, E - Extended -55°C to +125°C ambient
[2]"A" versions of the ADSP-1009 will be available in 1Q85
[3]ADSP-1009 and ADSP-1010 are also available in 68-Terminal Ceramic Leadless Chip Carrier and 68-Pin Grid Array

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ANALOG DEVICES

16 × 16-Bit CMOS Single Port Multiplier/Accumulator

ADSP-1110

The ADSP-1110 is a high-speed, low-power single-port 16 × 16-bit multiplier/accumulator (MAC), with processing throughput comparable to existing three-port MAC's. Its single-bus structure offers unique advantages: more compact packaging in a 28-pin DIP; simpler system interface to single-bus peripherals; and, significantly reduced cost. In addition, innovative on-chip features extend the ADSP-1110's capabilities and eliminate external hardware.

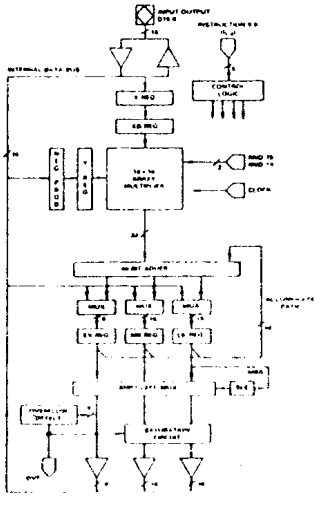
All inputs to and outputs from the ADSP-1110 pass through its single 16-bit I/O port. All I/O operations are single cycle. A multiply or MAC operation requires two cycles to complete—consistent with the two cycles required to load input pairs to the multiplier. An internal pipeline register enables a new input to be loaded as the previous multiply/accumulate is computed—allowing the device's full 5MHz computational bandwidth to be utilized.

A six-bit microcode instruction word governs the ADSP-1110's operation. The instruction set centers around I/O and multiply/accumulate operations. Additional instructions allow extra precision in single and double precision operations to be obtained efficiently.

Multiplier products are accumulated in a 40-bit wide Multiplier Result (MR) register, which consists of a 16-bit MS (Most Significant) and LS (Least Significant) register, and an 8-bit EX (Extension) register. Either multiplier input can be a two's complement or unsigned magnitude number. Overflow from the lower 32 bits of the MR into the upper eight guard bits is detected and can be monitored externally. Outputs can, conditional upon overflow status, be saturated to full scale. An MR register can be shifted left by one bit upon output; two independent controls allow rounding consistent with output formatting.

The ADSP-1110 is optimal for applications where board space is limited but the performance of a DSP processor is required. In addition, a microprocessor-based system can realize greater throughput by utilizing the ADSP-1110 as an accelerator.

ADSP-1110 FUNCTIONAL BLOCK DIAGRAM



Model	Multiply Accumulate Time (ns) +25°C/Over T_{amb}	Power Dissipation	Package	Temp. Range[1]
ADSP-1110JD	205/240	225mW	28 Pin DIP	C
ADSP-1110KD	165/190	225mW	"	C
ADSP-1110SD/883B	180/250	250mW	"	E
ADSP-1110TD/883B	165/225	250mW	"	E

NOTE
[1]C = Commercial 0 to +70°C; E = Extended −55°C to +125°C ambient

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