英文版



数字系统设计与VHDL

Digital Systems Design with VHDL

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Charles H. Roth, Jr. Lizy Kurian John

著

梁松海 改编

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(英文版)

Digital Systems Design with VHDL

電子工業出版社・ Publishing House of Electronics Industry 北京・BEIJING 本书对原著进行了结构调整,使之更适合作为本科双语教学教材。第1章首先回顾了逻辑设计基本原理,第2章和第3章分别讲解了VHDL基本知识和高级主题,第4章为简单设计实例,第5章讨论状态机,第6章讨论浮点数运算,第7章讨论硬件测试和可测试性设计,第8章给出了一些高级设计实例。全书将工业标准硬件描述语言VHDL和数字系统设计融为一体,较好地实现了控制逻辑和运算部件的整合设计,并给出了多个设计实例,便于学生在实践中得到提高。

本书适合作为高等院校电子、电气和计算机专业本科生数字系统设计类课程的双语教学教材,也适合作为相关工程技术人员的参考书。

Charles H. Roth, Jr. & Lizy Kurian John

DIGITAL SYSTEMS DESIGN WITH VHDL

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2001年7月间,电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师,商量引进国外教材问题。与会同志对出版社提出的计划十分赞同,大家认为,这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材,意味着开设了一门好的课程,甚至可能预示着一个崭新学科的诞生。20世纪40年代 MIT 林肯实验室出版的一套 28 本雷达丛书,对近代电子学科、特别是对雷达技术的推动作用,就是一个很好的例子。

我国领导部门对教材建设一直非常重视。20世纪80年代,在原教委教材编审委员会的领导下,汇集了高等院校几百位富有教学经验的专家,编写、出版了一大批教材;很多院校还根据学校的特点和需要,陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来,随着教学改革不断深入和科学技术的飞速进步,有的教材内容已比较陈旧、落后,难以适应教学的要求,特别是在电子学和通信技术发展神速、可以讲是日新月异的今天,如何适应这种情况,更是一个必须认真考虑的问题。解决这个问题,除了依靠高校的老师和专家撰写新的符合要求的教科书外,引进和出版一些国外优秀电子与通信教材,尤其是有选择地引进一批英文原版教材,是会有好处的。

一年多来,电子工业出版社为此做了很多工作。他们成立了一个"国外电子与通信教材系列"项目组,选派了富有经验的业务骨干负责有关工作,收集了230余种通信教材和参考书的详细资料,调来了100余种原版教材样书,依靠由20余位专家组成的出版委员会,从中精选了40多种,内容丰富,覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面,既可作为通信专业本科生和研究生的教学用书,也可作为有关专业人员的参考材料。此外,这批教材,有的翻译为中文,还有部分教材直接影印出版,以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里,我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度,充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步,对高校教学工作会不断提出新的要求和希望。我想,无论如何,要做好引进国外教材的工作,一定要联系我国的实际。教材和学术专著不同,既要注意科学性、学术性,也要重视可读性,要深入浅出,便于读者自学;引进的教材要适应高校教学改革的需要,针对目前一些教材内容较为陈旧的问题,有目的地引进一些先进的和正在发展中的交叉学科的参考书;要与国内出版的教材相配套,安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求,希望它们能放在学生们的课桌上,发挥一定的作用。

最后,预祝"国外电子与通信教材系列"项目取得成功,为我国电子与通信教学和通信产业的 发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题,提出意见和 建议,以便再版时更正。

美佑寿

中国工程院院士、清华大学教授 "国外电子与通信教材系列"出版委员会主任

出版说明

进人21世纪以来,我国信息产业在生产和科研方面都大大加快了发展速度,并已成为国民经济发展的支柱产业之一。但是,与世界上其他信息产业发达的国家相比,我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天,我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社,我们始终关注着全球电子信息技术的发展方向,始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间,我社先后从世界著名出版公司引进出版了40余种教材,形成了一套"国外计算机科学教材系列",在全国高校以及科研部门中受到了欢迎和好评,得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材,尤其是有选择地引进一批英文原版教材,将有助于我国信息产业培养具有国际竞争能力的技术人才,也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于"十五"期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见,我们决定引进"国外电子与通信教材系列",并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商,其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等,其中既有本科专业课程教材,也有研究生课程教材,以适应不同院系、不同专业、不同层次的师生对教材的需求,广大师生可自由选择和自由组合使用。我们还将与国外出版商一起,陆续推出一些教材的教学支持资料,为授课教师提供帮助。

此外,"国外电子与通信教材系列"的引进和出版工作得到了教育部高等教育司的大力支持和帮助,其中的部分引进教材已通过"教育部高等学校电子信息科学与工程类专业教学指导委员会"的审核,并得到教育部高等教育司的批准,纳入了"教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书"。

为做好该系列教材的翻译工作,我们聘请了清华大学、北京大学、北京邮电大学、南京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学、中山大学、哈尔滨工业大学、西南交通大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望,具有丰富的教学经验,他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外,对于编辑的选择,我们达到了专业对口;对于从英文原书中发现的错误,我们通过与作者联络、从网上下载勘误表等方式,逐一进行了修订;同时,我们对审校、排版、印制质量进行了严格把关。

今后,我们将进一步加强同各高校教师的密切关系,努力引进更多的国外优秀教材和教学参考书,为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足,在选题、翻译、出版等方面的工作中还有许多需要改进的地方,恳请广大师生和读者提出批评及建议。

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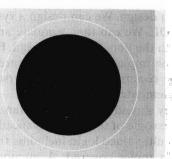
改编者序

本书是在 Digital Systems Design Using VHDL, Second Edition 的基础上改编的英文版教材(改后英文书名为 Digital Systems Design with VHDL),适用于本科高年级学生和研究生针对数字系统进行 VHDL 设计与实现的英语或双语教学使用。

本书作者Charles H. Roth, Jr.是美国斯坦福大学博士,1961年就职于得克萨斯大学奥斯汀分校,目前是电气与计算机工程系教授。他的授课和研究领域涵盖了数字系统理论和设计、微计算机系统和VHDL应用,出版了4本著作。作者在手工电路设计和基于硬件描述语言的电路系统设计领域积累了深厚的工作经验和教学经历,以电路系统设计为核心来开展VHDL教学是本书区别于一般专注于VHDL语言文法讲解教材的显著特点,受到了使用者的高度评价。

Digital Systems Design Using VHDL, Second Edition 的内容体系与国内高校数字系统设计相关课程的教学内容和课程安排存在一些不匹配之处,其中可编程逻辑器件简介和FPGA设计部分的内容,已有专门的课程讲授,微程序设计和RISC微处理器设计部分,需要计算机体系结构设计相关课程作为先导,并有专门的课程讲授(对这些内容感兴趣的读者可参阅电子工业出版社所出中文版《数字系统设计与VHDL(第二版)》,ISBN: 978-7-121-06728-0)。为了更好地突出本书在数字系统设计方面的特色,我们将这两部分的内容进行了删除,同时对原著进行了结构调整,使之更适合作为本科双语教学教材。其中第1章首先回顾了逻辑设计基本原理,第2章和第3章分别讲解了VHDL基本知识和高级主题,第4章为简单设计实例,第5章讨论状态机,第6章讨论浮点数运算,第7章讨论硬件测试和可测试性设计,第8章给出了一些高级设计实例。

改编后的版本虽经反复推敲,但由于改编者水平有限,书中仍难免有不妥之处,恳请广大同行和读者给予指正(敬请致函liangsh@szu.edu.cn),以便进一步提高本书的质量,更好地推动双语教学。



Preface

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This textbook is intended for a senior-level course in digital systems design. The book covers both basic principles of digital system design and the use of a hardware description language, VHDL, in the design process. After basic principles have been covered, design is best taught by using examples. For this reason, many digital system design examples, ranging in complexity from a simple binary adder to a microprocessor, are included in the text.

Students using this textbook should have completed a course in the fundamentals of logic design, including both combinational and sequential circuits. Although no previous knowledge of VHDL is assumed, students should have programming experience using a modern high-level language such as C.

Because students typically take their first course in logic design two years before this course, most students need a review of the basics. For this reason, Chapter 1 includes a review of logic design fundamentals. Most students can review this material on their own, so it is unnecessary to devote much lecture time to this chapter. However, a good understanding of timing in sequential circuits and the principles of synchronous design is essential to the digital system design process.

Chapter 2 starts with an overview of modern design flow. It also summarizes various technologies for implementation of digital designs. Then, it introduces the basics of VHDL, and this hardware description language is used throughout the rest of the book. Additional features of VHDL are introduced on an as-needed basis, and more advanced features are covered in Chapter 3. From the start, we relate the constructs of VHDL to the corresponding hardware. Some textbooks teach VHDL as a programming language and devote many pages to teaching the language syntax. Instead, our emphasis is on how to use VHDL in the digital design process. The language is very complex, so we do not attempt to cover all its features. We emphasize the basic features that are necessary for digital design and omit some of the less-used features. Use of standard IEEE VHDL libraries is introduced in this chapter and only IEEE standard libraries are used throughout the text.

VHDL is very useful in teaching top-down design. We can design a system at a high level and express the algorithms in VHDL. We can then simulate and debug the designs at this level before proceeding with the detailed logic design. However, no design is complete until it has actually been implemented in hardware and the hardware has been tested. For this reason, we recommend that the course include some lab exercises in which designs are implemented in hardware.

By the time students reach Chapter 3, they should be thoroughly familiar with the basics of VHDL. At this point we introduce some of the more advanced features of VHDL and illustrate their use. The use of multi-valued logic, including the IEEE-1164 standard logic, is one of the important topics covered. A memory model with tri-state output busses is presented to illustrate the use of the multi-valued logic.

Chapter 4 presents a variety of design examples, including both arithmetic and non-arithmetic examples. Simple examples such as a BCD to 7-segment display decoder to more complex examples such as game scoreboards, keypad scanners and binary dividers are presented. The chapter presents common techniques used for computer arithmetic, including carry look-ahead addition, and binary multiplication and division. Use of a state machine for sequencing the operations in a digital system is an important concept presented in this chapter. Synthesizable VHDL code is presented for the various designs. A variety of examples are presented so that instructors can select their favorite designs for teaching.

Use of sequential machine charts (SM charts) as an alternative to state graphs is presented in Chapter 5. We show how to write VHDL code based on SM charts and how to realize hardware to implement the SM charts. Then, the technique of microprogramming is presented. Transformation of SM charts for different types of microprogramming is discussed. Then, we show how the use of linked state machines facilitates the decomposition of complex systems into simpler ones. The design of a dice-game simulator is used to illustrate these techniques.

Basic techniques for floating-point arithmetic are described in Chapter 6. A simple floating-point format with 2's complement numbers is presented and then the IEEE standard floating-point formats are presented. A floating-point multiplier example is presented starting with development of the basic algorithm, then simulating the system using VHDL, and finally synthesizing and implementing the system using an FPGA.

The important topics of hardware testing and design for testability are covered in Chapter 7. This chapter introduces the basic techniques for testing combinational and sequential logic. Then scan design and boundary-scan techniques, which facilitate the testing of digital systems, are described. The chapter concludes with a discussion of built-in self-test (BIST). VHDL code for a boundary-scan example and for a BIST example is included. The topics in this chapter play an important role in digital system design, and we recommend that they be included in any course on this subject. Chapter 7 can be covered any time after the completion of Chapter 3.

Chapter 8 presents three complete design examples that illustrate the use of VHDL synthesis tools. First, a wristwatch design is presented. It shows the progress of a design from a textual description to a state diagram and then a VHDL model. This example illustrates modular design. The test bench for the wristwatch illustrates the use of multiple procedure calls to facilitate the testing. The second example describes the use of VHDL to model RAM memories. The third example, a serial communications receiver-transmitter, should easily be understood by any student who has completed the material through Chapter 3.

This book is the result of many years of teaching a senior course in digital systems design at the University of Texas at Austin. Throughout the years, the technology for hardware implementation of digital systems has kept changing, but many of the same design principles are still applicable. In the early years of the course, we handwired modules consisting of discrete transistors to implement our designs. Then integrated circuits were introduced, and we were able to implement our designs using breadboards and TTL logic. Now we are able to use FPGAs and CPLDs to realize very complex designs. We originally used our own hardware description language together with a simulator running on a mainframe computer. When PCs came along, we wrote an improved hardware description language and implemented a simulator that ran on PCs. When VHDL was adopted as an IEEE standard and became widely used in industry, we switched to VHDL. The widespread availability of high-quality commercial CAD tools now enables us to synthesize complex designs directly from the VHDL code.

All of the VHDL code in this textbook[®] has been tested using the ModelSim simulator. The ModelSim software is available in a student edition, and we recommend its use in conjunction with this text. The CD that accompanies this text provides a link for downloading the ModelSim student edition and an introductory tutorial to help students get started using the software. All of the VHDL code in this textbook is available on the CD. The CD also contains two software packages, LogicAid and SimUaid, which are useful in teaching digital system design. Instruction manuals and examples of using this software are on the CD.

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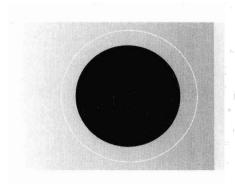
① 书中提及的 VHDL 代码及其他光盘内容均可从华信教育资源网(www.hxedu.com.cn)下载。

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Chapter 6 Floating-Point Arithmetic



Review of Logic Design Fundamentals

This chapter reviews many of the logic design topics normally taught in a first course in logic design. Some of the review examples that follow are referenced in later chapters of this text. For more details on any of the topics discussed in this chapter, the reader should refer to a standard logic design textbook such as Roth, Fundamentals of Logic Design, 5th Edition (Thomson Brooks/Cole, 2004). First, we review combinational logic and then sequential logic. Combinational logic has no memory, so the present output depends only on the present input. Sequential logic has memory, so the present output depends not only on the present input but also on the past sequence of inputs. The sections on sequential circuit timing and synchronous design are particularly important, since a good understanding of timing issues is essential to the successful design of digital systems.

1.1 Combinational Logic

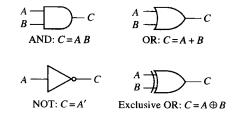
Some of the basic gates used in logic circuits are shown in Figure 1-1. Unless otherwise specified, all the variables that we use to represent logic signals will be two-valued, and the two values will be designated 0 and 1. We will normally use positive logic, for which a low voltage corresponds to a logic 0 and a high voltage corresponds to a logic 1. When negative logic is used, a low voltage corresponds to a logic 1 and a high voltage corresponds to a logic 0.

For the AND gate of Figure 1-1, the output C=1 if and only if the input A=1 and the input B=1. We will use a raised dot or simply write the variables side by side to indicate the AND operation; thus C=A AND $B=A\cdot B=AB$. For the OR gate, the output C=1 if and only if the input A=1 or the input B=1 (inclusive OR). We will use C=1 to indicate the OR operation; thus C=1 OR C=1 OR and if C=1 OR and C=1 OR are an an output C=1 if C=1 OR and C=1 OR and C=1 OR and C=1 OR are an an output C=1 OR and C=1 OR are an an output C=1 OR and C=1 OR an are an an output C=1 OR an are an an output C=1 OR are an are an

$$C = A \text{ XOR } B = AB' + A'B = A \oplus B \tag{1-1}$$

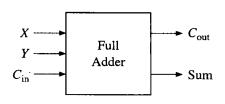
The behavior of a combinational logic circuit can be specified by a truth table that gives the circuit outputs for each combination of input values. As an example,

FIGURE 1-1: Basic Gates



consider the full adder of Figure 1-2, which adds two binary digits (X and Y) and a carry ($C_{\rm in}$) to give a sum (Sum) and a carry out ($C_{\rm out}$). The truth table specifies the adder outputs as a function of the adder inputs. For example, when the inputs are X=0, Y=0 and $C_{\rm in}=1$, adding the three inputs gives 0+0+1=01, so the sum is 1 and the carry out is 0. When the inputs are 011, 0+1+1=10, so Sum=0 and $C_{\rm out}=1$. When the inputs are $X=Y=C_{\rm in}=1$, 1+1+1=11, so Sum=1 and $C_{\rm out}=1$.

FIGURE 1-2: Full Adder



X	Y	C_{in}	$C_{ m out}$	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Full adder module

(b) Truth table

We will derive algebraic expressions for Sum and C_{out} from the truth table. From the table, Sum=1 when X=0, Y=0, and $C_{in}=1$. The term $X'Y'C_{in}$ equals 1 only for this combination of inputs. The term $X'YC'_{in}=1$ only when X=0, Y=1, and $C_{in}=0$. The term $XY'C'_{in}$ is 1 only for the input combination X=1, Y=0, and $C_{in}=0$. The term XYC'_{in} is 1 only when $X=Y=C_{in}=1$. Therefore, Sum is formed by ORing these four terms together:

$$Sum = X'Y'C_{in} + X'YC'_{in} + XY'C'_{in} + XYC_{in}$$
 (1-2)

Each of the terms in this sum of products (SOP) expression is 1 for exactly one combination of input values. In a similar manner, $C_{\rm out}$ is formed by ORing four terms together:

$$C_{\text{out}} = X'YC_{\text{in}} + XY'C_{\text{in}} + XYC'_{\text{in}} + XYC_{\text{in}}$$
 (1-3)

Each term in Equations (1-2) and (1-3) is referred to as a *minterm*, and these equations are referred to as *minterm expansions*. These minterm expansions can also be written in *m*-notation or decimal notation as follows:

Sum =
$$m_1 + m_2 + m_4 + m_7 = \sum m(1, 2, 4, 7)$$

 $C_{\text{out}} = m_3 + m_5 + m_6 + m_7 = \sum m(3, 5, 6, 7)$

The decimal numbers designate the rows of the truth table for which the corresponding function is 1. Thus Sum = 1 in rows 001, 010, 100, and 111 (rows 1, 2, 4, 7).

A logic function can also be represented in terms of the inputs for which the function value is 0. Referring to the truth table for the full adder, $C_{\text{out}} = 0$ when $X = Y = C_{\text{in}} = 0$. The term $(X + Y + C_{\text{in}})$ is 0 only for this combination of inputs. The term $(X + Y + C_{\text{in}})$ is 0 only when X = Y = 0 and $C_{\text{in}} = 1$. The term $(X + Y' + C_{\text{in}})$ is 0 only when $X = C_{\text{in}} = 0$ and Y = 1. The term $(X' + Y + C_{\text{in}})$ is 0 only when X = 1 and $Y = C_{\text{in}} = 0$. C_{out} is formed by ANDing these four terms together:

$$C_{\text{out}} = (X + Y + C_{\text{in}})(X + Y + C_{\text{in}}')(X + Y' + C_{\text{in}})(X' + Y + C_{\text{in}})$$
 (1-4)

 $C_{\rm out}$ is 0 only for the 000, 001, 010, and 100 rows of the truth table and, therefore, must be 1 for the remaining four rows. Each of the terms in the Product of Sums (POS) expression in Equation (1-4) is referred to as a *maxterm*, and (1-4) is called a *maxterm* expansion. This maxterm expansion can also be written in decimal notation as

$$C_{\text{out}} = M_0 \cdot M_1 \cdot M_2 \cdot M_4 = \Pi M(0, 1, 2, 4)$$

where the decimal numbers correspond to the truth table rows for which $C_{\rm out} = 0$.

1.2 Boolean Algebra and Algebraic Simplification

The basic mathematics used for logic design is Boolean algebra. Table 1-1 summarizes the laws and theorems of Boolean algebra. They are listed in dual pairs; for example, Equation (1-10D) is the dual of (1-10). They can be verified easily for two-valued logic by using truth tables. These laws and theorems can be used to simplify logic functions so they can be realized with a reduced number of components.

A very important law in Boolean algebra is the *DeMorgan's law*. DeMorgan's laws stated in Equations (1-16, 1-16D) can be used to form the complement of an expression on a step-by-step basis. The generalized form of DeMorgan's law in Equation (1-17) can be used to form the complement of a complex expression in one step. Equation (1-17) can be interpreted as follows: To form the complement of a Boolean expression, replace each variable by its complement; also replace 1 with 0, 0 with 1, OR with AND, and AND with OR. Add parentheses as required to assure the proper hierarchy of operations. If AND is performed before OR in F, then parentheses may be required to assure that OR is performed before AND in F'.

Example

Find the complement of F if

$$F = X + E'K (C (AB + D') \cdot 1 + WZ' (G'H + 0))$$

$$F' = X' (E + K' + (C' + (A' + B') D + 0) (W' + Z + (G + H') \cdot 1))$$

Additional parentheses in F' were added when an AND operation in F was replaced with an OR. The dual of an expression is the same as its complement, except that the variables are not complemented.