专业英语阅读

计算机专业英语

（第3版）

ENGLISH FOR COMPUTER

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哈尔滨工业大学出版社

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内 容 提 要

本文通过计算机各领域知识的介绍，使学生了解和掌握常用的计算机专业英语词汇。书中内容包括微机结构、算法语言、数据库、编译系统、操作系统、网络协议、多媒体技术、Windows 98 及超文本标志语言 HTML4 等方面的知识。书后附有常用计算机专业英语词汇表、参考译文和在国际刊物上发表论文的英文样本。

本书可作为计算机专业的计算机专业英语课教材，也可供有关计算机专业的科研、教学人员、计算机应用人员以及计算机爱好者使用。

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第三版前言

随着计算机的普及，计算机专业英语已逐渐成为计算机专业的一门必修课，为配合大学本、专科计算机专业的英语教学，我们哈尔滨工业大学计算机科学与工程系部分授课教师编写了这本书。

本书的编写目的首先是让学生掌握计算机专业英语的基本专业术语，同时是为了使学生了解一些计算机专业的基本知识。

本书问世多年来，得到各方同仁和读者的厚爱与支持，值此再版之机，深表谢意。

为了适应计算机技术的迅猛发展，本书已修订多次并增加许多新内容，此次再版增加的是 Windows 98、超文本标志语言 HTML4 内容和一篇加拿大作者英文论文原本。

本书的后半部是各章的参考译文，学生可参考这些译文理解原文。书末附有常用的专业术语，以便学生阅读、翻译和写作英文文章时查阅。

本书的第 1、2 章和第 11 章由吴岩编写；第 3、4 章由李秀坤编写；第 5、6、9、10 章由王开铸编写；第 7、8 章由刘挺编写。全书由王开铸统稿、定稿。

作者深感出一本高质量的书，需作者与读者双方面的努力和培植，因此，真诚希望广大读者多提宝贵意见。

作　者

2002 年 1 月

于哈尔滨工业大学

目　录

CHAPTER 1 The 8086 Primer

1.1 Overview

The 8086 has four sets of registers. The first set contains general registers that are used to hold intermediate results. The second set contains pointer and index registers that are used to locate information within a specified portion of memory. The third set contains segment registers that are used to specify these portions of memory, and the fourth set contains the instruction pointer. There are also nine flags in the 8086. These flags are used to record the state of the processor and to control its operation. The 8086 can access up to 1 000 000 bytes of memory and up to 65 000 input or output ports.

The 8086 is a single integrated-circuit chip containing most of the components that make up a computer. The chip also contains all of the registers and flags. The memory and input/output ports are not contained on the chip, but they can be easily connected to the chip to form a computer.

Typical computer instructions involve locating designated operands (data to be processed), performing an operation on the values of these operands, and storing the result back into a designated result location. The locations of the operands and the result can be either in memory or in a register as designated by the instruction.

The memory in an 8086 system is a sequence of up to 2^{20} 8-bit quantities called bytes. Each byte is assigned a unique address ranging from 0

to $2^{20}-1$. Any two consecutive bytes in memory are defined as a word. Each byte in a word has a byte address, and the smaller of these two addresses is used as the address of the word.

The 8086 has some instructions that access (read or write) bytes and other instructions that access words. For the 8086, the amount of information which transfers to or from memory at one time is always 16-bits. In the case of byte instructions, only eight of those bits are used and the other eight are ignored. The 16-bits are always the contents of two consecutive bytes in memory starting with a byte at an even address.

Since the 8086 can address up to 2^{20} bytes of memory, it would seem that within the 8086 processor, byte and word address must be represented as 20-bit quantities. In fact, the 8086 was designed to perform 16-bit arithmetic, and thus the address objects it manipulates can only be 16 bits in length. An additional mechanism is required to build addresses.

The things connecting an 8086 system to the rest of the world are called ports. The 8086 can access up to 2^{16} 8-bit ports analogous to memory bytes. Each 8-bit port is assigned a unique address ranging from 0 to $2^{16}-1$. Any two consecutive 8-bit ports can be treated as a 16-bit port analogous to memory words. Through these ports, 8086 can receive information about external events and can send out signals that control other events.

The 8086 processor contains a total of thirteen 16-bit registers and nine 1-bit flags. The registers are subdivided into four sets. Three of the sets each contain four registers. The thirteenth register is the instruction pointer. The programmer does not use it, so it is in a set by itself.

The registers are divided into the general registers, the pointer and index registers, and the segment registers.

Instructions in 8086 usually perform operations on one or two operands. In the case of one operand, the operand-addressing mode is

sometimes referred to as indirect memory addressing because the operand is in memory but the offset is not specified directly. For the two operands, the two-operand instruction using the w field to indicate the operands are eight bits (w = 0) or 16 bits (w = 1). Another is a new field not encountered before, namely the d field (d stands for destination). The d field specifies whether the result should be stored back into the operand specified by the mod field and r/m field(d = 0) or into operand specified by the reg field (d = 1).

The operand into which the result is to be stored is called the destination operand, and the remaining operand is called the source operand.

One of the operands of a two-operand instruction can be a constant contained in the instruction itself. Since instructions are frequently located in read-only memories(ROMs), this would be a ideal place to keep constant operands. It is not allowed by the memory to store a result back into such an operand.

New words and Phrases

register 寄存器
general register 通用寄存器
intermediate result 中间结果
pointer and index register 指针和索引寄存器
information 信息
memory 内存
segment register 段寄存器
instruction pointer 指令指针
flag 标志位
processor 处理器
operation 操作
bit 比特,位
byte 字节
word 字
manipulate 操作
input or output port 输入或输出端口
integrated-circuit chip 集成电路芯片
operand 操作数
designate 指明,标示
external event 外界事件
operand-addressing model 操

作数 寻址模式
offset 偏移量
even address 偶地址
destination operand 目标 操作数
source operand 源操作数
Read-Only Memory(ROM) 只读存贮器
constant operand 常量操作数

1.2 8086 Family Architecture

The 8086 family is considered individually as third-generation microprocessors. This system architecture specifies how the processors and other components relate to each other, and it is the key to the exceptional versatility of these products. The components in the 8086 family have been designed to operate together in diverse combinations within the systematic framework of the overall family architecture. So a single family of components can be used to solve a wide array of microcomputing problems. Finally, the modular structure of the family architecture provides an orderly way for systems to grow and change. All the components which constitute the 8086 microprocessor family are described as follows:

·Microprocessors

Microprocessors have the following characteristics:

1. Standard operating speed is 5 MHz (200 ns cycle time); a selected 8 MHz version of the 8086 CPU is also available.

2. Chips are housed in reliable 40-Pin packages.

3. Processors operate on both 8-bit and 16-bit data types; but internal data paths are at least 16-bits wide.

4. Up to 1 megabyte of memory can be addressed, besides a separate 64K byte I/O space.

5. The address/data and status interfaces of the processors are com-

patible (the address and the data buses are time-multiplexed at the processor, i.e., an address transmission is followed by a data transmission over a subset of the same physical lines).

The 8086 is third-generation central processing units (CPU) that differ primarily in their external data paths. In one bus cycle, the 8086 can transfer either 8-bit or 16-bits. Therefore, the 8086 is capable of greater throughput. The processor has two kinds of operating mode.

In maximum mode, an 8288 Bus Controller assumes responsibility for controlling devices attached to the system bus; in minimum mode, the CPUs emit the bus control signals needed by memory and I/O peripheral components.

· Interrupt Controller

The 8086 family-compatible version of the familiar 8259 has been enhanced to operate on the advanced interrupt facilities of the 8086 and the 8088 CPUs. The 8059A accepts interrupt requests from up to eight sources at most.

· Bus Interface Components

Except for the 8284, all components are optional; their inclusion in a system is based on the needs of the application. All of the bus interface components are implemented using bipolar technology to provide high-quality, high-drive signals and very fast internal switching.

· Multiprocessing

Employing multiple processors in medium to large systems offers several significant advantages over the centralized approach that relies on a single CPU and extremely fast memory.

The 8086 family architecture is explicitly designed to simplify the development of multiple processor systems by providing facilities for coordinating the interaction of the processors. The architecture supports two types of processors: independent processors and coprocessors. The 8086

family architecture provides built-in solutions to two classic multiprocessing coordination problems: bus arbitration and mutual exclusion.

·Bus Organization

The 8086 family has two different types of buses: system and local. Both buses may be shared by multiple processors. Microprocessors are always connected to a local bus, and memory and I/O components usually reside on a system bus. The 8086 family bus interface components link a local bus to a system bus.

The local bus is optimized for use by the 8086 family microprocessors. Standard memory and I/O components are not attached to the local bus, so information can be multiplexed and encoded to make very efficient use of processor pins. A full implementation of an 8086 system bus consists of the following five sets of signals: address bus, data bus, control bus, interrupt lines, and arbitration lines. The system bus designed as is modulars and subsets may be implemented according to the needs of the application. A group of bus interface components transforms the signals of a local bus into a system bus. The number of bus interface components required to generate a system bus depends on the size and complexity of the system.

The processor(s) and bus interface group(s) that are connected by a local bus constitute a processing module. A simple processing module could consist of a single CPU and one bus interface group. A more complex module would contain multiple processors, such as two IOPs, or a CPU and one or two IOPs. One bus interface group typically links the processors in the module to a public system bus; a second bus interface group may be connected to a processing module's local bus, generating a second bus. This bus can provide the processing module with a private address space that is not accessible to other processing modules.

New Words and Phrases

architecture 体系结构
microprocessor 微处理器
component 元件,部件
versatility 多功能性,多方面性
product 产品
diverse 多种多样的,不同的
framework 框架,结构
microcomputing 微计算
modular 有标准组件的
characteristic 特征
package 组件
megabyte 兆字节
interface 接口
compatible 兼容的,一致的
bus 总线
time-multiplexed 时分多路
path 路径
bus cycle 总线周期
throughput 流量,容许量
controller 控制器
peripheral component 外围部件
central processing units (CPU) 中央处理部件
interrupt controller 中断控制器
facility 设备,机构,容易
coprocessor 协处理器
built-in 插入,加入,内部
multiprocessing 多重处理
coordination 协调
arbitration 仲裁
mutual exclusion 互斥
operating mode 操作模式
local bus 局部总线
system bus 系统总线
encode 译成密码,编码
pin 管脚,杆头,引线

1.3 8086 Central Processing Units (CPUs)

In almost every other respect the processors are identical; software for one CPU will execute on the other without alteration. The outstanding characteristics of 8086 is that it is suitable for an very wide spectrum of

microcomputer application. Because of the processors' dual operating modes (minimum and maximum mode) and built-in multiprocessing features, the 8086 can be used in the large domain. Several of the 40 CPU pins have dual functions that are selected by a strapping pin. In the case of minimum mode, these pins transfer control signals directly to memory and input/output devices. In maximum mode these same pins take on different functions that are helpful in medium to large systems, especially systems with multiple processors. The control functions assigned to these pins in minimum mode are assumed by a support chip, the 8288 Bus Controller.

The 8086's CPU is substantially more powerful than any microprocessor previously offered by Intel. The 8086's advantage over the 8088 is attributable to its 16-bit external data bus. Software for high-performance 8086 system need not be written in assembly language. The CPUs are designed to provide direct hardware support for programs written in high-level languages such as Intel's PL/M-86. Most high-level languages store variables in memory; the 8086 symmetrical instruction set supports direct operation on memory operands, including operands on the stack. The hardware addressing modes provide efficient, straightforward implementations of based variables, arrays, arrays of structures and other high-level language data constructs.

Executing a instruction includes the steps shown below:

1. Fetch the next instruction from memory
2. Read an operand(if nesessary)
3. Execute the instruction
4. Write the result (if necessary)

While 8086 CPU perfoms the same steps, it allocates them to two separate processing units within the CPU; they are the execution unit (EU) and the bus interface unit(BIU). The execution unit executes in-